

High-Speed CMOS Logic Digital Phase-Locked Loop

Features

- Digital Design Avoids Analog Compensation Errors
- Easily Cascadable for Higher Order Loops
- Useful Frequency Range
 - K-Clock DC to 55MHz (Typ)
 - I/D-Clock DC to 35MHz (Typ)
- Dynamically Variable Bandwidth
- Very Narrow Bandwidth Attainable
- Power-On Reset
- Output Capability
 - Standard XORPD_{OUT}, ECPD_{OUT}
 - Bus Driver I/D_{OUT}
- Fanout (Over Temperature Range)
 - Standard Outputs 10 LSTTL Loads
 - Bus Driver Outputs 15 LSTTL Loads
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- 'HC297 Types
 - Operation Voltage 2 to 6V
 - High Noise Immunity N_{IL} = 30%, N_{IH} = 30% of V_{CC} at 5V
- CD74HCT297 Types
 - Operation Voltage 4.5 to 5.5V
 - Direct LSTTL Input Logic Compatibility
V_{IL} = 0.8V (Max), V_{IH} = 2V (Min)
 - CMOS Input Compatibility I_I ≤ 1μA at V_{OL}, V_{OH}

Description

The 'HC297 and CD74HCT297 are high-speed silicon gate CMOS devices that are pin-compatible with low power Schottky TTL (LSTTL).

These devices are designed to provide a simple, cost-effective solution to high-accuracy, digital, phase-locked-loop applications. They contain all the necessary circuits, with the exception of the divide-by-N counter, to build first-order phase-locked-loops.

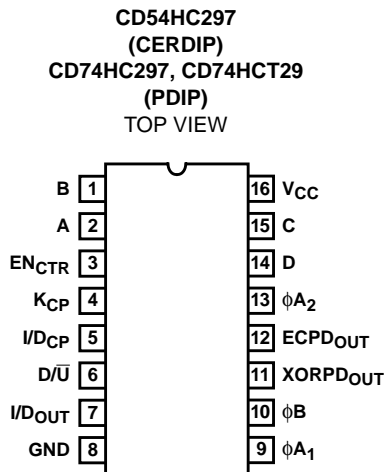
Both EXCLUSIVE-OR (XORPD) and edge-controlled phase detectors (ECPD) are provided for maximum flexibility. The input signals for the EXCLUSIVE-OR phase detector must have a 50% duty factor to obtain the maximum lock-range.

Proper partitioning of the loop function, with many of the building blocks external to the package, makes it easy for the designer to incorporate ripple cancellation (see Figure 2) or to cascade to higher order phase-locked-loops.

The length of the up/down K-counter is digitally programmable according to the K-counter function table. With A, B, C and D all LOW, the K-counter is disabled. With A HIGH and B, C and D LOW, the K-counter is only three stages long, which widens the bandwidth or capture range and shortens the lock time of the loop. When A, B, C and D are all programmed HIGH, the K-counter becomes seventeen stages long, which narrows the bandwidth or capture range and lengthens the lock time. Real-time control of loop bandwidth by manipulating the A to D inputs can maximize the overall performance of the digital phase-locked-loop.

The 'HC297 and CD74HCT297 can perform the classic first order phase-locked-loop function without using analog components. The accuracy of the digital phase-locked-loop (DPLL) is not affected by V_{CC} and temperature variations but depends solely on accuracies of the K-clock and loop propagation delays.

Pinout



Ordering Information

| PART NUMBER | TEMP. RANGE (°C) | PACKAGE |
|--------------|------------------|--------------|
| CD54HC297F3A | -55 to 125 | 16 Ld CERDIP |
| CD74HC297E | -55 to 125 | 16 Ld PDIP |
| CD74HCT297E | -55 to 125 | 16 Ld PDIP |

CD54HC297, CD74HC297, CD74HCT297

The phase detector generates an error signal waveform that, at zero phase error, is a 50% duty factor square wave. At the limits of linear operation, the phase detector output will be either HIGH or LOW all of the time depending on the direction of the phase error ($\phi_{IN} - \phi_{OUT}$). Within these limits the phase detector output varies linearly with the input phase error according to the gain K_d , which is expressed in terms of phase detector output per cycle or phase error. The phase detector output can be defined to vary between ± 1 according to the relation:

$$\text{phase detector output} = \frac{\%HIGH - \%LOW}{100}$$

The output of the phase detector will be $K_d\phi_e$, where the phase error $\phi_e = \phi_{IN} - \phi_{OUT}$.

EXCLUSIVE-OR phase detectors (XORPD) and edge-controlled phase detectors (ECPD) are commonly used digital types. The ECPD is more complex than the XORPD logic function but can be described generally as a circuit that changes states on one of the transitions of its inputs. The gain (K_d) for an XORPD is 4 because its output remains HIGH (XORPD_{OUT} = 1) for a phase error of one quarter cycle.

Similarly, K_d for the ECPD is 2 since its output remains HIGH for a phase error of one half cycle. The type of phase detector will determine the zero-phase-error point, i.e., the phase separation of the phase detector inputs for a ϕ_e defined to be zero. For the basic DPLL system of Figure 3, $\phi_e = 0$ when the phase detector output is a square wave.

The XORPD inputs are one quarter cycle out-of-phase for zero phase error. For the ECPD, $\phi_e = 0$ when the inputs are one half cycle out of phase.

The phase detector output controls the up/down input to the K-counter. The counter is clocked by input frequency Mf_c which is a multiple M of the loop center frequency f_c . When the K-counter recycles up, it generates a carry pulse. Recycling while counting down generates a borrow pulse. If the carry and the borrow outputs are conceptually combined into one output that is positive for a carry and negative for a borrow, and if the K-counter is considered as a frequency divider with the ratio Mf_c/K , the output of the K-counter will equal the input frequency multiplied by the division ratio. Thus the output from the K-counter is $(K_d\phi_e Mf_c)/K$.

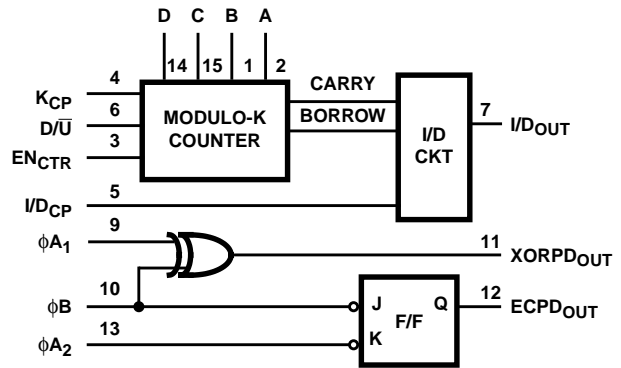
The carry and borrow pulses go to the increment/decrement (I/D) circuit which, in the absence of any carry or borrow pulses has an output that is one half of the input clock (I/D_{CP}). The input clock is just a multiple, $2N$, of the loop center frequency. In response to a carry or borrow pulse, the I/D circuit will either add or delete a pulse at I/D_{OUT} . Thus the output of the I/D circuit will be $Nf_c + (K_d\phi_e Mf_c)/2K$.

The output of the N-counter (or the output of the phase-locked-loop) is thus: $f_o = f_c + (K_d\phi_e Mf_c)/2KN$.

If this result is compared to the equation for a first-order analog phase-locked-loop, the digital equivalent of the gain of the VCO is just $Mf_c/2KN$ or f_c/K for $M = 2N$.

Thus, the simple first-order phase-locked-loop with an adjustable K-counter is the equivalent of an analog phase-locked-loop with a programmable VCO gain.

Functional Diagram



**FUNCTION TABLE
EXCLUSIVE-OR PHASE DETECTOR**

| ϕA_1 | ϕB | XORPD OUT |
|------------|----------|-----------|
| L | L | L |
| L | H | H |
| H | L | H |
| H | H | L |

**FUNCTION TABLE
EDGE-CONTROLLED PHASE DETECTOR**

| ϕA_2 | ϕB | ECPD OUT |
|------------|----------|-----------|
| H or L | ↓ | H |
| ↓ | H or L | L |
| H or L | ↑ | No Change |
| ↑ | H or L | No Change |

H = Steady-State High Level, L = Steady-State Low Level, ↑ = LOW to HIGH ϕ Transition, ↓ = HIGH to LOW ϕ Transition

**K-COUNTER FUNCTION TABLE
(DIGITAL CONTROL)**

| D | C | B | A | MODULO (K) |
|---|---|---|---|------------|
| L | L | L | L | Inhibited |
| L | L | L | H | 2^3 |
| L | L | H | L | 2^4 |
| L | L | H | H | 2^5 |
| L | H | L | L | 2^6 |
| L | H | L | H | 2^7 |
| L | H | H | L | 2^8 |
| L | H | H | H | 2^9 |
| H | L | L | L | 2^{10} |
| H | L | L | H | 2^{11} |
| H | L | H | L | 2^{12} |
| H | L | H | H | 2^{13} |
| H | H | L | L | 2^{14} |
| H | H | L | H | 2^{15} |
| H | H | H | L | 2^{16} |
| H | H | H | H | 2^{17} |

CD54HC297, CD74HC297, CD74HCT297

Absolute Maximum Ratings

| | |
|--|-------------|
| DC Supply Voltage, V_{CC} | -0.5V to 7V |
| DC Input Diode Current, I_{IK} | |
| For $V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$ | $\pm 20mA$ |
| DC Output Diode Current, I_{OK} | |
| For $V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$ | $\pm 20mA$ |
| DC Drain Current, per Output, I_O | |
| For $-0.5V < V_O < V_{CC} + 0.5V$ | $\pm 25mA$ |
| DC Output Source or Sink Current per Output Pin, I_O | |
| For $V_O > -0.5V$ or $V_O < V_{CC} + 0.5V$ | $\pm 25mA$ |
| DC V_{CC} or Ground Current, I_{CC} | $\pm 50mA$ |

Thermal Information

| | |
|--|------------------------------------|
| Thermal Resistance (Typical, Note 1) | θ_{JA} ($^{\circ}C/W$) |
| E (PDIP) Package | 67 |
| Maximum Junction Temperature | 150 $^{\circ}C$ |
| Maximum Storage Temperature Range | -65 $^{\circ}C$ to 150 $^{\circ}C$ |
| Maximum Lead Temperature (Soldering 10s) | 300 $^{\circ}C$ |

Operating Conditions

| | |
|--|------------------------------------|
| Temperature Range, T_A | -55 $^{\circ}C$ to 125 $^{\circ}C$ |
| Supply Voltage Range, V_{CC} | |
| HC Types | .2V to 6V |
| HCT Types | 4.5V to 5.5V |
| DC Input or Output Voltage, V_I, V_O | 0V to V_{CC} |
| Input Rise and Fall Time | |
| 2V | 1000ns (Max) |
| 4.5V | 500ns (Max) |
| 6V | 400ns (Max) |

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

- The package thermal impedance is calculated in accordance with JESD 51-7.

DC Electrical Specifications

| PARAMETER | SYMBOL | TEST CONDITIONS | | V_{CC} (V) | 25 $^{\circ}C$ | | | -40 $^{\circ}C$ TO 85 $^{\circ}C$ | | -55 $^{\circ}C$ TO 125 $^{\circ}C$ | | UNITS |
|---|----------|-------------------------|------------------|--------------|----------------|-----|------|-----------------------------------|------|------------------------------------|------|-------|
| | | V_I (V) | I_O (mA) | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| HC TYPES | | | | | | | | | | | | |
| High Level Input Voltage | V_{IH} | - | - | 2 | 1.5 | - | - | 1.5 | - | 1.5 | - | V |
| | | | | 4.5 | 3.15 | - | - | 3.15 | - | 3.15 | - | V |
| | | | | 6 | 4.2 | - | - | 4.2 | - | 4.2 | - | V |
| Low Level Input Voltage | V_{IL} | - | - | 2 | - | - | 0.5 | - | 0.5 | - | 0.5 | V |
| | | | | 4.5 | - | - | 1.35 | - | 1.35 | - | 1.35 | V |
| | | | | 6 | - | - | 1.8 | - | 1.8 | - | 1.8 | V |
| High Level Output Voltage CMOS Loads | V_{OH} | V_{IH} or V_{IL} | -0.02 | 2 | 1.9 | - | - | 1.9 | - | 1.9 | - | V |
| | | | -0.02 | 4.5 | 4.4 | - | - | 4.4 | - | 4.4 | - | V |
| | | | -0.02 | 6 | 5.9 | - | - | 5.9 | - | 5.9 | - | V |
| High Level Output Voltage TTL Loads | V_{OH} | V_{IH} or V_{IL} | -6 (Note 2) | 4.5 | 3.98 | - | - | 3.84 | - | 3.7 | - | V |
| | | | -7.8 (Note 2) | 6 | 5.48 | - | - | 5.34 | - | 5.2 | - | V |
| Low Level Output Voltage CMOS Loads | V_{OL} | V_{IH} or V_{IL} | 0.02 | 2 | - | - | 0.1 | - | 0.1 | - | 0.1 | V |
| | | | 0.02 | 4.5 | - | - | 0.1 | - | 0.1 | - | 0.1 | V |
| | | | 0.02 | 6 | - | - | 0.1 | - | 0.1 | - | 0.1 | V |
| Low Level Output Voltage TTL Loads | V_{OL} | V_{IH} or V_{IL} | 4 (Note 2) | 4.5 | - | - | 0.26 | - | 0.33 | - | 0.4 | V |
| | | | 5.2 (Note 2) | 6 | - | - | 0.26 | - | 0.33 | - | 0.4 | V |

CD54HC297, CD74HC297, CD74HCT297

DC Electrical Specifications (Continued)

| PARAMETER | SYMBOL | TEST CONDITIONS | | V _{CC} (V) | 25°C | | | -40°C TO 85°C | | -55°C TO 125°C | | UNITS |
|--|---------------------------|------------------------------------|---------------------|---------------------|------|-----|------|---------------|------|----------------|-----|-------|
| | | V _I (V) | I _O (mA) | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| Input Leakage Current | I _I | V _{CC} or GND | - | 6 | - | - | ±0.1 | - | ±1 | - | ±1 | μA |
| Quiescent Device Current | I _{CC} | V _{CC} or GND | 0 | 6 | - | - | 8 | - | 80 | - | 160 | μA |
| HCT TYPES | | | | | | | | | | | | |
| High Level Input Voltage | V _{IH} | - | - | 4.5 to 5.5 | 2 | - | - | 2 | - | 2 | - | V |
| Low Level Input Voltage | V _{IL} | - | - | 4.5 to 5.5 | - | - | 0.8 | - | 0.8 | - | 0.8 | V |
| High Level Output Voltage CMOS Loads | V _{OH} | V _{IH} or V _{IL} | -0.02 | 4.5 | 4.4 | - | - | 4.4 | - | 4.4 | - | V |
| High Level Output Voltage TTL Loads | | | -4 | 4.5 | 3.98 | - | - | 3.84 | - | 3.7 | - | V |
| Low Level Output Voltage CMOS Loads | V _{OL} | V _{IH} or V _{IL} | 0.02 | 4.5 | - | - | 0.1 | - | 0.1 | - | 0.1 | V |
| Low Level Output Voltage TTL Loads | | | 4 | 4.5 | - | - | 0.26 | - | 0.33 | - | 0.4 | V |
| Input Leakage Current | I _I | V _{CC} to GND | 0 | 5.5 | - | - | ±0.1 | - | ±1 | - | ±1 | μA |
| Quiescent Device Current | I _{CC} | V _{CC} or GND | 0 | 5.5 | - | - | 8 | - | 80 | - | 160 | μA |
| Additional Quiescent Device Current Per Input Pin: 1 Unit Load | ΔI _{CC} (Note 2) | V _{CC} -2.1 | - | 4.5 to 5.5 | - | 100 | 360 | - | 450 | - | 490 | μA |

NOTE:

2. For dual-supply systems theoretical worst case (V_I = 2.4V, V_{CC} = 5.5V) specification is 1.8mA.

HCT Input Loading Table

| INPUT | UNIT LOADS |
|---|------------|
| EN _{CTR} , D/ <u>U</u> | 0.3 |
| A, B, C, D, K _{CP} , φA ₂ | 0.6 |
| I/D _{CP} , φA ₁ , φB | 1.5 |

NOTE: Unit Load is ΔI_{CC} limit specified in DC Electrical Specifications table, e.g., 360μA max at 25°C.

CD54HC297, CD74HC297, CD74HCT297

Prerequisite For Switching Function

| PARAMETER | SYMBOL | V _{CC} (V) | 25°C | | -40°C TO 85°C | | -55°C TO 125°C | | UNITS |
|--|------------------|---------------------|------|-----|---------------|-----|----------------|-----|-------|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| HC TYPES | | | | | | | | | |
| Maximum Clock Frequency K _{CP} | f _{MAX} | 2 | 6 | - | 5 | - | 4 | - | MHz |
| | | 4.5 | 30 | - | 24 | - | 20 | - | MHz |
| | | 6 | 35 | - | 28 | - | 24 | - | MHz |
| Maximum Clock Frequency I/D _{CP} | f _{MAX} | 2 | 4 | - | 3 | - | 2 | - | MHz |
| | | 4.5 | 20 | - | 16 | - | 13 | - | MHz |
| | | 6 | 24 | - | 19 | - | 15 | - | MHz |
| Clock Pulse Width K _{CP} | t _w | 2 | 80 | - | 100 | - | 120 | - | ns |
| | | 4.5 | 16 | - | 20 | - | 24 | - | ns |
| | | 6 | 14 | - | 17 | - | 20 | - | ns |
| Clock Pulse Width I/D _{CP} | t _w | 2 | 125 | - | 155 | - | 190 | - | ns |
| | | 4.5 | 25 | - | 31 | - | 38 | - | ns |
| | | 6 | 21 | - | 26 | - | 32 | - | ns |
| Set-up Time D/ \bar{U} , EN _{CTR} to K _{CP} | t _{SU} | 2 | 100 | - | 125 | - | 150 | - | ns |
| | | 4.5 | 20 | - | 25 | - | 30 | - | ns |
| | | 6 | 17 | - | 21 | - | 26 | - | ns |
| Hold Time D/ \bar{U} , EN _{CTR} to K _{CP} | t _H | 2 | 0 | - | 0 | - | 0 | - | ns |
| | | 4.5 | 0 | - | 0 | - | 0 | - | ns |
| | | 6 | 0 | - | 0 | - | 0 | - | ns |
| HCT TYPES | | | | | | | | | |
| Maximum Clock Frequency K _{CP} | f _{MAX} | 4.5 | 30 | - | 24 | - | 20 | - | MHz |
| Maximum Clock Frequency I/D _{CP} | f _{MAX} | 4.5 | 20 | - | 16 | - | 13 | - | MHz |
| Clock Pulse Width K _{CP} | t _w | 4.5 | 16 | - | 20 | - | 24 | - | ns |
| Clock Pulse Width I/D _{CP} | t _w | 4.5 | 25 | - | 31 | - | 38 | - | ns |
| Set-up Time D/ \bar{U} , EN _{CTR} to K _{CP} | t _{SU} | 4.5 | 20 | - | 25 | - | 30 | - | ns |
| Hold Time D/ \bar{U} , EN _{CTR} to K _{CP} | t _H | 4.5 | 0 | - | 0 | - | 0 | - | ns |

Switching Specifications Input t_r, t_f = 6ns

| PARAMETER | SYMBOL | TEST CONDITIONS | V _{CC} (V) | 25°C | | -40°C TO 85°C | -55°C TO 125°C | UNITS |
|---|-------------------------------------|-----------------------|---------------------|------|-----|---------------|----------------|-------|
| | | | | TYP | MAX | MAX | MAX | |
| HC TYPES | | | | | | | | |
| Propagation Delay, I/D _{CP} to I/D _{OUT} | t _{PLH} , t _{PHL} | C _L = 50pF | 2 | - | 175 | 220 | 265 | ns |
| | | | 4.5 | - | 35 | 44 | 53 | ns |
| | | | 6 | - | 30 | 34 | 43 | ns |

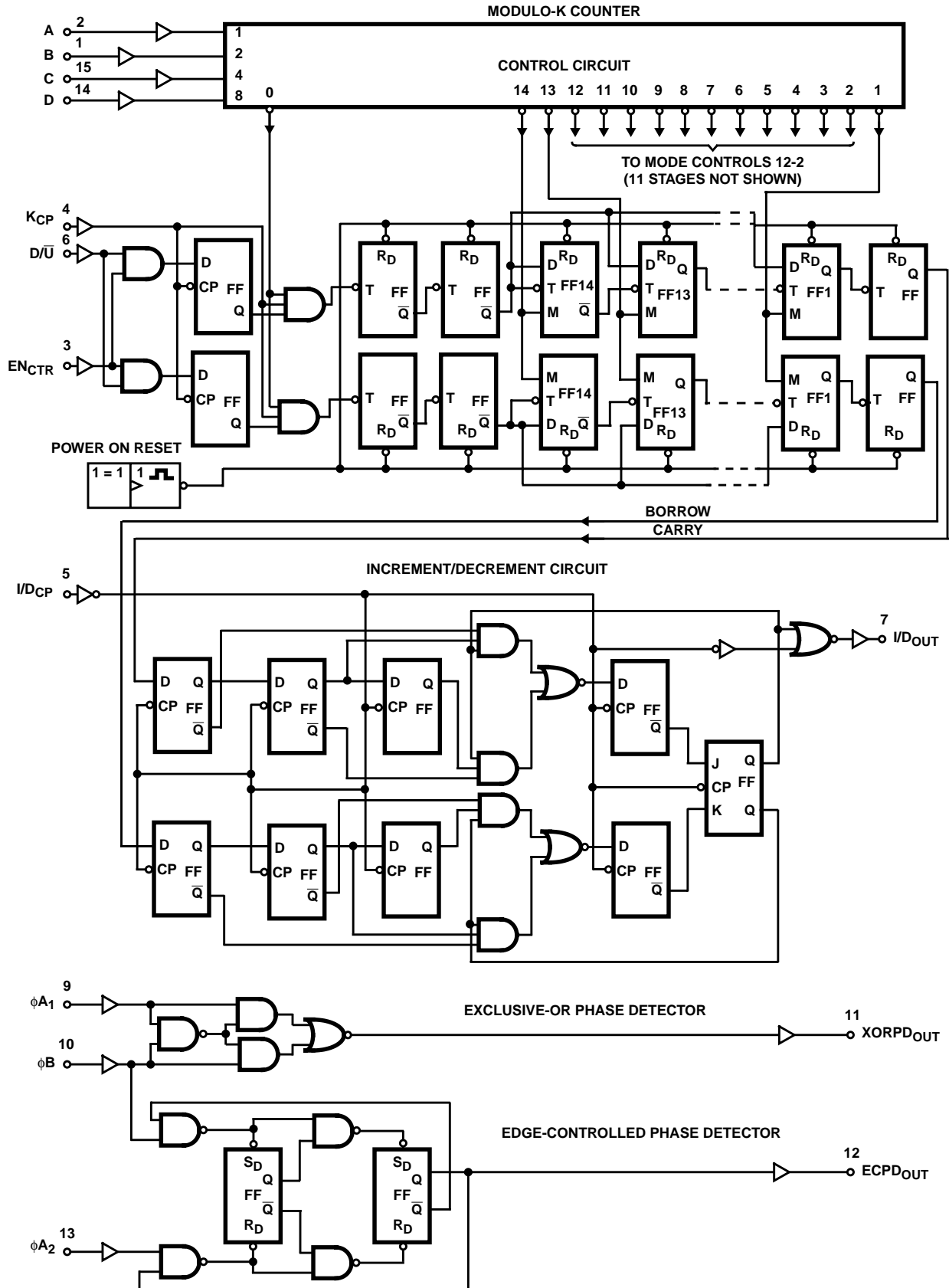
CD54HC297, CD74HC297, CD74HCT297

Switching Specifications Input $t_r, t_f = 6\text{ns}$ (Continued)

| PARAMETER | SYMBOL | TEST CONDITIONS | V _{CC} (V) | 25°C | | -40°C TO 85°C | -55°C TO 125°C | UNITS |
|---|--------------------|---------------------|---------------------|------|-----|---------------|----------------|-------|
| | | | | TYP | MAX | MAX | MAX | |
| Propagation Delay, $\phi A_1, \phi B$ to XORPD _{OUT} | t_{PLH}, t_{PHL} | $C_L = 50\text{pF}$ | 2 | - | 150 | 190 | 225 | ns |
| | | | 4.5 | - | 30 | 38 | 45 | ns |
| | | | 6 | - | 26 | 33 | 38 | ns |
| Propagation Delay, $\phi B, \phi A_2$ to ECPD _{OUT} | t_{PHL}, t_{PHL} | $C_L = 50\text{pF}$ | 2 | - | 200 | 250 | 300 | ns |
| | | | 4.5 | - | 40 | 50 | 60 | ns |
| | | | 6 | - | 34 | 43 | 51 | ns |
| Output Transition Time XORPD _{OUT} ECPD _{OUT} | t_{TLH} | $C_L = 50\text{pF}$ | 2 | - | 75 | 95 | 110 | ns |
| | | | 4.5 | - | 15 | 19 | 22 | ns |
| | | | 6 | - | 13 | 16 | 19 | ns |
| Output Transition Time I/D _{OUT} | t_{TLH} | $C_L = 50\text{pF}$ | 2 | - | 60 | 75 | 90 | ns |
| | | | 4.5 | - | 12 | 15 | 18 | ns |
| | | | 6 | - | 10 | 13 | 15 | ns |
| Input Capacitance | C_I | - | - | - | 10 | 10 | 10 | pF |
| HCT TYPES | | | | | | | | |
| Propagation Delay, I/DCP to I/D _{OUT} | t_{PLH}, t_{PHL} | $C_L = 50\text{pF}$ | 4.5 | - | 35 | 44 | 53 | ns |
| Propagation Delay, $\phi A_1, \phi B$ to XORPD _{OUT} | t_{PLH}, t_{PHL} | $C_L = 50\text{pF}$ | 4.5 | - | 30 | 38 | 45 | ns |
| Propagation Delay, $\phi B, \phi A_2$ to ECPD _{OUT} | t_{PHL}, t_{PHL} | $C_L = 50\text{pF}$ | 4.5 | - | 40 | 50 | 60 | ns |
| Output Transition Time XORPD _{OUT} | t_{TLH} | $C_L = 50\text{pF}$ | 4.5 | - | 15 | 19 | 22 | ns |
| Output Transition Time ECPD _{OUT} | t_{TLH} | $C_L = 50\text{pF}$ | 4.5 | - | 12 | 15 | 18 | ns |
| Input Capacitance | C_I | - | - | - | 10 | 10 | 10 | pF |

CD54HC297, CD74HC297, CD74HCT297

Logic Diagram



CD54HC297, CD74HC297, CD74HCT297

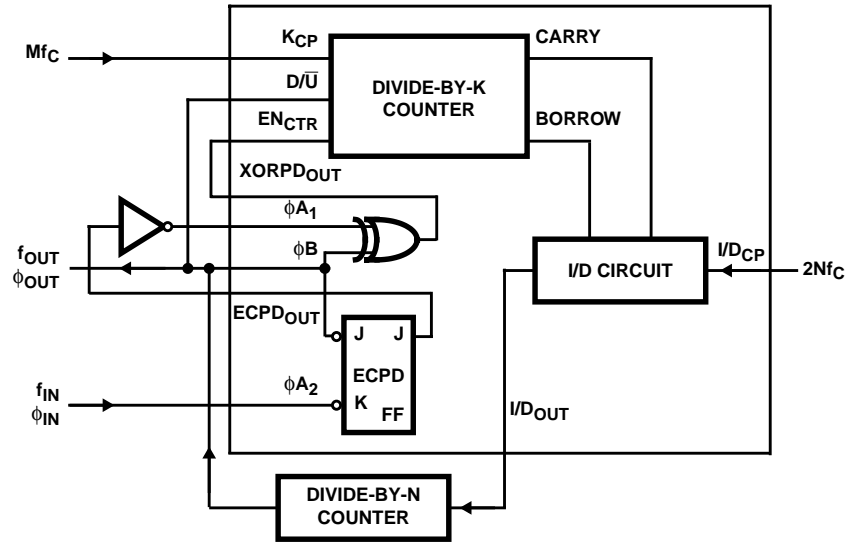


FIGURE 1. DPLL USING BOTH PHASE DETECTORS IN A RIPPLE-CANCELLATION SCHEME

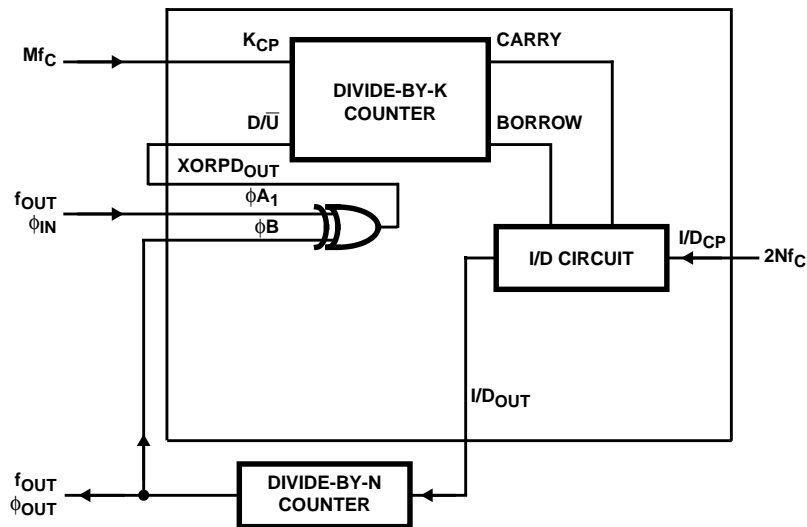


FIGURE 2. DPLL USING EXCLUSIVE-OR PHASE DETECTION

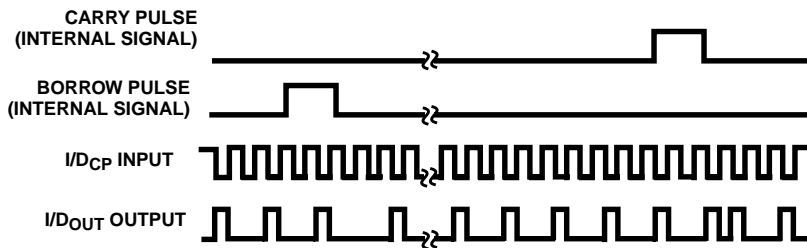


FIGURE 3. TIMING DIAGRAM: I/D_{OUT} IN-LOCK CONDITION

CD54HC297, CD74HC297, CD74HCT297

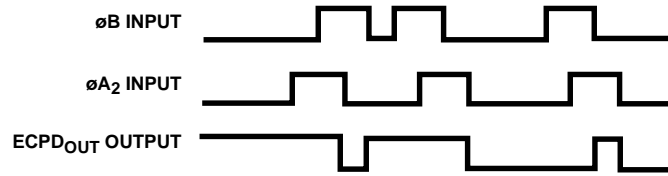


FIGURE 4. TIMING DIAGRAM: EDGE CONTROLLED PHASE COMPARATOR WAVEFORMS

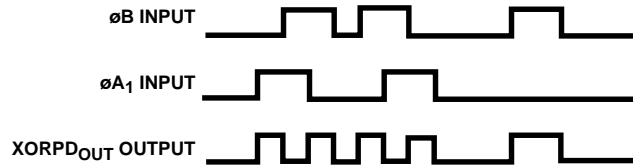


FIGURE 5. TIMING DIAGRAM: EXCLUSIVE OR PHASE DETECTOR WAVEFORMS

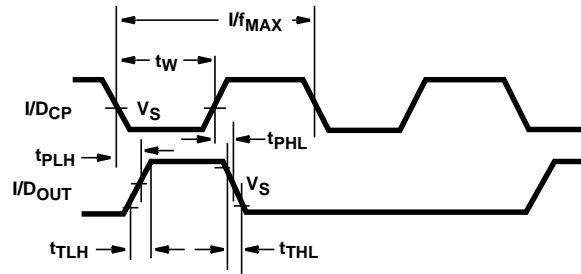


FIGURE 6. WAVEFORMS SHOWING THE CLOCK (I/D_{CP}) TO OUTPUT (I/D_{OUT}) PROPAGATION DELAYS, CLOCK PULSE WIDTH, OUTPUT TRANSITION TIMES AND MAXIMUM CLOCK PULSE FREQUENCY

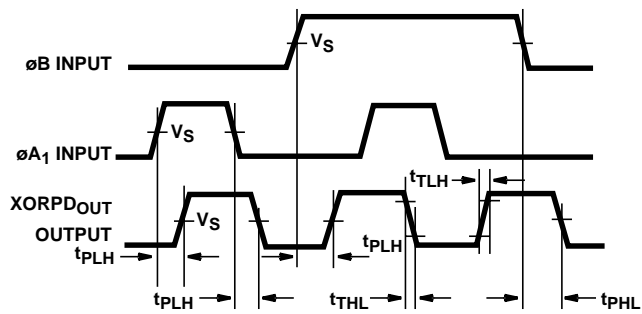


FIGURE 7. WAVEFORMS SHOWING THE PHASE INPUT (ϕB , ϕA_1) TO OUTPUT ($XORPD_{OUT}$) PROPAGATION DELAYS AND OUTPUT TRANSITION TIMES

CD54HC297, CD74HC297, CD74HCT297

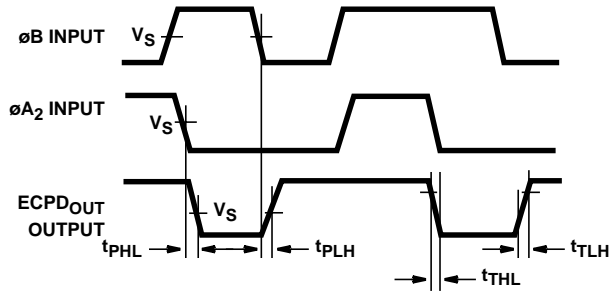
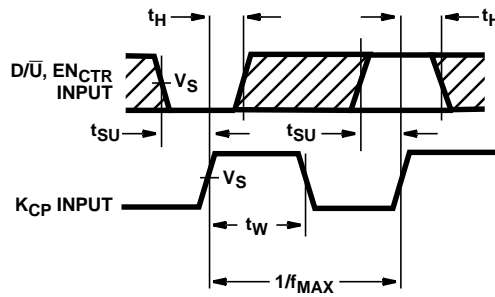


FIGURE 8. WAVEFORMS SHOWING THE PHASE INPUT (ϕB , ϕA_2) TO OUTPUT (ECPD_{OUT}) PROPAGATION DELAYS AND OUTPUT TRANSITION TIMES



NOTE: The shaded areas indicate when the input is permitted to change for predictable output performance.

FIGURE 9. WAVEFORMS SHOWING THE CLOCK (K_{CP}) PULSE WIDTH AND MAXIMUM CLOCK PULSE FREQUENCY, AND THE INPUT (D/ \bar{U} , EN_{CTR}) TO CLOCK (K_{CP}) SETUP AND HOLD TIMES

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|------------------|--------------------------------------|----------------------|--------------|--------------------------------|-------------------------|
| 5962-8999001EA | ACTIVE | CDIP | J | 16 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-8999001EA CD54HC297F3A | Samples |
| CD54HC297F3A | ACTIVE | CDIP | J | 16 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-8999001EA CD54HC297F3A | Samples |
| CD74HC297E | ACTIVE | PDIP | N | 16 | 25 | RoHS & Green | NIPDAU | N / A for Pkg Type | -55 to 125 | CD74HC297E | Samples |
| CD74HC297EE4 | ACTIVE | PDIP | N | 16 | 25 | TBD | Call TI | Call TI | -55 to 125 | | Samples |
| CD74HCT297E | ACTIVE | PDIP | N | 16 | 25 | RoHS & Green | NIPDAU | N / A for Pkg Type | -55 to 125 | CD74HCT297E | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF CD54HC297, CD74HC297 :

- Catalog : [CD74HC297](#)
- Military : [CD54HC297](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TUBE


*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|-------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| CD74HC297E | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| CD74HC297E | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| CD74HCT297E | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| CD74HCT297E | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---------------|------------------------|------------------------|------------------------|------------------------|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package is hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2022, Texas Instruments Incorporated