TPS57160-Q1 1.5-A 60-V Step-Down DC-DC Converter With Eco-mode™ Control

1 Features

- Qualified for Automotive Applications
- 3.5-V to 60-V Input Voltage Range
- 200-mΩ High-Side MOSFET
- High Efficiency at Light Loads With Pulse-Skipping Eco-mode™ Control Scheme
- 116-μA Operating Quiescent Current
- 1.5-μA Shutdown Current
- 100-kHz to 2.5-MHz Switching Frequency
- Synchronizes to External Clock
- Adjustable Slow Start/Sequencing
- Undervoltage and Overvoltage Power-good Output
- Adjustable Undervoltage Lockout (UVLO) Voltage and Hysteresis
- 0.8-V Internal Voltage Reference
- Supported by SwitcherPro™ Software Tool (ti.com/tool/switcherpro)
- Z-Suffix Offers Improved Delamination

2 Applications

- 12-V, 24-V, and 48-V Industrial and Commercial Low-Power Systems
- Aftermarket Automotive Accessories: Video, GPS, Entertainment

3 Description

The TPS57160-Q1 device is a 60-V 1.5-A step-down regulator with an integrated high-side MOSFET. Current-mode control provides simple external compensation and flexible component selection. A low-ripple pulse-skip mode reduces the no load, input supply current to 116 μA. Using the enable pin, shutdown supply current is reduced to 1.5 μA.

Undervoltage lockout is set internally at 2.5 V but can be increased using the enable pin. The output voltage startup ramp is controlled by the slow-start pin that can also be configured for sequencing or tracking. An open-drain power-good signal indicates the output is within 92% to 109% of the nominal voltage.

A wide switching frequency range allows efficiency and external component size to be optimized. Frequency foldback and thermal shutdown protects the part during an overload condition.

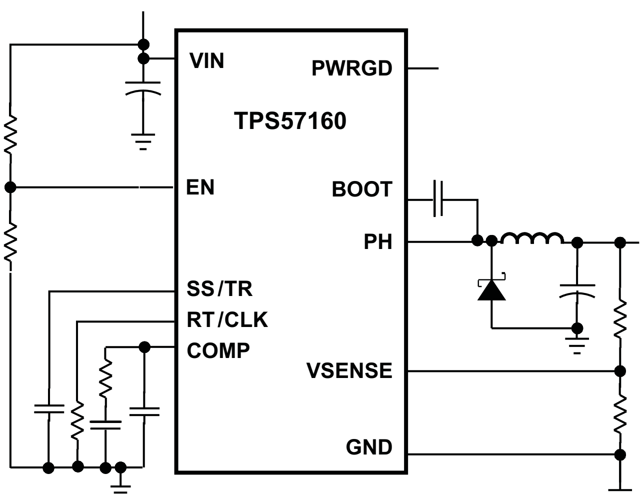
The TPS57160-Q1 device is available in a 10-pin thermally enhanced MSOP-PowerPAD™ (DGQ) or 10-pin VSON (DRC) package. The Z-suffix offers reduced delamination compared to standard device.

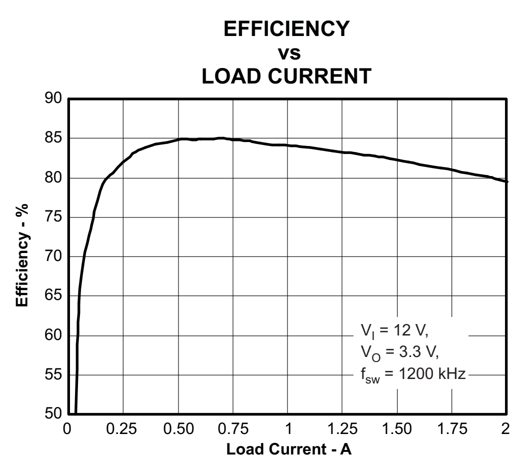
Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS57160-Q1	MSOP-PowerPAD (10)	3.00 mm × 3.00 mm
	VSON (10)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

4 Simplified Schematic





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5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (February 2015) to Revision E — **Page**

- Updated the corner pin values for the CDM ESD rating ... 4
- Changed the thermal information values for the DGQ (MSOP) and DRC (VSON) packages in the *Thermal Information* table ... 5

Changes from Revision C (June 2012) to Revision D — **Page**

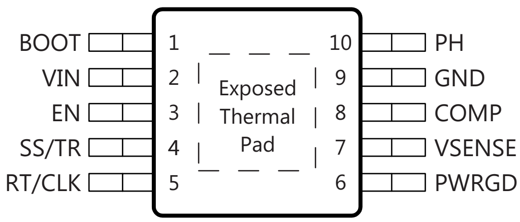
- Added the *ESD Ratings* table, *Feature Description* section, *Device Functional Modes* section, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Released the Z-suffix orderable part number, TPS57160ZQDGQRQ1, which offers improved delamination ... 1
- Updated the voltage reference parameter in the *Electrical Characteristics* table ... 5

Changes from Revision B (March 2011) to Revision C — **Page**

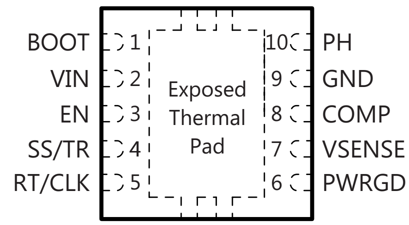
- Changed "regulated output supply current" to "input supply current ... 1
- Updated footnote under Abs Max table. ... 4
- Changed 25°C to 125°C ... 5
- Changed 25°C to 125°C ... 6
- Changed 0.5 to 0.45 ... 6
- Added (Fault) and (Good) to VSENSE rising and falling ... 6
- Changed Figure 21 to match 57060-Q1 ... 10
- Changed "to the COMP" to "from the COMP" ... 14
- Changed "UVLO adjust registers" to "UVLO adjust resistors" ... 14
- Changed power pad to PowerPAD ... 40

6 Pin Configuration and Functions

DGQ Package
10-Pin MSOP-PowerPAD
Top View



DRC Package
10-Pin VSON With Exposed Thermal Pad
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
BOOT	1	O	A bootstrap capacitor is required between BOOT and PH. If the voltage on this capacitor is below the minimum required by the output device, the output is forced to switch off until the capacitor is refreshed.
COMP	8	O	Error amplifier output, and input to the output switch current comparator. Connect frequency compensation components to COMP.
EN	3	I	Enable pin, internal pullup current source. Pull below 1.2 V to disable. Float to enable. Adjust the input undervoltage lockout with two resistors.
GND	9	—	Ground
PH	10	I	The source of the internal high-side power MOSFET.
PWRGD	6	O	Open-drain output, asserts low if output voltage is low due to thermal shutdown, dropout, overvoltage, or EN shut down.
RT/CLK	5	I	Resistor timing and external clock. An internal amplifier holds this pin at a fixed voltage when using an external resistor to ground to set the switching frequency. If the pin is pulled above the PLL upper threshold, a mode change occurs and the pin becomes a synchronization input. The internal amplifier is disabled and the pin is a high impedance clock input to the internal PLL. If clocking edges stop, the internal amplifier is re-enabled and the mode returns to a resistor set function.
SS/TR	4	I	Slow-start and tracking. An external capacitor connected to this pin sets the output rise time. Because the voltage on this pin overrides the internal reference, it can be used for tracking and sequencing.
VIN	2	I	Input supply voltage, 3.5 V to 60 V.
VSENSE	7	I	Inverting node of the transconductance (gm) error amplifier.
Thermal Pad		—	GND pin must be electrically connected to the exposed pad on the printed circuit board for proper operation.

7 Specifications

7.1 Absolute Maximum Ratings

over operating temperature range (unless otherwise noted)[1]

			MIN	MAX	UNIT
Input voltage, V_{IN}	VIN		–0.3	65	V
	EN[2]		–0.3	5	
	BOOT			73	
	VSENSE		–0.3	3	
	COMP		–0.3	3	
	PWRGD		–0.3	6	
	SS/TR		–0.3	3	
	RT/CLK		–0.3	3.6	
Output voltage, V_{OUT}	BOOT to PH			8	V
	PH		–0.6	65	
		200 ns	–1	65	
		30 ns	–2	65	
		Maximum dc voltage, T_J = –40°C		–0.85	
Differential voltage, V_{DIFF}	PAD to GND			±200	mV
Source current, I_{SOURCE}	EN			100	µA
	BOOT			100	mA
	VSENSE			10	µA
	PH		Current Limit		
	RT/CLK			100	µA
Sink current, I_{SINK}	VIN		Current Limit		
	COMP			100	µA
	PWRGD			10	mA
	SS/TR			200	µA
Operating junction temperature, T_J			–40	150	°C
Storage temperature, T_{stg}			–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated is not implied. Exposure beyond absolute maximum rated conditions for extended periods may affect device reliability.
(2) See the *Enable and Adjusting Undervoltage Lockout* section for details.

7.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002[1]		±2000	V
		Charged-device model (CDM), per AEC Q100-011	All pins	±500	
			Corner pins (1, 5, 6, and 10)	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
T_A	Operating ambient temperature	–40		125	°C

7.4 Thermal Information

THERMAL METRIC[(1)(2)]		DGQ (MSOP-PowerPAD) 10 PINS	DRC (VSON) 10 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance (standard board)	67.4	45.2	°C/W
$R_{\theta JA}$	Junction-to-ambient thermal resistance (custom board)[(3)]	—	61.5	
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	46.7	52.1	
$R_{\theta JB}$	Junction-to-board thermal resistance	38.4	20.6	
ψ_{JT}	Junction-to-top characterization parameter	1.9	0.9	
ψ_{JB}	Junction-to-board characterization parameter	38.1	20.8	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	15.9	5.2	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) Power rating at a specific ambient temperature T_A should be determined with a junction temperature of 150°C. This is the point where distortion starts to substantially increase. See power dissipation estimate in application section of this data sheet for more information.
(3) Test boards conditions:
(a) 3 inches x 3 inches, 2 layers, thickness: 0.062 inch
(b) 2 oz. copper traces located on the top of the PCB
(c) 2 oz. copper ground plane, bottom layer
(d) 6 thermal vias (13mil) located under the device package

7.5 Electrical Characteristics

T_J = –40°C to 150°C, VIN = 3.5 V to 60 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE (VIN PIN)					
Operating input voltage		3.5		60	V
Internal undervoltage lockout threshold	No voltage hysteresis, rising and falling		2.5		V
Shutdown supply current	EN = 0 V, 25°C, 3.5 V ≤ V_{IN} ≤ 60 V		1.5	4	µA
	EN = 0 V, 125°C, 3.5 V ≤ V_{IN} ≤ 60 V		1.9	6.5	µA
Operating nonswitching supply current	VSENSE = 0.83 V, VIN = 12 V, T_J = 25°C		116	136	µA
ENABLE AND UVLO (EN PIN)					
Enable threshold voltage	No voltage hysteresis, rising and falling, T_J = 25°C	1.15	1.25	1.36	V
Input current	Enable threshold +50 mV		–3.8		µA
	Enable threshold –50 mV		–0.9		µA
Hysteresis current			–2.9		µA
VOLTAGE REFERENCE					
Voltage reference		0.792	0.8	0.808	V
HIGH-SIDE MOSFET					
On-resistance	VIN = 3.5 V, BOOT-PH = 3 V		300		mΩ
	VIN = 12 V, BOOT-PH = 6 V		200	410	mΩ
ERROR AMPLIFIER					
Input current			50		nA
Error amplifier transconductance (g_M)	–2 µA < I_{COMP} < 2 µA, V_{COMP} = 1 V		97		µMhos
Error amplifier transconductance (g_M) during slow start	–2 µA < I_{COMP} < 2 µA, V_{COMP} = 1 V, V_{VSENSE} = 0.4 V		26		µMhos
Error amplifier dc gain	V_{VSENSE} = 0.8 V		10,000		V/V
Error amplifier bandwidth			2700		kHz
Error amplifier source/sink	$V_{(COMP)}$ = 1 V, 100-mV overdrive		±7		µA
COMP to switch current transconductance			6		A/V

Electrical Characteristics (continued)

T_J = –40°C to 150°C, VIN = 3.5 V to 60 V (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
CURRENT LIMIT						
	Current limit threshold	VIN = 12 V, T_J = 25°C	1.8	2.7		A
THERMAL SHUTDOWN						
	Thermal shutdown			182		°C
TIMING RESISTOR AND EXTERNAL CLOCK (RT/CLK PIN)						
	Switching frequency range using RT mode	VIN = 12 V	100		2500	kHz
f_{SW}	Switching frequency	VIN = 12 V, R_T = 200 kΩ	450	581	720	kHz
	Switching frequency range using CLK mode	VIN = 12 V	300		2200	kHz
	Minimum CLK input pulse width			40		ns
	RT/CLK high threshold	VIN = 12 V		1.9	2.2	V
	RT/CLK low threshold	VIN = 12 V	0.45	0.7		V
	RT/CLK falling edge to PH rising edge delay	Measured at 500 kHz with RT resistor in series		60		ns
	PLL lock in time	Measured at 500 kHz		100		μs
SLOW START AND TRACKING (SS/TR)						
	Charge current	$V_{SS/TR}$ = 0.4 V		2		μA
	SS/TR-to-VSENSE matching	$V_{SS/TR}$ = 0.4 V		45		mV
	SS/TR-to-reference crossover	98% nominal		1		V
	SS/TR discharge current (overload)	VSENSE = 0 V, V(SS/TR) = 0.4 V		112		μA
	SS/TR discharge voltage	VSENSE = 0 V		54		mV
POWER-GOOD (PWRGD PIN)						
V_{VSENSE}	VSENSE threshold	VSENSE falling (Fault)		92%		
		VSENSE rising (Good)		94%		
		VSENSE rising (Fault)		109%		
		VSENSE falling (Good)		107%		
	Hysteresis	VSENSE falling		2%		
	Output high leakage	VSENSE = VREF, V(PWRGD) = 5.5 V, T_J = 25°C		10		nA
	On resistance	I(PWRGD) = 3 mA, VSENSE < 0.79 V		50		Ω
	Minimum VIN for defined output	V(PWRGD) < 0.5 V, II(PWRGD) = 100 μA		0.95	1.5	V

7.6 Typical Characteristics

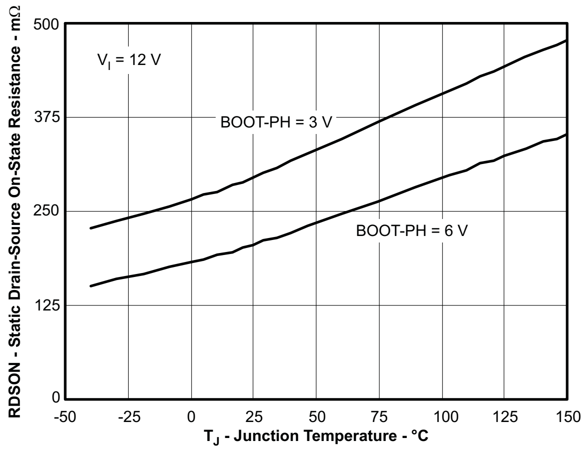


Figure 1. ON Resistance vs Junction Temperature

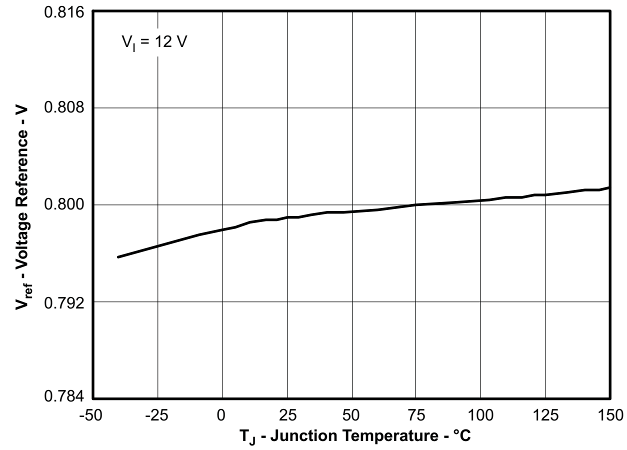


Figure 2. Voltage Reference vs Junction Temperature

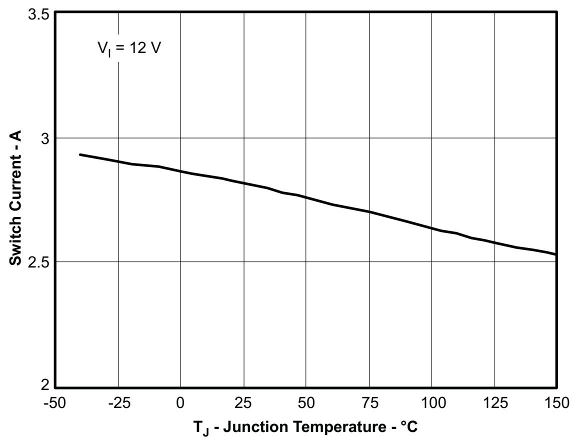


Figure 3. Switch Current Limit vs Junction Temperature

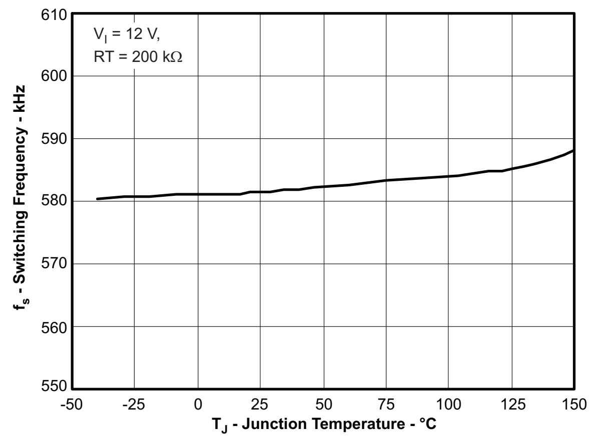


Figure 4. Switching Frequency vs Junction Temperature

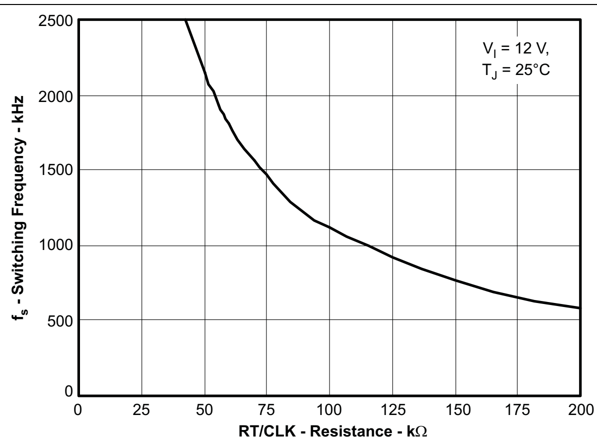


Figure 5. Switching Frequency vs RT/CLK Resistance, High Frequency Range

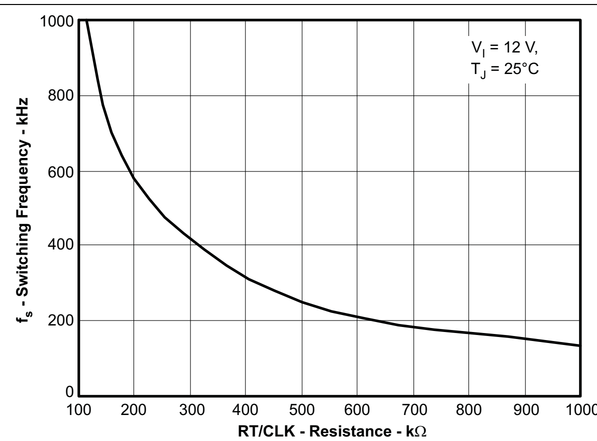


Figure 6. Switching Frequency vs RT/CLK Resistance, Low Frequency Range

Typical Characteristics (continued)

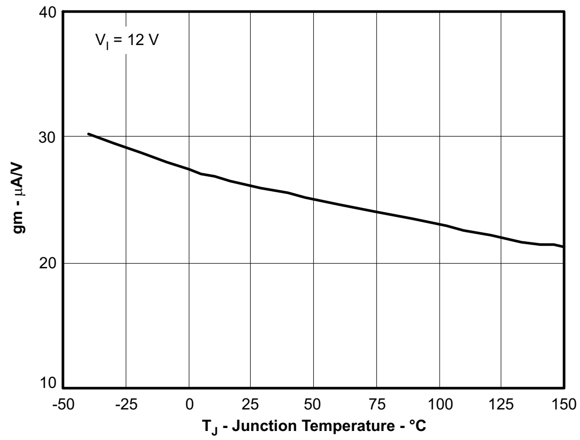


Figure 7. EA Transconductance During Slow Start vs Junction Temperature

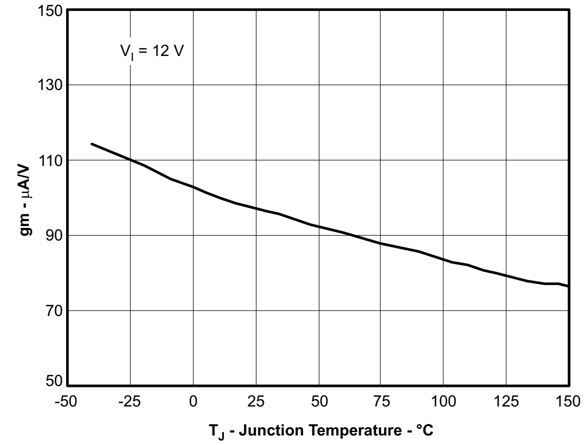


Figure 8. EA Transconductance vs Junction Temperature

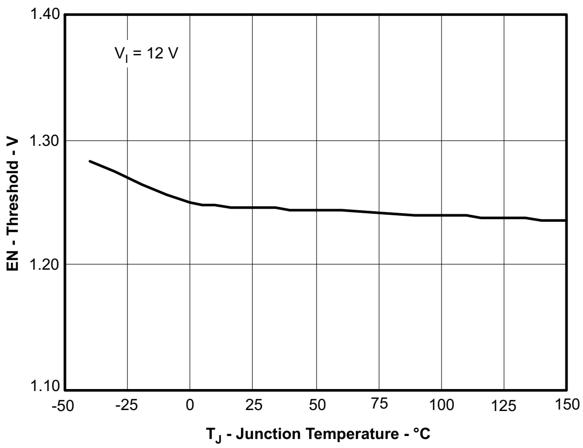


Figure 9. EN Pin Voltage vs Junction Temperature

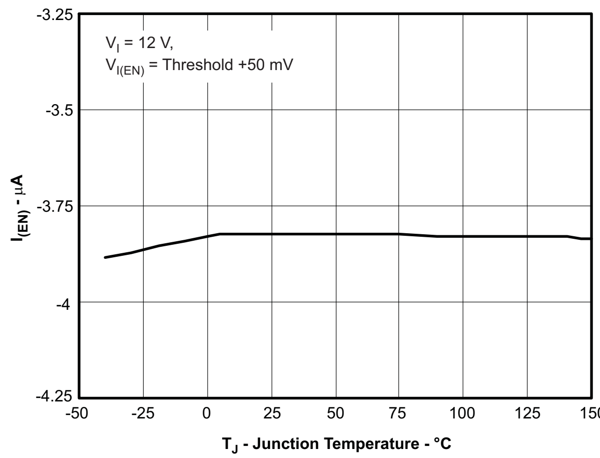


Figure 10. EN Pin Current vs Junction Temperature

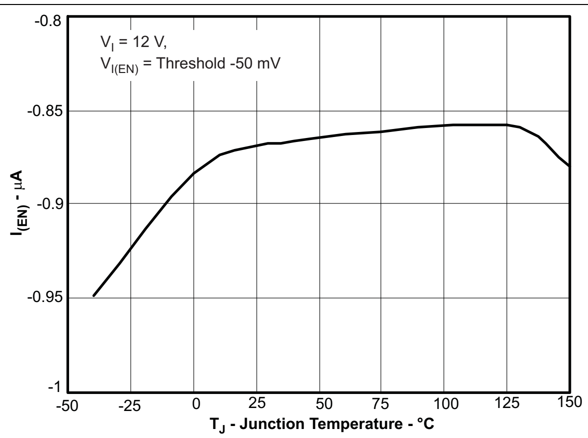


Figure 11. EN Pin Current vs Junction Temperature

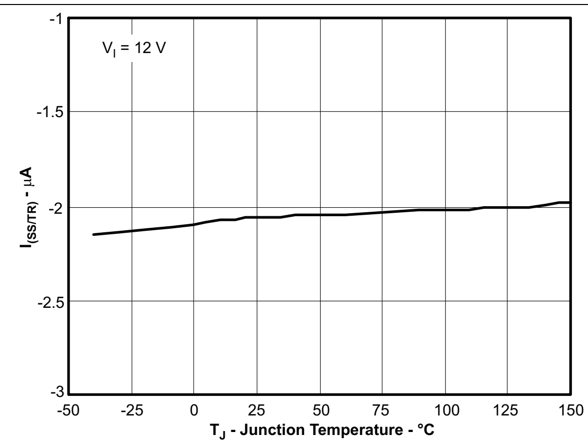


Figure 12. SS/TR Charge Current vs Junction Temperature

Typical Characteristics (continued)

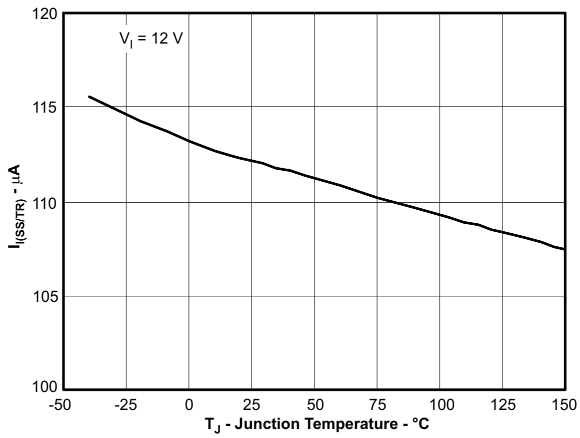


Figure 13. SS/TR Discharge Current vs Junction Temperature

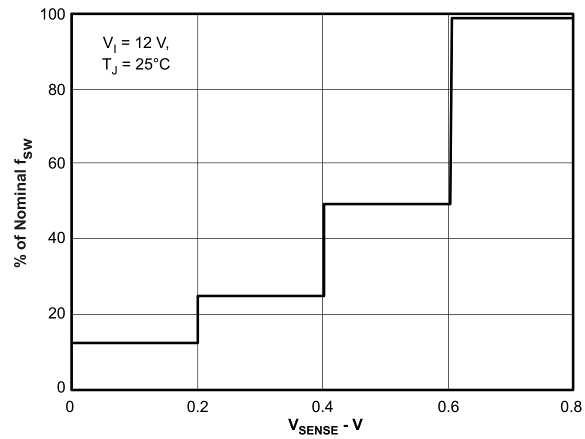


Figure 14. Switching Frequency vs VSENSE

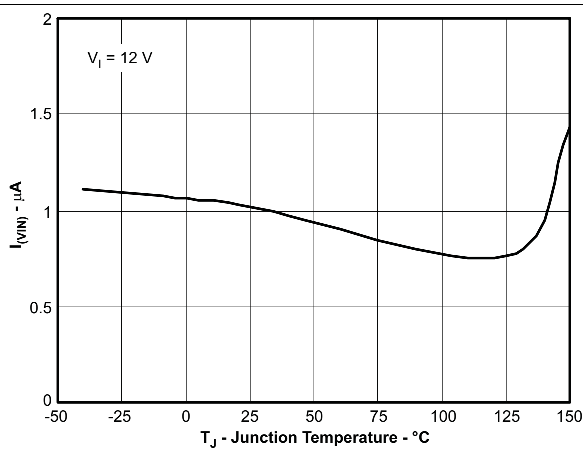


Figure 15. Shutdown Supply Current vs Junction Temperature

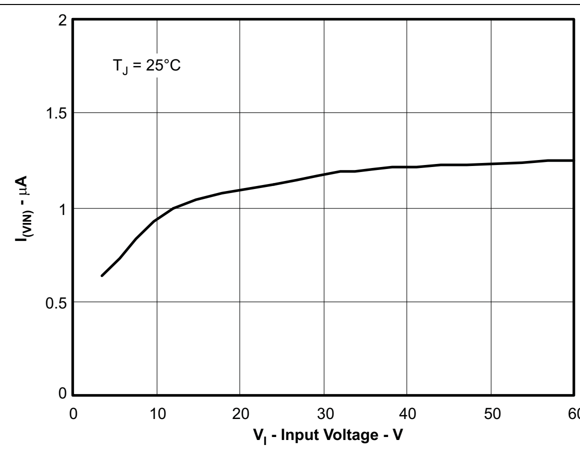


Figure 16. Shutdown Supply Current vs Input Voltage (V_{IN})

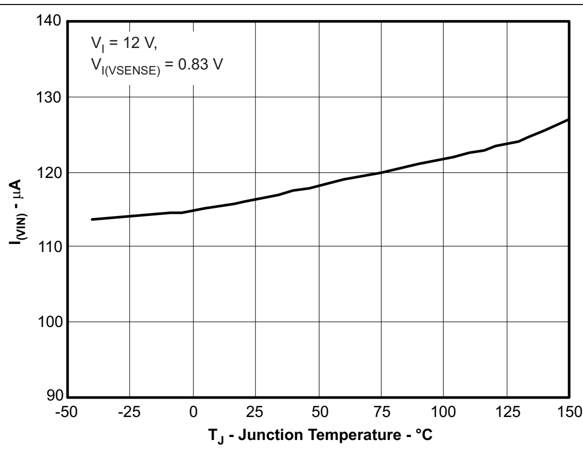


Figure 17. VIN Supply Current vs Junction Temperature

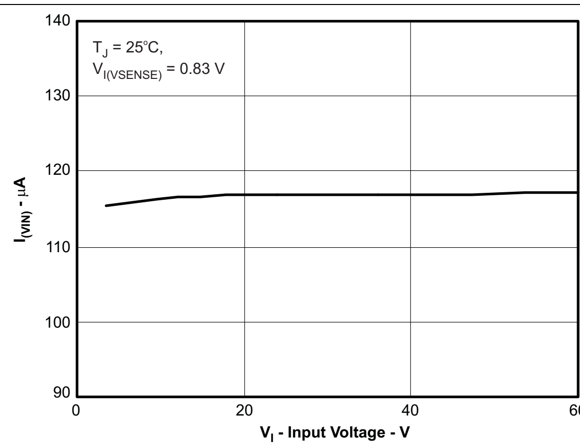


Figure 18. VIN Supply Current vs Input Voltage

Typical Characteristics (continued)

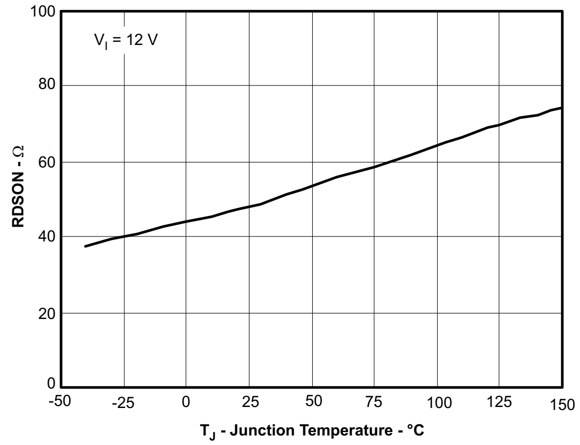


Figure 19. PWRGD ON Resistance vs Junction Temperature

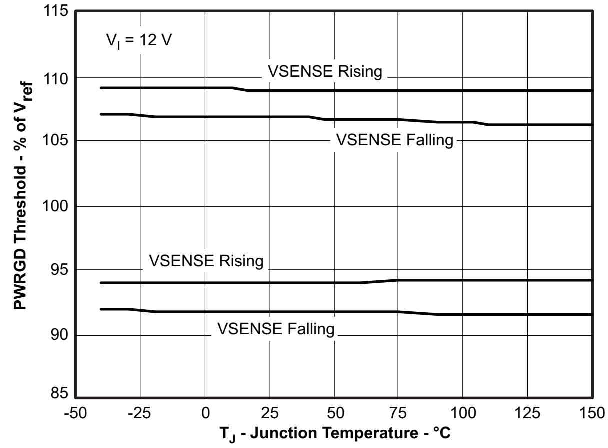


Figure 20. PWRGD Threshold vs Junction Temperature

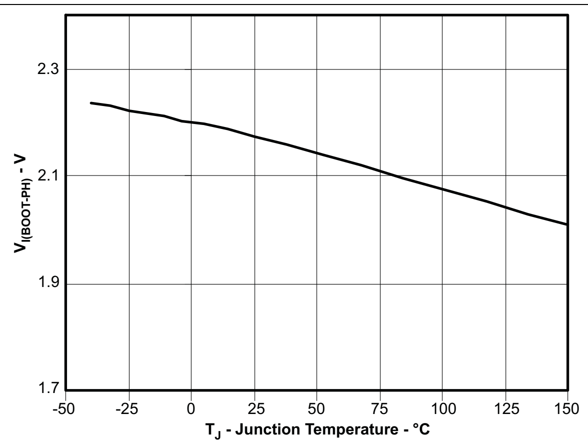


Figure 21. BOOT-PH UVLO vs Junction Temperature

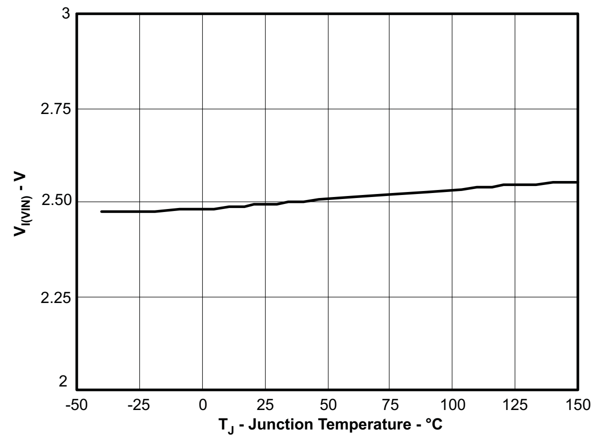


Figure 22. Input Voltage (UVLO) vs Junction Temperature

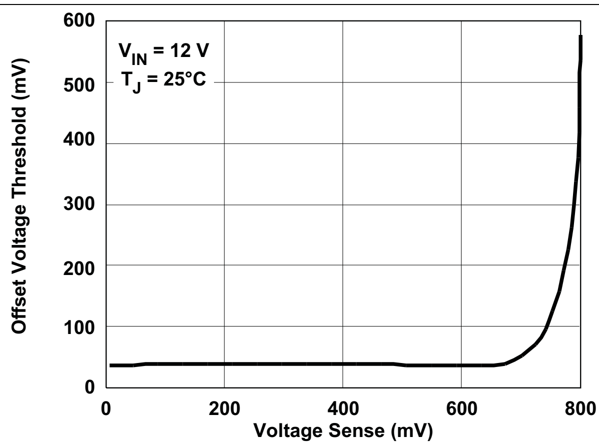


Figure 23. SS/TR to VSENSE Offset vs VSENSE

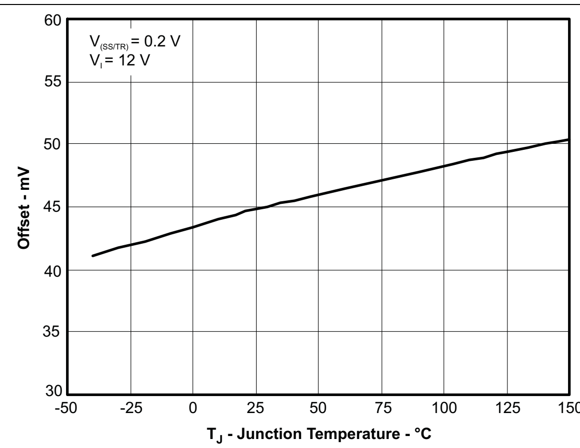


Figure 24. SS/TR to VSENSE Offset vs Temperature

8 Detailed Description

8.1 Overview

The TPS57160-Q1 device is a 60-V 1.5-A step-down (buck) regulator with an integrated high-side n-channel MOSFET. To improve performance during line and load transients the device implements a constant frequency, current mode control which reduces output capacitance and simplifies external frequency compensation design. The wide switching frequency of 100 kHz to 2500 kHz allows for efficiency and size optimization when selecting the output filter components. The switching frequency is adjusted using a resistor to ground on the RT/CLK pin. The device has an internal phase lock loop (PLL) on the RT/CLK pin that is used to synchronize the power switch turn on to a falling edge of an external system clock.

The TPS57160-Q1 has a default start up voltage of approximately 2.5 V. The EN pin has an internal pullup current source that can be used to adjust the input voltage undervoltage lockout (UVLO) threshold with two external resistors. In addition, the pullup current provides a default condition. When the EN pin is floating, the device can operate. The operating current is 116 μA when not switching and under no load. When the device is disabled, the supply current is 1.5 μA.

The integrated 200-mΩ high-side MOSFET allows for high efficiency power supply designs capable of delivering 1.5-A continuous current to a load. The TPS57160-Q1 reduces the external component count by integrating the boot recharge diode. The bias voltage for the integrated high-side MOSFET is supplied by a capacitor on the BOOT to PH pin. The boot capacitor voltage is monitored by an UVLO circuit and turns off the high-side MOSFET when the boot voltage falls below a preset threshold. The TPS57160-Q1 can operate at high duty cycles because of the boot UVLO. The output voltage can be stepped down to as low as the 0.8-V reference.

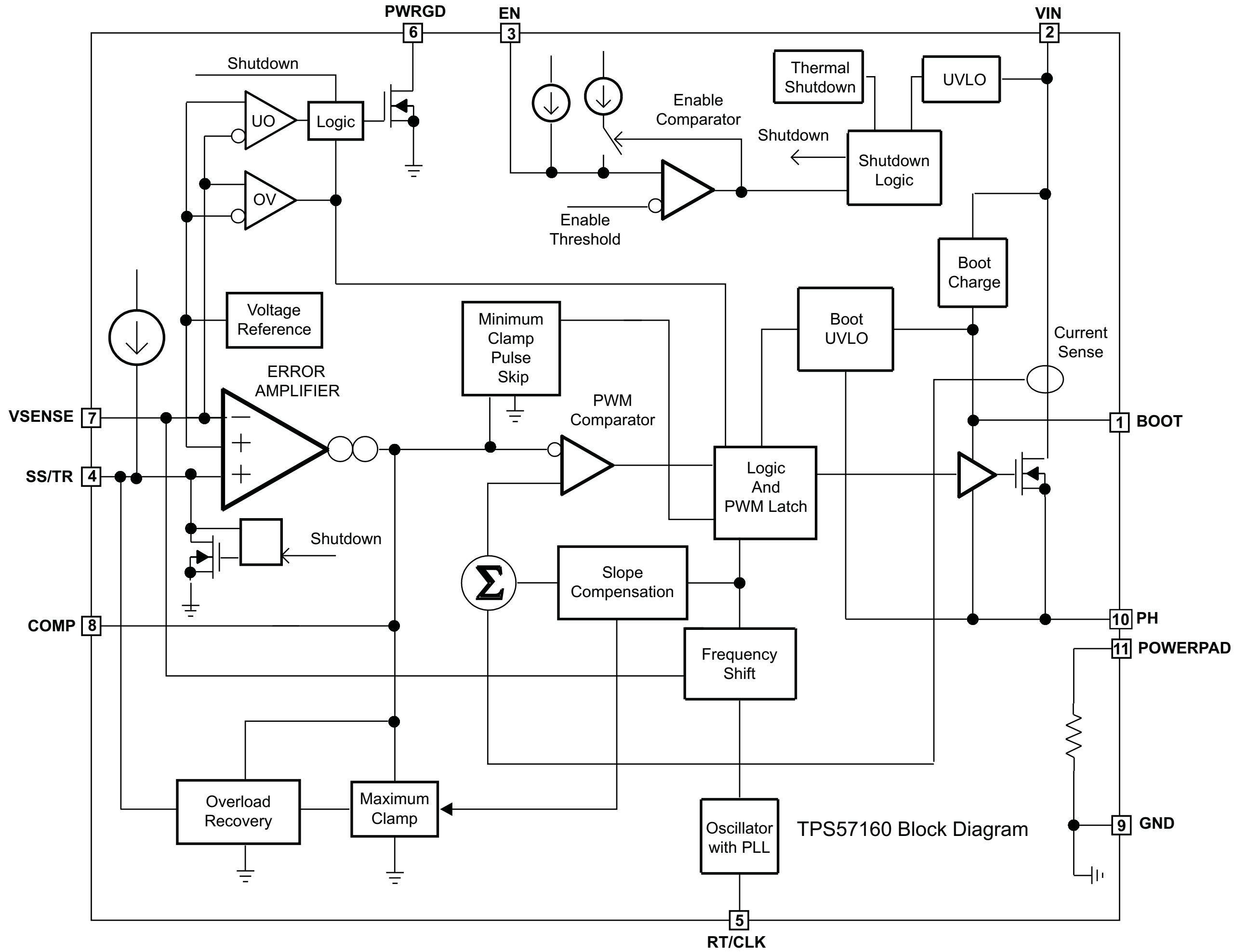
The TPS57160-Q1 has a power-good comparator (PWRGD) which asserts when the regulated output voltage is less than 92% or greater than 109% of the nominal output voltage. The PWRGD pin is an open drain output which de-asserts when the VSENSE pin voltage is between 94% and 107% of the nominal output voltage allowing the pin to transition high when a pullup resistor is used.

The TPS57160-Q1 minimizes excessive output overvoltage (OV) transients by taking advantage of the OV power-good comparator. When the OV comparator is activated, the high-side MOSFET is turned off and masked from turning on until the output voltage is lower than 107%.

The SS/TR (slow start/tracking) pin is used to minimize inrush currents or provide power supply sequencing during power up. A small value capacitor should be coupled to the pin to adjust the slow start time. A resistor divider can be coupled to the pin for critical power supply sequencing requirements. The SS/TR pin is discharged before the output powers up. This discharging ensures a repeatable restart after an over-temperature fault, UVLO fault or a disabled condition.

The TPS57160-Q1, also, discharges the slow-start capacitor during overload conditions with an overload recovery circuit. The overload recovery circuit slow starts the output from the fault voltage to the nominal regulation voltage once a fault condition is removed. A frequency foldback circuit reduces the switching frequency during startup and overcurrent fault conditions to help control the inductor current.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Fixed Frequency PWM Control

The TPS57160-Q1 uses an adjustable fixed frequency, peak current mode control. The output voltage is compared through external resistors on the VSENSE pin to an internal voltage reference by an error amplifier which drives the COMP pin. An internal oscillator initiates the turn on of the high-side power switch. The error amplifier output is compared to the high-side power switch current. When the power switch current reaches the level set by the COMP voltage, the power switch is turned off. The COMP pin voltage increases and decreases as the output current increases and decreases. The device implements a current limit by clamping the COMP pin voltage to a maximum level. The Eco-mode is implemented with a minimum clamp on the COMP pin.

8.3.2 Slope Compensation Output Current

The TPS57160-Q1 adds a compensating ramp to the switch current signal. This slope compensation prevents sub-harmonic oscillations. The available peak inductor current remains constant over the full duty cycle range.

8.3.3 Low Dropout Operation and Bootstrap Voltage (BOOT)

The TPS57160-Q1 has an integrated boot regulator, and requires a small ceramic capacitor between the BOOT and PH pins to provide the gate drive voltage for the high-side MOSFET. The BOOT capacitor is refreshed when the high-side MOSFET is off and the low side diode conducts. The value of this ceramic capacitor should be 0.1 µF. A ceramic capacitor with an X7R or X5R grade dielectric with a voltage rating of 10 V or higher is recommended because of the stable characteristics overtemperature and voltage.

Feature Description (continued)

To improve drop out, the TPS57160-Q1 is designed to operate at 100% duty cycle as long as the BOOT to PH pin voltage is greater than 2.1 V. When the voltage from BOOT to PH drops below 2.1 V, the high-side MOSFET is turned off using an UVLO circuit which allows the low side diode to conduct and refresh the charge on the BOOT capacitor. Because the supply current sourced from the BOOT capacitor is low, the high-side MOSFET can remain on for more switching cycles than are required to refresh the capacitor, thus the effective duty cycle of the switching regulator is high.

The effective duty cycle during dropout of the regulator is mainly influenced by the voltage drops across the power MOSFET, inductor resistance, low side diode and printed circuit board resistance. During operating conditions in which the input voltage drops and the regulator is operating in continuous conduction mode, the high-side MOSFET can remain on for 100% of the duty cycle to maintain output regulation, until the BOOT to PH voltage falls below 2.1 V.

Attention must be taken in maximum duty cycle applications which experience extended time periods with light loads or no load. When the voltage across the BOOT capacitor falls below the 2.1-V UVLO threshold, the high-side MOSFET is turned off, but there may not be enough inductor current to pull the PH pin down to recharge the BOOT capacitor. The high-side MOSFET of the regulator stops switching because the voltage across the BOOT capacitor is less than 2.1 V. The output capacitor then decays until the difference in the input voltage and output voltage is greater than 2.1 V, at which point the BOOT UVLO threshold is exceeded, and the device starts switching again until the desired output voltage is reached. This operating condition persists until the input voltage and/or the load current increases. It is recommended to adjust the VIN stop voltage greater than the BOOT UVLO trigger condition at the minimum load of the application using the adjustable VIN UVLO feature with resistors on the EN pin.

The start and stop voltages for typical 3.3-V and 5-V output applications are shown in Figure 25 and Figure 26. The voltages are plotted versus load current. The start voltage is defined as the input voltage needed to regulate the output within 1%. The stop voltage is defined as the input voltage at which the output drops by 5% or stops switching.

During high duty cycle conditions, the inductor current ripple increases while the BOOT capacitor is being recharged resulting in an increase in ripple voltage on the output. This is due to the recharge time of the boot capacitor being longer than the typical high-side off time when switching occurs every cycle.

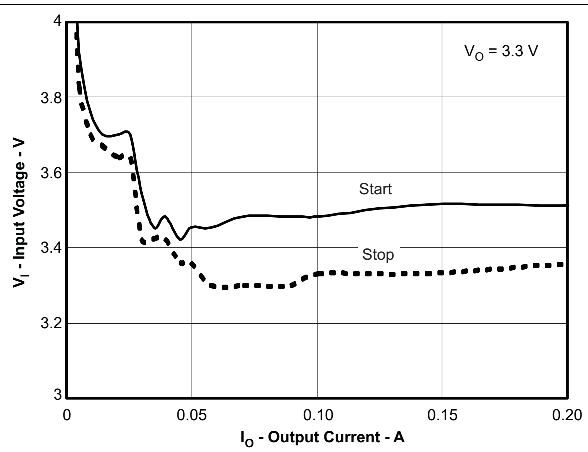


Figure 25. 3.3-V Start/Stop Voltage

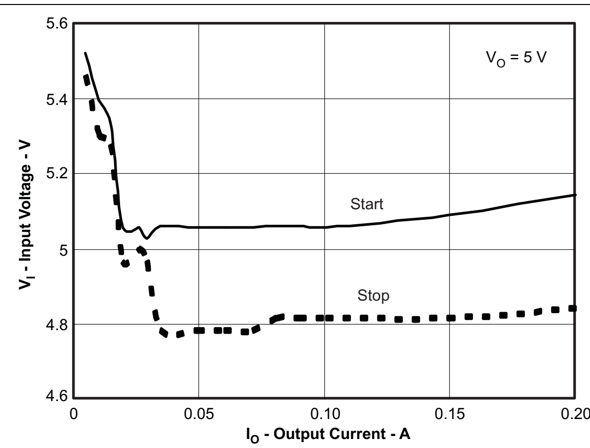


Figure 26. 5-V Start/Stop Voltage

Feature Description (continued)

8.3.4 Error Amplifier

The TPS57160-Q1 has a transconductance amplifier for the error amplifier. The error amplifier compares the VSENSE voltage to the lower of the SS/TR pin voltage or the internal 0.8-V voltage reference. The transconductance (gm) of the error amplifier is 97 μA/V during normal operation. During the slow start operation, the transconductance is a fraction of the normal operating gm. When the voltage of the VSENSE pin is below 0.8 V and the device is regulating using the SS/TR voltage, the gm is 25 μA/V.

The frequency compensation components (capacitor, series resistor and capacitor) are added from the COMP pin to ground.

8.3.5 Voltage Reference

The voltage reference system produces a precise ±2% voltage reference over temperature by scaling the output of a temperature stable bandgap circuit.

8.3.6 Adjusting the Output Voltage

The output voltage is set with a resistor divider from the output node to the VSENSE pin. It is recommended to use 1% tolerance or better divider resistors. Start with a 10 kΩ for the R2 resistor and use the Equation 1 to calculate R1. To improve efficiency at light loads consider using larger value resistors. If the values are too high, the regulator is more susceptible to noise, and voltage errors from the VSENSE input current are noticeable

$$R1 = R2 \times \left(\frac{V_{OUT} - 0.8\ V}{0.8\ V} \right) \quad (1)$$

8.3.7 Enable and Adjusting Undervoltage Lockout

The TPS57160-Q1 is disabled when the VIN pin voltage falls below 2.5 V. If an application requires a higher undervoltage lockout (UVLO), use the EN pin as shown in Figure 27 to adjust the input voltage UVLO by using the two external resistors. Though it is not necessary to use the UVLO adjust resistors, for operation it is highly recommended to provide consistent power up behavior. The EN pin has an internal pullup current source, I1, of 0.9 μA that provides the default condition of the TPS57160-Q1 operating when the EN pin floats. Once the EN pin voltage exceeds 1.25 V, an additional 2.9 μA of hysteresis, I_{HYS}, is added. This additional current facilitates input voltage hysteresis. Use Equation 2 to set the external hysteresis for the input voltage. Use Equation 3 to set the input start voltage.

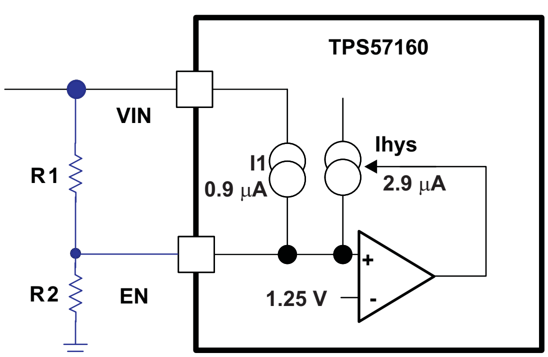


Figure 27. Adjustable Undervoltage Lockout (UVLO)

$$R1 = \frac{V_{START} - V_{STOP}}{I_{HYS}} \quad (2)$$

$$R2 = \frac{V_{ENA}}{\frac{V_{START} - V_{ENA}}{R1} + I_1} \quad (3)$$

Feature Description (continued)

Another technique to add input voltage hysteresis is shown in Figure 28. This method may be used, if the resistance values are high from the previous method and a wider voltage hysteresis is needed. The resistor R3 sources additional hysteresis current into the EN pin.

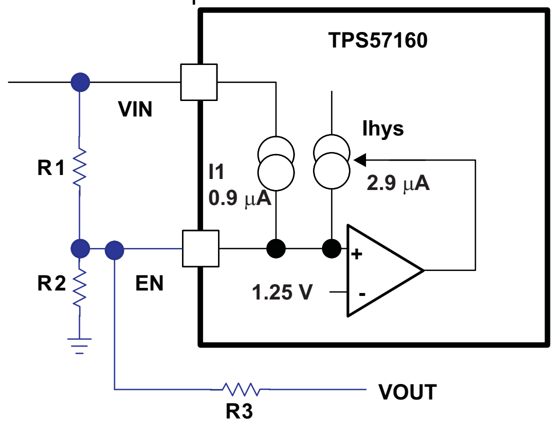


Figure 28. Adding Additional Hysteresis

$$R1 = \frac{V_{START} - V_{STOP}}{I_{HYS} + \frac{V_{OUT}}{R3}} \quad (4)$$

$$R2 = \frac{V_{ENA}}{\frac{V_{START} - V_{ENA}}{R1} + I_1 - \frac{V_{ENA}}{R3}} \quad (5)$$

Do not place a low-impedance voltage source with greater than 5 V directly on the EN pin. Do not place a capacitor directly on the EN pin if V_{EN} > 5 V when using a voltage divider to adjust the start and stop voltage. The node voltage, (see Figure 29) must remain equal to or less than 5.8 V. The zener diode can sink up to 100 µA. The EN pin voltage can be greater than 5 V if the V_{IN} voltage source has a high impedance and does not source more than 100 µA into the EN pin.

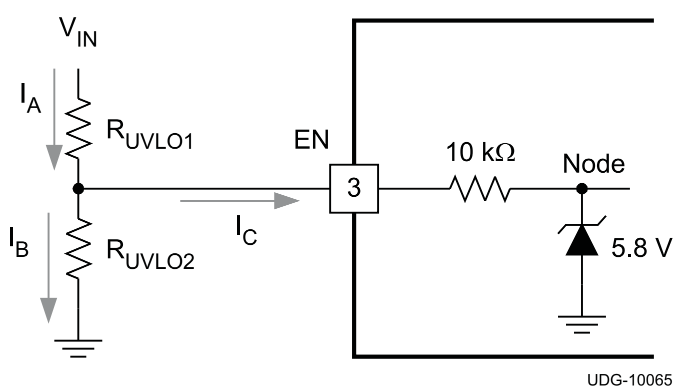


Figure 29. Node Voltage

Feature Description (continued)

8.3.8 Slow Start/Tracking Pin (SS/TR)

The TPS57160-Q1 device effectively uses the lower voltage of the internal voltage reference or the SS/TR pin voltage as the power-supply's reference voltage and regulates the output accordingly. A capacitor on the SS/TR pin to ground implements a slow start time. The TPS57160-Q1 has an internal pullup current source of 2 μA that charges the external slow-start capacitor. The calculations for the slow start time (10% to 90%) are shown in Equation 6. The voltage reference (V_{REF}) is 0.8 V and the slow start current (I_{SS}) is 2 μA. The slow-start capacitor should remain lower than 0.47 μF and greater than 0.47 nF.

$$C_{SS}\ (nF) = \frac{T_{SS}\ (ms) \times I_{SS}\ (\mu A)}{V_{REF}\ (V) \times 0.8} \tag{6}$$

At power up, the TPS57160-Q1 device does not start switching until the slow start pin is discharged to less than 40 mV to ensure a proper power up, see Figure 30.

Also, during normal operation, the TPS57160-Q1 device stops switching and the SS/TR must be discharged to 40 mV when the VIN UVLO is exceeded, EN pin pulled below 1.25 V, or a thermal shutdown event occurs.

The VSENSE voltage follows the SS/TR pin voltage with a 45-mV offset up to 85% of the internal voltage reference. When the SS/TR voltage is greater than 85% on the internal reference voltage the offset increases as the effective system reference transitions from the SS/TR voltage to the internal voltage reference (see Figure 23). The SS/TR voltage ramps linearly until clamped at 1.7 V.

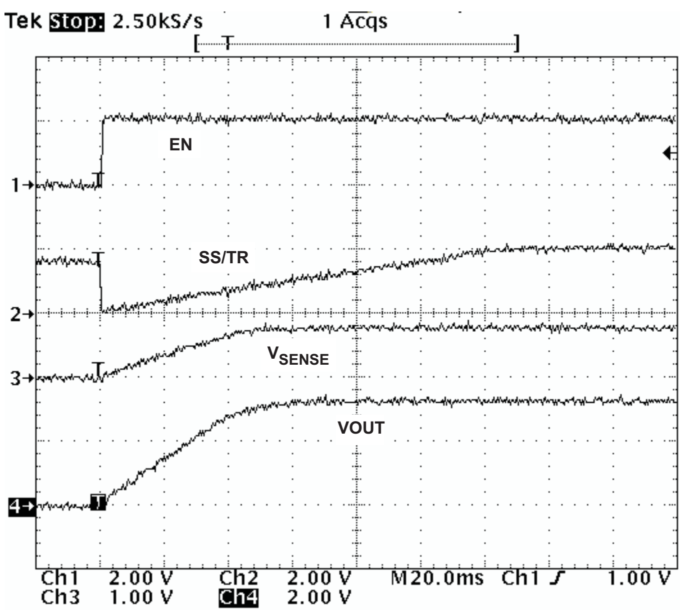


Figure 30. Operation of SS/TR Pin When Starting

8.3.9 Overload Recovery Circuit

The TPS57160-Q1 device has an overload recovery (OLR) circuit. The OLR circuit slow starts the output from the overload voltage to the nominal regulation voltage once the fault condition is removed. The OLR circuit discharges the SS/TR pin to a voltage slightly greater than the VSENSE pin voltage using an internal pulldown of 100 μA when the error amplifier is changed to a high voltage from a fault condition. When the fault condition is removed, the output slow starts from the fault voltage to nominal output voltage.

Feature Description (continued)

8.3.10 Constant Switching Frequency and Timing Resistor (RT/CLK Pin)

The switching frequency of the TPS57160-Q1 is adjustable over a wide range from approximately 100 kHz to 2500 kHz by placing a resistor on the RT/CLK pin. The RT/CLK pin voltage is typically 0.5 V and must have a resistor to ground to set the switching frequency. To determine the timing resistance for a given switching frequency, use Equation 7 or the curves in Figure 31 or Figure 32. To reduce the solution size one would typically set the switching frequency as high as possible, but tradeoffs of the supply efficiency, maximum input voltage and minimum controllable on time should be considered.

The minimum controllable on time is typically 130 ns and limits the maximum operating input voltage.

The maximum switching frequency is also limited by the frequency shift circuit. More discussion on the details of the maximum switching frequency is located below.

$$R_T\ (k\Omega) = \frac{206033}{f_{SW}\ (kHz)^{1.0888}} \tag{7}$$

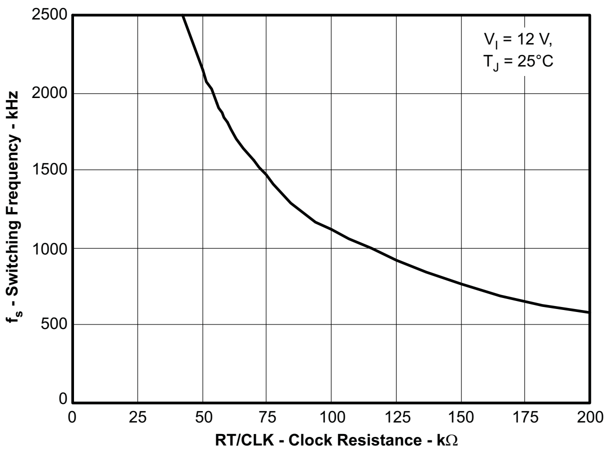


Figure 31. High Range RT

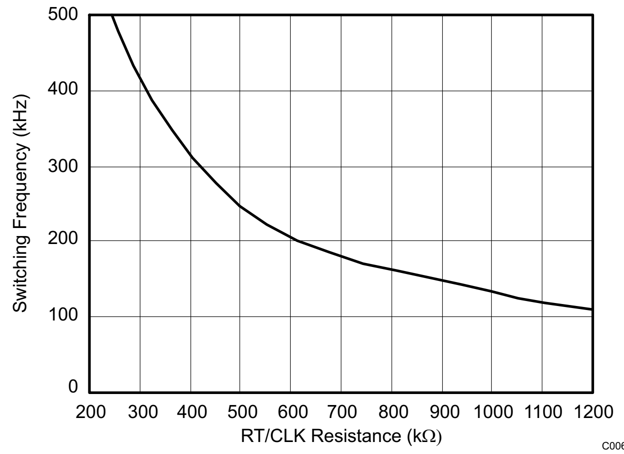


Figure 32. Low Range RT

8.3.11 Overcurrent Protection and Frequency Shift

The TPS57160-Q1 implements current mode control, which uses the COMP pin voltage to turn off the high-side MOSFET on a cycle by cycle basis. Each cycle the switch current and COMP pin voltage are compared, when the peak switch current intersects the COMP voltage, the high-side switch is turned off. During overcurrent conditions that pull the output voltage low, the error amplifier responds by driving the COMP pin high, increasing the switch current. The error amplifier output is clamped internally, which functions as a switch current limit.

To increase the maximum operating switching frequency at high input voltages the TPS57160-Q1 implements a frequency shift. The switching frequency is divided by 8, 4, 2, and 1 as the voltage ramps from 0 V to 0.8 V on the VSENSE pin.

The device implements a digital frequency shift to enable synchronizing to an external clock during normal startup and fault conditions. Because the device can divide the switching frequency only by 8, there is a maximum input voltage limit at which the device operates and can maintain frequency shift protection.

During short-circuit events (particularly with high input voltage applications), the control loop has a finite minimum controllable on time and the output has a low voltage. During the switch-on time, the inductor current ramps to the peak current limit because of the high input voltage and minimum on time. During the switch-off time, the inductor would normally not have enough off time and output voltage for the inductor to ramp down by the ramp up amount. The frequency shift effectively increases the off time, allowing the current to ramp down.

Feature Description (continued)

8.3.12 Selecting the Switching Frequency

The switching frequency that is selected should be the lower value of the two equations, Equation 8 and Equation 9. Equation 8 is the maximum switching frequency limitation set by the minimum controllable on time. Setting the switching frequency above this value causes the regulator to skip switching pulses.

Equation 9 is the maximum switching frequency limit set by the frequency shift protection. To have adequate output short circuit protection at high input voltages, the switching frequency should be set to be less than the $f_{SW(maxshift)}$ frequency. In Equation 9, to calculate the maximum switching frequency one must take into account that the output voltage decreases from the nominal voltage to 0 volts, the f_{DIV} integer increases from 1 to 8 corresponding to the frequency shift.

In Figure 33, the solid line illustrates a typical safe operating area regarding frequency shift and assumes the output voltage is zero volts, and the resistance of the inductor is 0.1 Ω, FET on resistance of 0.2 Ω, and the diode voltage drop is 0.5 V. The dashed line is the maximum switching frequency to avoid pulse skipping. Enter these equations in a spreadsheet or other software or use the SwitcherPro design software to determine the switching frequency.

$$f_{SW(max\,skip)} = \frac{1}{t_{ON}} \times \left(\frac{I_L \times R_{dc} + V_{OUT} + V_d}{V_{IN} - I_L \times R_{DS(on)} + V_d} \right)$$

where

- t_{ON} is the controllable on time.
- I_L is the inductor current.
- R_{dc} is the inductor resistance.
- V_{OUT} is the output voltage.
- V_d is the diode voltage drop.
- V_{IN} is the maximum input voltage.
- $R_{DS(on)}$ is the switch on resistance. (8)

$$f_{SWshift} = \frac{f_{DIV}}{t_{ON}} \times \left(\frac{I_L \times R_{dc} + V_{OUT(sc)} + V_d}{V_{IN} - I_L \times R_{DS(on)} + V_d} \right)$$

where

- f_{DIV} is the frequency divide equals (1, 2, 4, or 8).
- $V_{OUT(SC)}$ is the output voltage during short. (9)

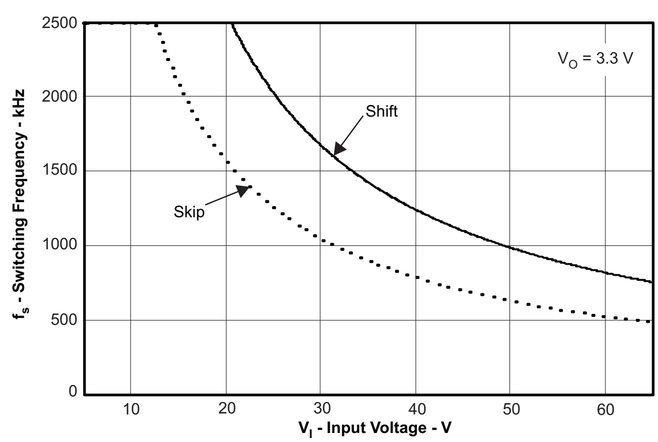


Figure 33. Maximum Switching Frequency vs Input Voltage

Feature Description (continued)

8.3.13 How to Interface to RT/CLK Pin

The RT/CLK pin can be used to synchronize the regulator to an external system clock. To implement the synchronization feature connect a square wave to the RT/CLK pin through the circuit network shown in Figure 34. The square wave amplitude must transition lower than 0.5 V and higher than 2.2 V on the RT/CLK pin and have an on time greater than 40 ns and an off time greater than 40 ns. The synchronization frequency range is 300 kHz to 2200 kHz. The rising edge of the PH is synchronized to the falling edge of RT/CLK pin signal. The external synchronization circuit should be designed in such a way that the device has the default frequency set resistor connected from the RT/CLK pin to ground should the synchronization signal turn off. It is recommended to use a frequency set resistor connected as shown in Figure 34 through a 50 Ω resistor to ground. The resistor should set the switching frequency close to the external CLK frequency. It is recommended to ac couple the synchronization signal through a 10-pF ceramic capacitor to RT/CLK pin and a 4-kΩ series resistor. The series resistor reduces PH jitter in heavy load applications when synchronizing to an external clock and in applications which transition from synchronizing to RT mode. The first time the CLK is pulled above the CLK threshold the device switches from the RT resistor frequency to PLL mode. The internal 0.5-V voltage source is removed and the CLK pin becomes high impedance as the PLL starts to lock onto the external signal. Because there is a PLL on the regulator the switching frequency can be higher or lower than the frequency set with the external resistor. The device transitions from the resistor mode to the PLL mode and then increases or decreases the switching frequency until the PLL locks onto the CLK frequency within 100 µs.

When the device transitions from the PLL to resistor mode the switching frequency slows down from the CLK frequency to 150 kHz, then reapply the 0.5-V voltage and the resistor then sets the switching frequency. The switching frequency is divided by 8, 4, 2, and 1 as the voltage ramps from 0 V to 0.8 V on VSENSE pin. The device implements a digital frequency shift to enable synchronizing to an external clock during normal startup and fault conditions. Figure 35, Figure 36 and Figure 37 show the device synchronized to an external system clock in continuous conduction mode (CCM) discontinuous conduction (DCM) and pulse skip mode (PSM).

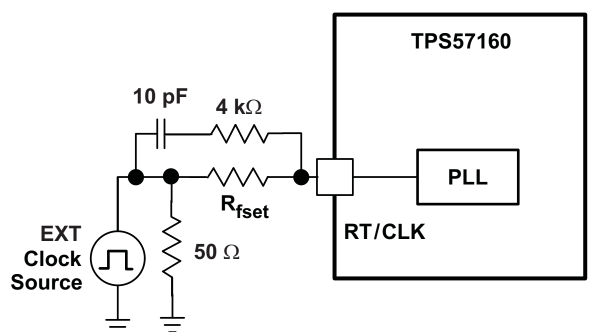


Figure 34. Synchronizing to a System Clock

Feature Description (continued)

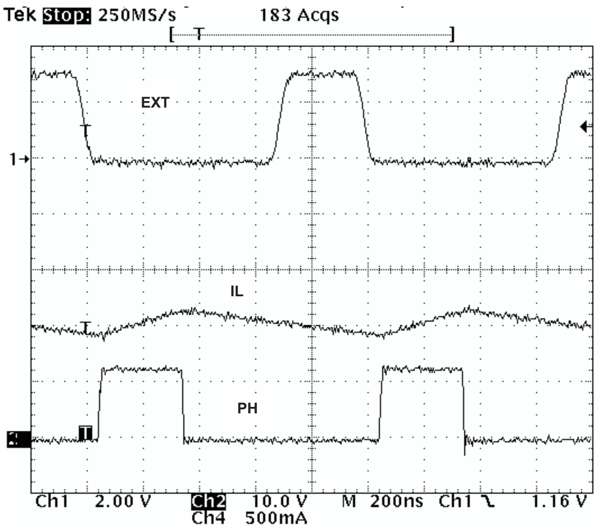


Figure 35. Plot of Synchronizing in CCM

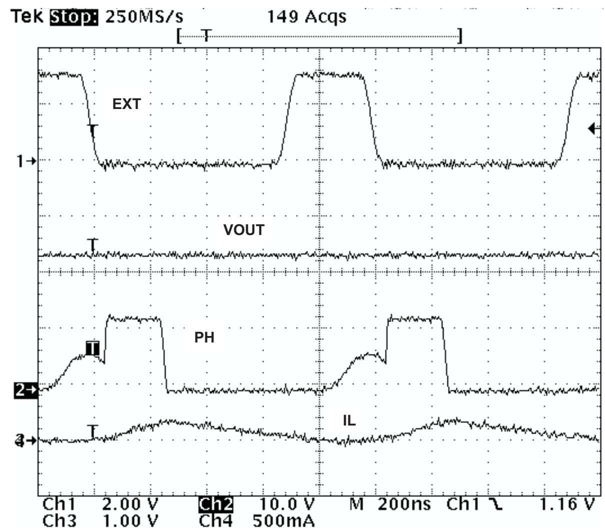


Figure 36. Plot of Synchronizing in DCM

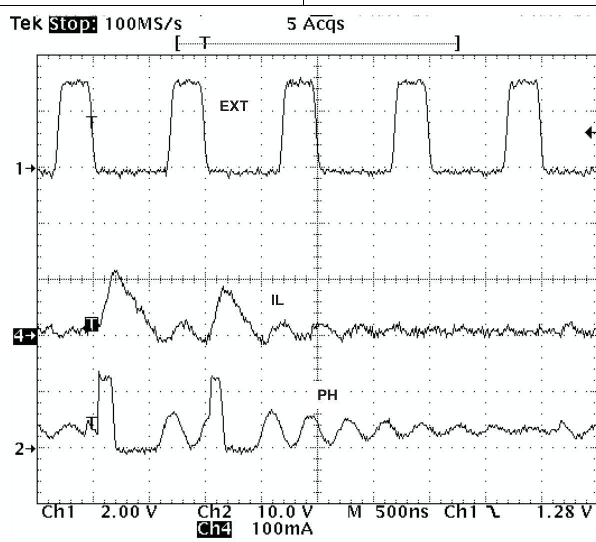


Figure 37. Plot of Synchronizing in PSM

8.3.14 Power-Good (PWRGD Pin)

The PWRGD pin is an open drain output. Once the VSENSE pin is between 94% and 107% of the internal voltage reference the PWRGD pin is de-asserted and the pin floats. It is recommended to use a pullup resistor between the values of 1 kΩ and 100 kΩ to a voltage source that is 5.5 V or less. The PWRGD is in a defined state once the V_{IN} input voltage is greater than 1.5 V but with reduced current sinking capability. PWRGD achieves full current sinking capability as V_{IN} input voltage approaches 3 V.

The PWRGD pin is pulled low when the VSENSE is lower than 92% or greater than 109% of the nominal internal reference voltage. Also, PWRGD is pulled low if the UVLO or thermal shutdown are asserted or EN is pulled low.

Feature Description (continued)

8.3.15 Overvoltage Transient Protection

The TPS57160-Q1 incorporates an overvoltage transient protection (OVTP) circuit to minimize voltage overshoot when recovering from output fault conditions or strong unload transients on power supply designs with low value output capacitance. For example, when the power supply output is overloaded the error amplifier compares the actual output voltage to the internal reference voltage. If the VSENSE pin voltage is lower than the internal reference voltage for a considerable time, the output of the error amplifier responds by clamping the error amplifier output to a high voltage. Thus, requesting the maximum output current. Once the condition is removed, the regulator output rises and the error amplifier output transitions to the steady state duty cycle. In some applications, the power supply output voltage can respond faster than the error amplifier output can respond, this actuality leads to the possibility of an output overshoot. The OVTP feature minimizes the output overshoot, when using a low value output capacitor, by implementing a circuit to compare the VSENSE pin voltage to OVTP threshold which is 109% of the internal voltage reference. If the VSENSE pin voltage is greater than the OVTP threshold, the high-side MOSFET is disabled preventing current from flowing to the output and minimizing output overshoot. When the VSENSE voltage drops lower than the OVTP threshold, the high-side MOSFET is allowed to turn on at the next clock cycle.

8.3.16 Thermal Shutdown

The device implements an internal thermal shutdown to protect itself if the junction temperature exceeds 182°C. The thermal shutdown forces the device to stop switching when the junction temperature exceeds the thermal trip threshold. Once the die temperature decreases below 182°C, the device reinitiates the power up sequence by discharging the SS/TR pin.

8.3.17 Small Signal Model for Loop Response

Figure 38 shows an equivalent model for the TPS57160-Q1 control loop which can be modeled in a circuit simulation program to check frequency response and dynamic load response. The error amplifier is a transconductance amplifier with a gm_{EA} of 97 μA/V. The error amplifier can be modeled using an ideal voltage controlled current source. The resistor R_o and capacitor C_o model the open loop gain and frequency response of the amplifier. The 1-mV ac voltage source between the nodes a and b effectively breaks the control loop for the frequency response measurements. Plotting c/a shows the small signal response of the frequency compensation. Plotting a/b shows the small signal response of the overall loop. The dynamic loop response can be checked by replacing R_L with a current source with the appropriate load step amplitude and step rate in a time domain analysis. This equivalent model is only valid for continuous conduction mode designs.

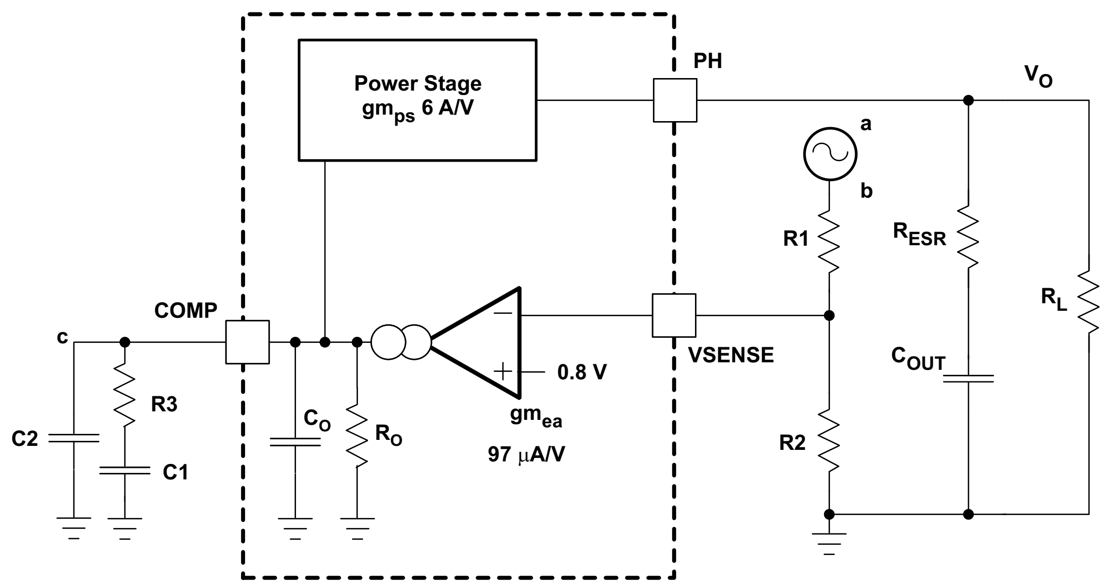


Figure 38. Small Signal Model for Loop Response

Feature Description (continued)

8.3.18 Simple Small Signal Model for Peak Current Mode Control

Figure 39 describes a simple small signal model that can be used to understand how to design the frequency compensation. The TPS57160-Q1 power stage can be approximated to a voltage-controlled current source (duty cycle modulator) supplying current to the output capacitor and load resistor. The control to output transfer function is shown in Equation 10 and consists of a dc gain, one dominant pole, and one ESR zero. The quotient of the change in switch current and the change in COMP pin voltage (node c in Figure 38) is the power stage transconductance. The gm_{PS} for the TPS57160-Q1 is 6 A/V. The low-frequency gain of the power stage frequency response is the product of the transconductance and the load resistance as shown in Equation 11.

As the load current increases and decreases, the low-frequency gain decreases and increases, respectively. This variation with the load may seem problematic at first glance, but fortunately the dominant pole moves with the load current (see Equation 12). The combined effect is highlighted by the dashed line in the right half of Figure 39. As the load current decreases, the gain increases and the pole frequency lowers, keeping the 0-dB crossover frequency the same for the varying load conditions which makes it easier to design the frequency compensation. The type of output capacitor chosen determines whether the ESR zero has a profound effect on the frequency compensation design. Using high ESR aluminum electrolytic capacitors may reduce the number frequency compensation components needed to stabilize the overall loop because the phase margin increases from the ESR zero at the lower frequencies (see Equation 13).

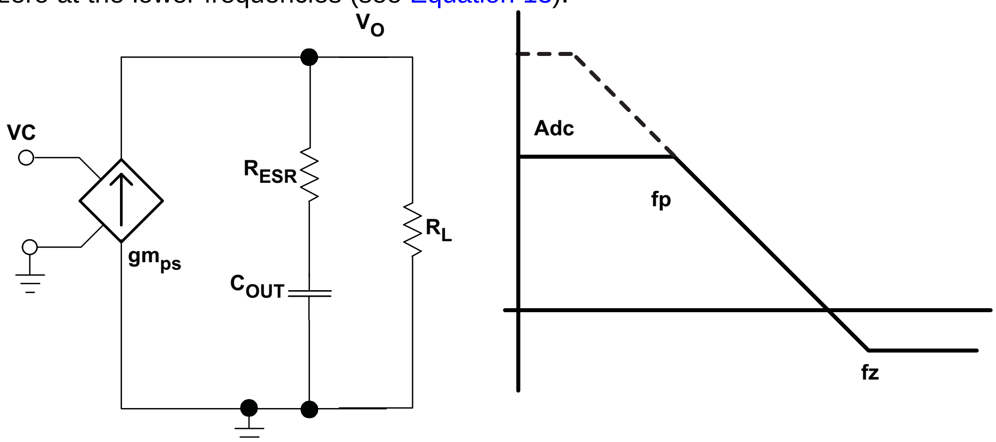


Figure 39. Simple Small Signal Model and Frequency Response for Peak Current Mode Control

$$\frac{V_{OUT}}{V_C} = Adc \times \frac{\left(1 + \frac{s}{2\pi \times f_Z}\right)}{\left(1 + \frac{s}{2\pi \times f_P}\right)} \tag{10}$$

$$Adc = gm_{ps} \times R_L \tag{11}$$

$$f_P = \frac{1}{C_{OUT} \times R_L \times 2\pi} \tag{12}$$

$$f_Z = \frac{1}{C_{OUT} \times R_{ESR} \times 2\pi} \tag{13}$$

8.3.19 Small Signal Model for Frequency Compensation

The TPS57160-Q1 uses a transconductance amplifier for the error amplifier and readily supports three of the commonly-used frequency compensation circuits. Compensation circuits Type 2A, Type 2B, and Type 1 are shown in Figure 40. Type 2 circuits most likely implemented in high bandwidth power-supply designs using low ESR output capacitors. The Type 1 circuit is used with power-supply designs with high-ESR aluminum electrolytic or tantalum capacitors.. Equation 14 and Equation 15 show how to relate the frequency response of the amplifier to the small signal model in Figure 40. The open-loop gain and bandwidth are modeled using the R_O and C_O shown in Figure 40. See the *Typical Application* section for a design example using a Type 2A network with a low ESR output capacitor.

Feature Description (continued)

Equation 14 through Equation 23 are provided as a reference for those who prefer to compensate using the preferred methods. Those who prefer to use prescribed method use the method outlined in the application section or use switched information.

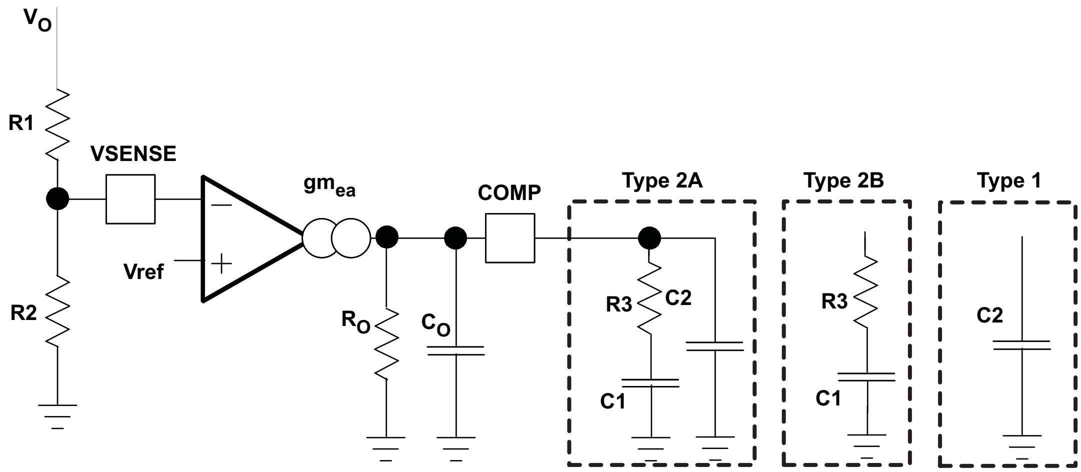


Figure 40. Types of Frequency Compensation

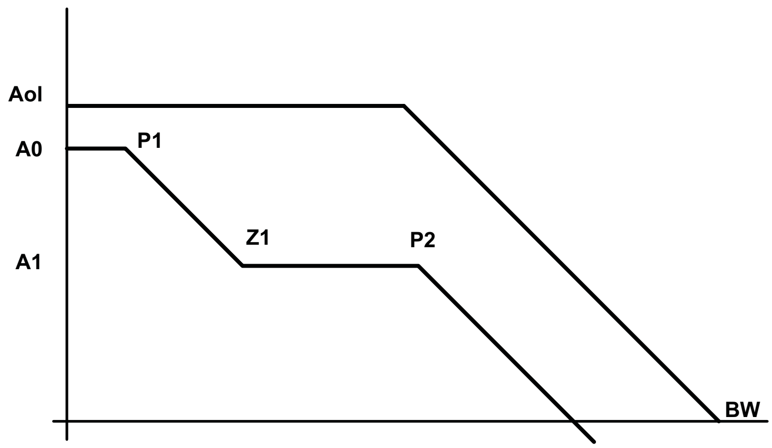


Figure 41. Frequency Response of the Type 2A and Type 2B Frequency Compensation

$$Ro = \frac{Aol(V/V)}{gm_{ea}} \tag{14}$$

$$C_{OUT} = \frac{gm_{ea}}{2\pi \times BW\ (Hz)} \tag{15}$$

$$EA = A0 \times \frac{\left(1 + \frac{s}{2\pi \times f_{Z1}}\right)}{\left(1 + \frac{s}{2\pi \times f_{P1}}\right) \times \left(1 + \frac{s}{2\pi \times f_{P2}}\right)} \tag{16}$$

$$A0 = gm_{ea} \times Ro \times \frac{R2}{R1 + R2} \tag{17}$$

$$A1 = gm_{ea} \times Ro|\,|R3 \times \frac{R2}{R1 + R2} \tag{18}$$

Feature Description (continued)

$$P1 = \frac{1}{2\pi \times Ro \times C1} \quad (19)$$

$$Z1 = \frac{1}{2\pi \times R3 \times C1} \quad (20)$$

$$P2 = \frac{1}{2\pi \times R3\,||\,R \times (C2 + C_{OUT})} \text{ type 2a} \quad (21)$$

$$P2 = \frac{1}{2\pi \times R3\,||\,R \times C_{OUT}} \text{ type 2b} \quad (22)$$

$$P2 = \frac{1}{2\pi \times R \times (C2 + C_{OUT})} \text{ type 1} \quad (23)$$

8.4 Device Functional Modes

8.4.1 Sequencing

Many of the common power supply sequencing methods can be implemented using the SS/TR, EN, and PWRGD pins. The sequential method can be implemented using an open drain output of a power-on reset pin of another device. The sequential method is illustrated in Figure 42 using two TPS57160-Q1 devices. The power-good is coupled to the EN pin on the TPS57160-Q1 device, which enables the second power supply once the primary supply reaches regulation. If needed, a 1-nF ceramic capacitor on the EN pin of the second power supply provide a 1-ms start-up delay. Figure 43 shows the results of Figure 42.

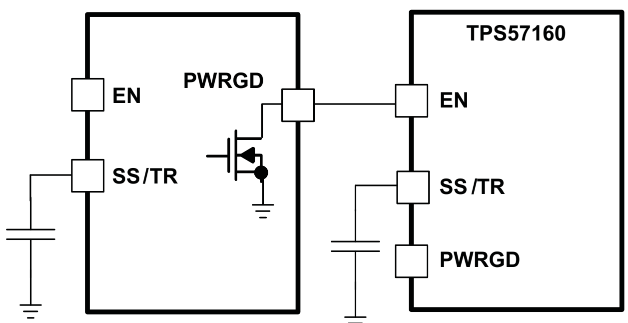


Figure 42. Schematic for Sequential Startup Sequence

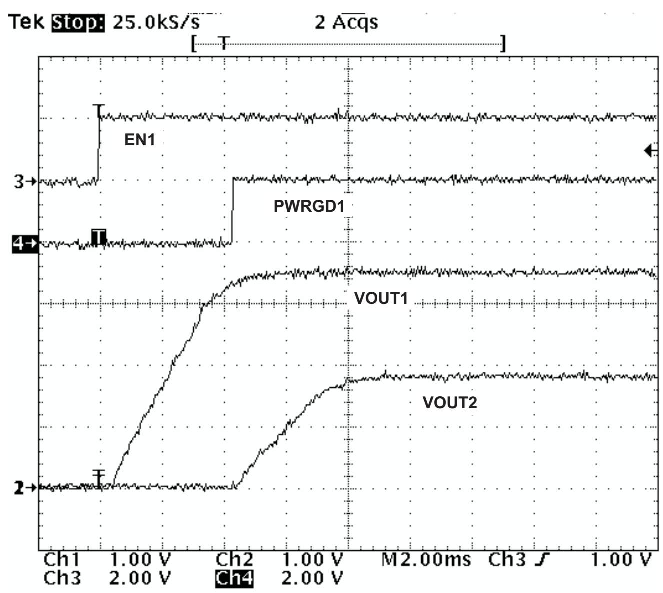


Figure 43. Sequential Startup Using EN and PWRGD

Device Functional Modes (continued)

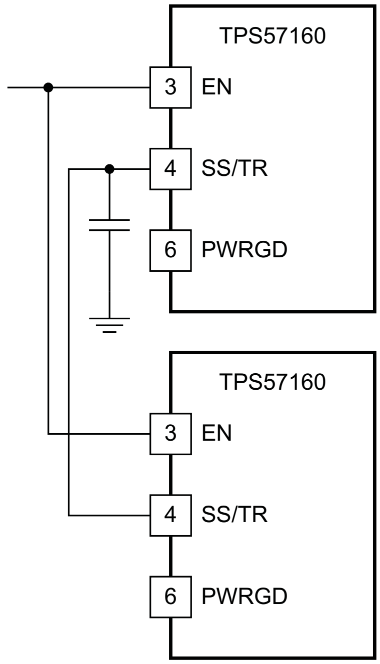


Figure 44. Schematic for Ratiometric Start-Up Using Coupled SS/TR Pins

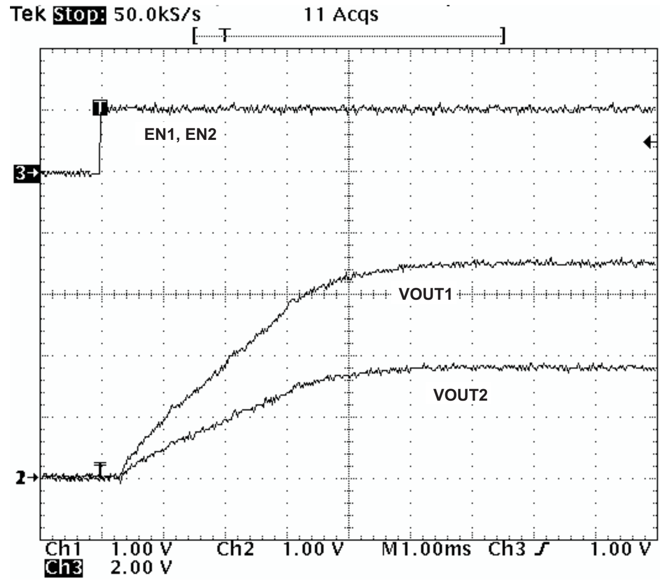


Figure 45. Ratiometric Startup Using Coupled SS/TR Pins

Figure 44 shows a method for ratiometric start-up sequence by connecting the SS/TR pins together. The regulator outputs ramp up and reach regulation at the same time. When calculating the slow start time, the pullup current source must be doubled in Equation 6. Figure 45 shows the results of Figure 44.

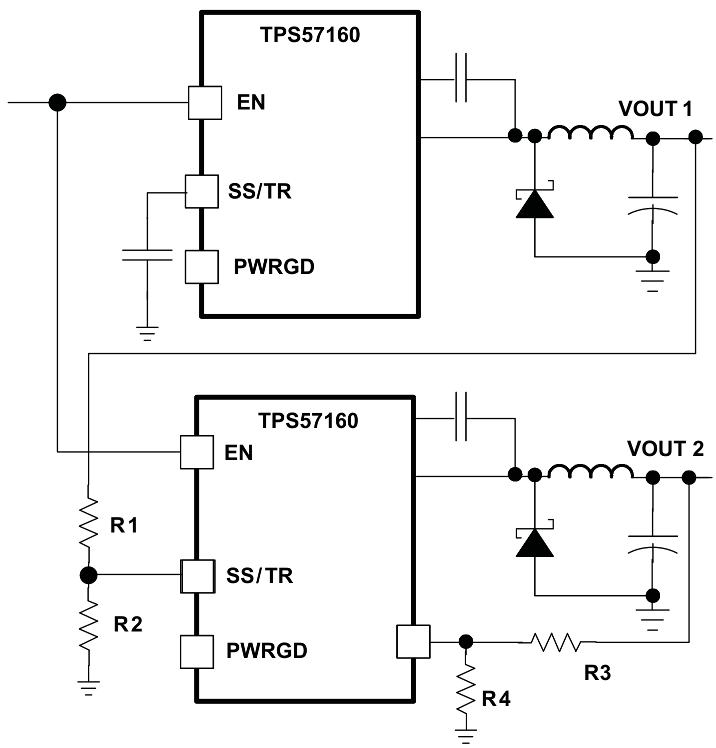


Figure 46. Schematic for Ratiometric and Simultaneous Start-Up Sequence

Device Functional Modes (continued)

Ratiometric and simultaneous power supply sequencing can be implemented by connecting the resistor network of R1 and R2 shown in Figure 46 to the output of the power supply that needs to be tracked or another voltage reference source. Using Equation 24 and Equation 25, the tracking resistors can be calculated to initiate the V_{OUT2} slightly before, after or at the same time as V_{OUT1}. Equation 26 is the voltage difference between V_{OUT1} and V_{OUT2} at the 95% of nominal output regulation.

The ΔV variable is zero volts for simultaneous sequencing. To minimize the effect of the inherent SS/TR to VSENSE offset ($V_{SSOFFSET}$) in the slow start circuit and the offset created by the pullup current source (I_{SS}) and tracking resistors, the $V_{SSOFFSET}$ and I_{SS} are included as variables in the equations.

To design a ratiometric start up in which the V_{OUT2} voltage is slightly greater than the V_{OUT1} voltage when V_{OUT2} reaches regulation, use a negative number in Equation 24 through Equation 26 for ΔV. Equation 26 results in a positive number for applications in which V_{OUT2} is slightly lower than V_{OUT1} when V_{OUT2} regulation is achieved.

Because the SS/TR pin must be pulled below 40 mV before starting after an EN, UVLO, or thermal shutdown fault, careful selection of the tracking resistors is needed to ensure device restart after a fault. Make sure the calculated R1 value from Equation 24 is greater than the value calculated in Equation 27 to ensure the device can recover from a fault.

As the SS/TR voltage becomes more than 85% of the nominal reference voltage the $V_{SSOFFSET}$ becomes larger as the slow start circuits gradually handoff the regulation reference to the internal voltage reference. The SS/TR pin voltage needs to be greater than 1.3 V for a complete handoff to the internal voltage reference as shown in Figure 23.

$$R1 = \frac{V_{OUT2} + \Delta V}{V_{REF}} \times \frac{V_{SSOFFSET}}{I_{SS}} \tag{24}$$

$$R2 = \frac{V_{REF} \times R1}{V_{OUT2} + \Delta V - V_{REF}} \tag{25}$$

$$\Delta V = V_{OUT1} - V_{OUT2} \tag{26}$$

$$R1 > 2800 \times V_{OUT1} - 180 \times \Delta V \tag{27}$$

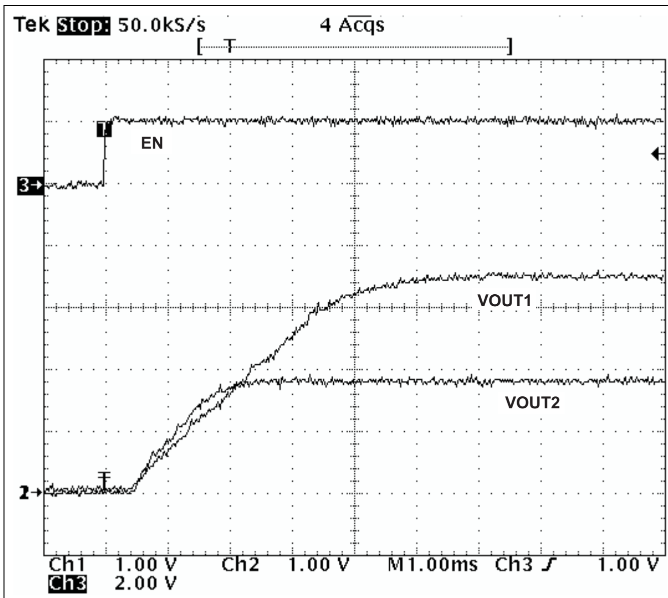


Figure 47. Ratiometric Startup With V_{OUT2} Leading V_{OUT1}

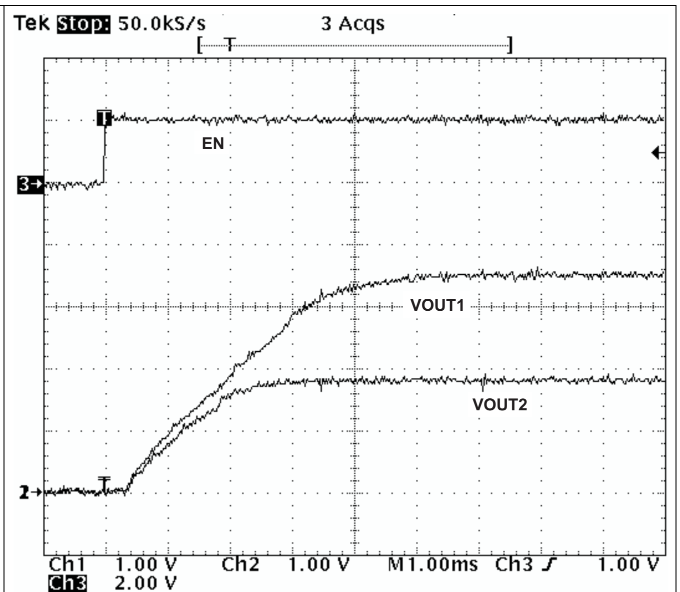


Figure 48. Ratiometric Startup With V_{OUT1} Leading V_{OUT2}

Device Functional Modes (continued)

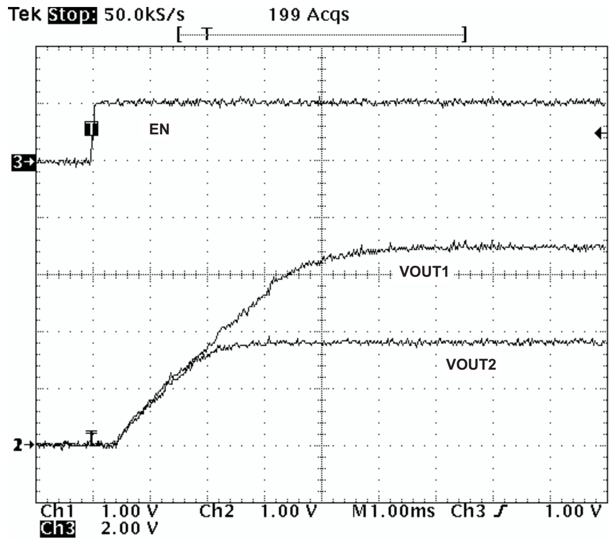


Figure 49. Simultaneous Startup With Tracking Resistor

8.4.2 Pulse-Skip Eco-Mode

The TPS57160-Q1 device operates in a pulse-skip Eco-mode control scheme at light load currents to improve efficiency by reducing switching and gate drive losses. The TPS57160-Q1 is designed so that if the output voltage is within regulation and the peak switch current at the end of any switching cycle is below the pulse skipping current threshold, the device enters Eco-mode control. This current threshold is the current level corresponding to a nominal COMP voltage or 500 mV.

When in Eco-mode, the COMP pin voltage is clamped at 500 mV and the high-side MOSFET is inhibited. Further decreases in load current or in output voltage cannot drive the COMP pin below this clamp voltage level.

Because the device is not switching, the output voltage begins to decay. As the voltage control loop compensates for the falling output voltage, the COMP pin voltage begins to rise. At this time, the high-side MOSFET is enabled and a switching pulse initiates on the next switching cycle. The peak current is set by the COMP pin voltage. The output voltage recharges the regulated value (see Figure 50), then the peak switch current starts to decrease, and eventually falls below the Eco-mode threshold at which time the device again enters Eco-mode.

For Eco-mode operation, the TPS57160-Q1 senses peak current, not average or load current, so the load current where the device enters Eco-mode is dependent on the output inductor value. For example, the circuit in Figure 51 enters Eco-mode at about 18 mA of output current. When the load current is low and the output voltage is within regulation, the device enters a sleep mode and draws only 116-μA input quiescent current. The internal PLL remains operating when in sleep mode. When operating at light load currents in the pulse skip mode, the switching transitions occur synchronously with the external clock signal.

Device Functional Modes (continued)

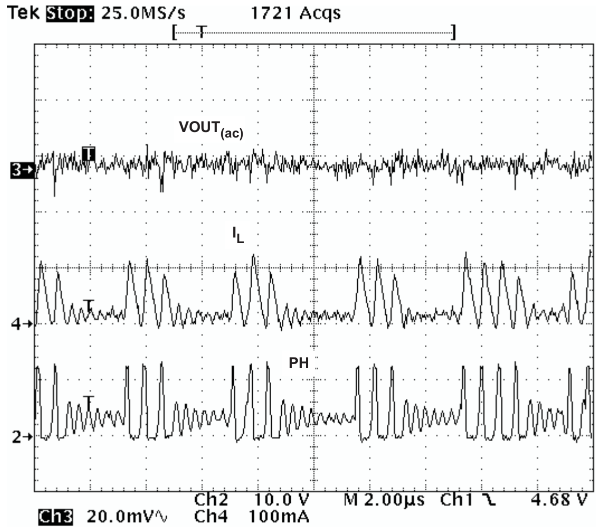


Figure 50. Pulse Skip Mode Operation

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TPS57160-Q1 DC-DC converter is designed to provide up to a 2.5-A output from an input voltage source of 3.5 V to 60 V. The high-side MOSFET is incorporated inside the TPS57160-Q1 package along with the gate-drive circuitry. The low drain-to-source on-resistance of the MOSFET allows the TPS57160-Q1 device to achieve high efficiencies and helps keep the junction temperature low at high output currents. The compensation components are external to the integrated circuit (IC), and an external divider allows for an adjustable output voltage. Additionally, the TPS57160-Q1 device provides adjustable slow start and undervoltage-lockout inputs.

9.2 Typical Application

This example details the design of a high frequency switching regulator design using ceramic output capacitors. A few parameters must be known to start the design process. These parameters are typically determined at the system level.

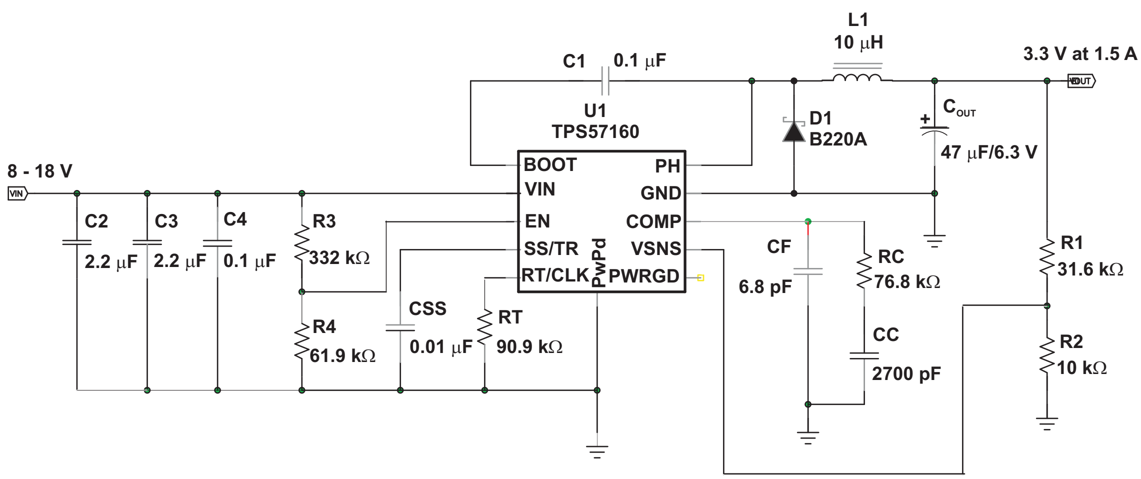


Figure 51. High Frequency, 3.3-V Output Power Supply Design with Adjusted UVLO

9.2.1 Design Requirements

For this example, start with the known parameters listed in Table 1.

Table 1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Output voltage	3.3 V
Transient response 0 to 1.5-A load step	ΔV_{OUT} = 4%
Maximum output current	1.5 A
Input voltage	12 V (nominal), 8 V to 18 V
Output voltage ripple	< 33 mV_{pp}
Start input voltage (rising VIN)	7.25 V
Stop input voltage (falling VIN)	6.25 V

9.2.2 Detailed Design Procedur

9.2.2.1 Selecting the Switching Frequency

The first step is to decide on a switching frequency for the regulator. Typically, the user wants to choose the highest switching frequency possible, because this produces the smallest solution size. The high switching frequency allows for lower valued inductors and smaller output capacitors compared to a power supply that switches at a lower frequency. The switching frequency that can be selected is limited by the minimum on-time of the internal power switch, the input voltage and the output voltage and the frequency shift limitation.

Equation 8 and Equation 9 must be used to find the maximum switching frequency for the regulator, choose the lower value of the two equations. Switching frequencies higher than these values result in pulse skipping or the lack of overcurrent protection during a short circuit.

The typical minimum on time (t_{onmin}) is 130 ns for the TPS57160-Q1 device. For this example, the output voltage is 3.3 V and the maximum input voltage is 18 V, which allows for a maximum switch frequency up to 1600 kHz when including the inductor resistance, on resistance and diode voltage in Equation 8. To ensure overcurrent runaway is not a concern during short circuits in your design use Equation 9 or the solid curve in Figure 33 to determine the maximum switching frequency. With a maximum input voltage of 20 V, for some margin above 18 V, assuming a diode voltage of 0.5 V, inductor resistance of 100 mΩ, switch resistance of 200 mΩ, a current limit value of 2.7 A, the maximum switching frequency is approximately 2500 kHz.

Choosing the lower of the two values and adding some margin a switching frequency of 1200 kHz is used. To determine the timing resistance for a given switching frequency, use Equation 7 or the curve in Figure 31.

The switching frequency is set by resistor R_t shown in Figure 51.

9.2.2.2 Output Inductor Selection (L_O)

To calculate the minimum value of the output inductor, use Equation 28.

K_{IND} is a coefficient that represents the amount of inductor ripple current relative to the maximum output current.

The inductor ripple current is filtered by the output capacitor. Therefore, choosing high inductor ripple currents impacts the selection of the output capacitor, because the output capacitor must have a ripple current rating equal to or greater than the inductor ripple current. In general, the inductor ripple value is at the discretion of the designer; however, the following guidelines may be used.

For designs using low ESR output capacitors such as ceramics, a value as high as K_{IND} = 0.3 may be used. When using higher ESR output capacitors, K_{IND} = 0.2 yields better results. Because the inductor ripple current is part of the PWM control system, the inductor ripple current should always be greater than 100 mA for dependable operation. In a wide input voltage regulator, it is best to choose an inductor ripple current on the larger side. This allows the inductor to still have a measurable ripple current with the input voltage at its minimum.

For this design example, use K_{IND} = 0.2 and the minimum inductor value is calculated to be 7.6 µH. For this design, a nearest standard value was chosen: 10 µH. For the output filter inductor, it is important that the RMS current and saturation current ratings not be exceeded. The RMS and peak inductor current can be found from Equation 30 and Equation 31.

For this design, the RMS inductor current is 1.506 A and the peak inductor current is 1.62 A. The chosen inductor is a MSS6132-103. It has a saturation current rating of 1.64 A and an RMS current rating of 1.9 A.

As the equation set demonstrates, lower ripple currents reduce the output voltage ripple of the regulator but require a larger value of inductance. Selecting higher ripple currents increases the output voltage ripple of the regulator but allows for a lower inductance value.

The current flowing through the inductor is the inductor ripple current plus the output current. During power up, faults or transient load conditions, the inductor current can increase above the calculated peak inductor current level calculated above. In transient conditions, the inductor current can increase up to the switch current limit of the device. For this reason, the most conservative approach is to specify an inductor with a saturation current rating equal to or greater than the switch current limit rather than the peak inductor current.

$$\text{Lo min} = \frac{\text{Vinmax} - \text{Vout}}{\text{Io} \times K_{IND}} \times \frac{\text{Vout}}{\text{Vinmax} \times f\text{sw}} \tag{28}$$

$$I_{RIPPLE} \leq I_O \times K_{IND} \quad (29)$$

$$I_{L(rms)} = \sqrt{(I_O)^2 + \frac{1}{12} \times \left(\frac{V_{OUT} \times (Vinmax - V_{OUT})}{Vinmax \times L_O \times f_{SW}} \right)^2} \quad (30)$$

$$I_{LPeak} = I_{OUT} + \frac{I_{RIPPLE}}{2} \quad (31)$$

9.2.2.3 Output Capacitor

There are three primary considerations for selecting the value of the output capacitor. The output capacitor determines the modulator pole, the output voltage ripple, and how the regulators responds to a large change in load current. The output capacitance needs to be selected based on the more stringent of these three criteria.

The desired response to a large change in the load current is the first criteria. The output capacitor needs to supply the load with current when the regulator cannot. This situation would occur if there are desired hold-up times for the regulator where the output capacitor must hold the output voltage above a certain level for a specified amount of time after the input power is removed. The regulator also temporarily is not able to supply sufficient output current if there is a large fast increase in the current needs of the load such as transitioning from no load to a full load. The regulator usually needs two or more clock cycles for the control loop to see the change in load current and output voltage and adjust the duty cycle to react to the change. The output capacitor must be sized to supply the extra current to the load until the control loop responds to the load change. The output capacitance must be large enough to supply the difference in current for two clock cycles while only allowing a tolerable amount of droop in the output voltage. Equation 32 shows the minimum output capacitance necessary to accomplish this.

Where ΔI_{OUT} is the change in output current, $f$sw is the regulators switching frequency and ΔV_{OUT} is the allowable change in the output voltage. For this example, the transient load response is specified as a 4% change in V_{OUT} for a load step from 0 A (no load) to 1.5 A (full load). For this example, ΔI_{OUT} = 1.5 – 0 = 1.5 A and ΔV_{OUT} = 0.04 × 3.3 = 0.132 V. Using these numbers gives a minimum capacitance of 18.9 μF. This value does not take the ESR of the output capacitor into account in the output voltage change. For ceramic capacitors, the ESR is usually small enough to ignore in this calculation. Aluminum electrolytic and tantalum capacitors have higher ESR that should be taken into account.

The catch diode of the regulator cannot sink current, so any stored energy in the inductor produces an output voltage overshoot when the load current rapidly decreases (see Figure 52). The output capacitor must be sized to absorb energy stored in the inductor when transitioning from a high load current to a lower load current. The excess energy that is stored in the output capacitor increases the voltage on the capacitor. The capacitor must be sized to maintain the desired output voltage during these transient periods. Equation 33 is used to calculate the minimum capacitance to keep the output voltage overshoot to a desired value. Where L is the value of the inductor, I_{OH} is the output current under heavy load, I_{OL} is the output under light load, VF is the final peak output voltage, and Vi is the initial capacitor voltage. For this example, the worst-case load step us from 1.5 A to 0 A. The output voltage increases during this load transition, and the stated maximum in our specification is 4% of the output voltage. This makes VF = 1.04 × 3.3 = 3.432. Vi is the initial capacitor voltage, which is the nominal output voltage of 3.3 V. Using these numbers in Equation 33 yields a minimum capacitance of 25.3 μF.

Equation 34 calculates the minimum output capacitance needed to meet the output voltage ripple specification. Where f_{sw} is the switching frequency, $V_{oripple}$ is the maximum allowable output voltage ripple, and I_{ripple} is the inductor ripple current. Equation 35 yields 0.7 μF.

Equation 35 calculates the maximum ESR an output capacitor can have to meet the output voltage ripple specification. Equation 35 indicates the ESR should be less than 147 mΩ.

The most stringent criteria for the output capacitor is 25.3 μF of capacitance to keep the output voltage in regulation during an unload transient.

Additional capacitance de-ratings for aging, temperature, and dc bias should be factored in, which increases this minimum value. For this example, a 47-μF 6.3-V X7R ceramic capacitor with 5-mΩ ESR is used.

Capacitors generally have limits to the amount of ripple current they can handle without failing or producing excess heat. An output capacitor that can support the inductor ripple current must be specified. Some capacitor data sheets specify the root mean square (RMS) value of the maximum ripple current. Equation 36 can be used to calculate the RMS ripple current the output capacitor needs to support. For this application, Equation 36 yields 64.8 mA.

$$C_{OUT} > \frac{2 \times \Delta I_{OUT}}{f_{SW} \times \Delta V_{OUT}} \tag{32}$$

$$C_{OUT} > L_O \times \frac{\left((I_{OH})^2 - (I_{OL})^2\right)}{\left((V_f)^2 - (V_i)^2\right)} \tag{33}$$

$$C_{OUT} > \frac{1}{8 \times f_{SW}} \times \frac{1}{\left(\frac{V_{OUT(ripple)}}{I_{RIPPLE}}\right)} \tag{34}$$

$$R_{ESR} = \frac{V_{OUT(ripple)}}{I_{RIPPLE}} \tag{35}$$

$$I_{COUT(rms)} = \frac{V_{OUT} \times \left(V_{IN(max)} - V_{OUT}\right)}{\sqrt{12} \times V_{IN(max)} \times L_O \times f_{SW}} \tag{36}$$

9.2.2.4 Catch Diode

The TPS57160-Q1 device requires an external catch diode between the PH pin and GND. The selected diode must have a reverse voltage rating equal to or greater than $V_{IN(max)}$. The peak current rating of the diode must be greater than the maximum inductor current. The diode should also have a low forward voltage. Schottky diodes are typically a good choice for the catch diode due to their low forward voltage. The lower the forward voltage of the diode, the higher the efficiency of the regulator.

Typically, the higher the voltage and current ratings the diode has, the higher the forward voltage. Because the design example has an input voltage up to 18 V, a diode with a minimum of 20-V reverse voltage is selected.

For the example design, the B220A Schottky diode is selected for its lower forward voltage, and it comes in a larger package size, which has good thermal characteristics over small devices. The typical forward voltage of the B220A is 0.50 V.

The diode must also be selected with an appropriate power rating. The diode conducts the output current during the off-time of the internal power switch. The off-time of the internal switch is a function of the maximum input voltage, the output voltage, and the switching frequency. The output current during the off-time is multiplied by the forward voltage of the diode which equals the conduction losses of the diode. At higher switch frequencies, the ac losses of the diode need to be taken into account. The ac losses of the diode are due to the charging and discharging of the junction capacitance and reverse recovery. Equation 37 is used to calculate the total power dissipation, conduction losses plus ac losses, of the diode.

The B220A has a junction capacitance of 120 pF. Using Equation 37, the selected diode dissipates 0.632 W. This power dissipation, depending on mounting techniques, should produce a 16°C temperature rise in the diode when the input voltage is 18 V and the load current is 1.5 A.

If the power supply spends a significant amount of time at light load currents or in sleep mode consider using a diode which has a low leakage current and slightly higher forward voltage drop.

$$P_D = \frac{\left(V_{IN(max)} - V_{OUT}\right) \times I_{OUT} \times V f d}{V_{IN(max)}} + \frac{C_j \times f_{SW} \times \left(V_{IN} + V f d\right)^2}{2} \tag{37}$$

9.2.2.5 Input Capacitor

The TPS57160-Q1 device requires a high-quality ceramic, type X5R or X7R, input decoupling capacitor of at least 3-μF effective capacitance and, in some applications, a bulk capacitance. The effective capacitance includes any dc bias effects. The voltage rating of the input capacitor must be greater than the maximum input voltage. The capacitor must also have a ripple current rating greater than the maximum input current ripple of the TPS57160-Q1. The input ripple current can be calculated using Equation 38.

The value of a ceramic capacitor varies significantly over temperature and the amount of dc bias applied to the capacitor. The capacitance variations due to temperature can be minimized by selecting a dielectric material that is stable over temperature. X5R and X7R ceramic dielectrics are usually selected for power regulator capacitors because they have a high capacitance to volume ratio and are fairly stable over temperature. The output capacitor must also be selected with the dc bias taken into account. The capacitance value of a capacitor decreases as the dc bias across a capacitor increases.

For this example design, a ceramic capacitor with at least a 20-V voltage rating is required to support the maximum input voltage. Common standard ceramic capacitor voltage ratings include 4 V, 6.3 V, 10 V, 16 V, 25 V, 50 V or 100 V, so a 25-V capacitor should be selected. For this example, two 2.2-μF 25-V capacitors in parallel have been selected. Table 2 shows a selection of high voltage capacitors. The input capacitance value determines the input ripple voltage of the regulator. The input voltage ripple can be calculated using Equation 39. Using the design example values, I_{outmax} = 1.5 A, C_{IN} = 4.4 μF, f_{sw} = 1200 kHz, yields an input voltage ripple of 71 mV and an RMS input ripple current of 0.701 A.

$$\text{Icirms} = \text{Iout} \times \sqrt{\frac{\text{Vout}}{\text{Vin min}} \times \frac{(\text{Vin min} - \text{Vout})}{\text{Vin min}}} \tag{38}$$

$$\Delta\text{Vin} = \frac{\text{Iout max} \times 0.25}{\text{Cin} \times f\text{sw}} \tag{39}$$

Table 2. Capacitor Types

VENDOR	VALUE (μF)	EIA SIZE	VOLTAGE	DIELECTRIC	COMMENTS
Murata	1 to 2.2	1210	100 V	X7R	GRM32 series
	1 to 4.7		50 V		
	1	1206	100 V		GRM31 series
	1 to 2.2		50 V		
Vishay	1 10 1.8	2220	50 V		VJ X7R series
	1 to 1.2		100 V		
	1 to 3.9	2225	50 V		
	1 to 1.8		100 V		
TDK	1 to 2.2	1812	100 V		C series C4532
	1.5 to 6.8		50 V		
	1 to 2.2	1210	100 V		C series C3225
	1 to 3.3		50 V		
AVX	1 to 4.7	1210	50 V		X7R dielectric series
	1		100 V		
	1 to 4.7	1812	50 V		
	1 to 2.2		100 V		

9.2.2.6 Slow-Start Capacitor

The slow-start capacitor determines the minimum amount of time required for the output voltage to reach its nominal programmed value during power up. This is useful if a load requires a controlled voltage slew rate. This is also used if the output capacitance is large and would require large amounts of current to quickly charge the capacitor to the output voltage level. The large currents necessary to charge the capacitor may make the TPS57160-Q1 reach the current limit or excessive current draw from the input power supply may cause the input voltage rail to sag. Limiting the output voltage slew rate solves both of these problems.

The slow start time must be long enough to allow the regulator to charge the output capacitor up to the output voltage without drawing excessive current. Equation 40 can be used to find the minimum slow start time, T_{SS}, necessary to charge the output capacitor, C_{OUT}, from 10% to 90% of the output voltage, V_{OUT}, with an average slow start current of I_{SSAVG}. In the example, to charge the 47-µF output capacitor up to 3.3 V while only allowing the average input current to be 0.125 A requires a 1-ms slow start time.

Once the slow start time is known, the slow-start capacitor value can be calculated using Equation 6. For the example circuit, the slow start time is not too critical, because the output capacitor value is 47 µF which does not require much current to charge to 3.3 V. The example circuit has the slow start time set to an arbitrary value of 1ms which requires a 3.3-nF capacitor.

$$T_{SS} > \frac{C_{OUT} \times V_{OUT} \times 0.8}{I_{SSAVG}} \tag{40}$$

9.2.2.7 Bootstrap Capacitor Selection

A 0.1-µF ceramic capacitor must be connected between the BOOT and PH pins for proper operation. It is recommended to use a ceramic capacitor with X5R or better grade dielectric. The capacitor should have a 10-V or higher voltage rating.

9.2.2.8 Undervoltage Lockout (UVLO) Set Point

The UVLO can be adjusted using an external voltage divider on the EN pin of the TPS57160-Q1. The UVLO has two thresholds, one for power up when the input voltage is rising and one for power down or brown outs when the input voltage is falling. For the example design, the supply should turn on and start switching once the input voltage increases above 7.25 V (enabled). After the regulator starts switching, it should continue to do so until the input voltage falls below 6.25 V (UVLO stop).

The programmable UVLO and enable voltages are set using a resistor divider between Vin and ground to the EN pin. Equation 2 through Equation 3 can be used to calculate the resistance values necessary. For the example application, a 332 kΩ between Vin and EN and a 61.9 kΩ between EN and ground are required to produce the 7.25 V and 6.25 V start and stop voltages.

9.2.2.9 Output Voltage and Feedback Resistors Selection

For the example design, 10 kΩ was selected for R2. Using Equation 1, R1 is calculated as 31.25 kΩ. The nearest standard 1% resistor is 31.6 kΩ. Due to current leakage of the VSENSE pin, the current flowing through the feedback network should be greater than 1 µA to maintain the output voltage accuracy. This requirement makes the maximum value of R2 equal to 800 kΩ. Choosing higher resistor values decreases quiescent current and improves efficiency at low output currents but may introduce noise immunity problems.

9.2.2.10 Compensation

There are several industry techniques used to compensate DC/DC regulators. The method presented here yields high phase margins. For most conditions, the regulator will have a phase margin between 60 and 90 degrees. The method presented here ignores the effects of the slope compensation that is internal to the TPS57160-Q1. Since the slope compensation is ignored, the actual crossover frequency is usually lower than the crossover frequency used in the calculations.

Use SwitcherPro software for a more accurate design.

The uncompensated regulator will have a dominant pole, typically located between 300 Hz and 3 kHz, due to the output capacitor and load resistance and a pole due to the error amplifier. One zero exists due to the output capacitor and the ESR. The zero frequency is higher than either of the two poles.

If left uncompensated, the double pole created by the error amplifier and the modulator would lead to an unstable regulator. To stabilize the regulator, one pole must be canceled out. One design approach is to locate a compensating zero at the modulator pole. Then select a crossover frequency that is higher than the modulator pole. The gain of the error amplifier can be calculated to achieve the desired crossover frequency. The capacitor used to create the compensation zero along with the output impedance of the error amplifier form a low frequency pole to provide a minus one slope through the crossover frequency. Then a compensating pole is added to cancel the zero due to the output capacitors ESR. If the ESR zero resides at a frequency higher than the switching frequency then it can be ignored.

To compensate the TPS57160-Q1 using this method, first calculate the modulator pole and zero using the following equations:

$$f_{P(mod)} = \frac{I_{OUT(max)}}{2 \times \pi \times V_{OUT} \times C_{OUT}}$$

where

- $I_{OUT(max)}$ is the maximum output current
- C_{OUT} is the output capacitance
- V_{OUT} is the nominal output voltage (41)

$$f_{Z(mod)} = \frac{1}{2 \times \pi \times R_{ESR} \times C_{OUT}} \tag{42}$$

For the example design, the modulator pole is located at 1.5 kHz and the ESR zero is located at 338 kHz.

Next, the designer selects a crossover frequency which will determine the bandwidth of the control loop. The crossover frequency must be located at a frequency at least five times higher than the modulator pole. The crossover frequency must also be selected so that the available gain of the error amplifier at the crossover frequency is high enough to allow for proper compensation.

Equation 47 is used to calculate the maximum crossover frequency when the ESR zero is located at a frequency that is higher than the desired crossover frequency. This will usually be the case for ceramic or low ESR tantalum capacitors. Aluminum Electrolytic and Tantalum capacitors will typically produce a modulator zero at a low frequency due to their high ESR.

The example application is using a low ESR ceramic capacitor with 10 mΩ of ESR making the zero at 338 kHz.

This value is much higher than typical crossover frequencies so the maximum crossover frequency is calculated using both Equation 43 and Equation 46.

Using Equation 46 gives a minimum crossover frequency of 7.6 kHz and Equation 43 gives a maximum crossover frequency of 45.3 kHz.

A crossover frequency of 45 kHz is arbitrarily selected from this range.

For ceramic capacitors use Equation 43:

$$f_{C(max)} \le 2100\sqrt{\frac{f_{P(mod)}}{V_{OUT}}} \tag{43}$$

For tantalum or aluminum capacitors use Equation 44:

$$f_{C(max)} \le \frac{51442}{\sqrt{V_{OUT}}} \tag{44}$$

For all cases use Equation 45 and Equation 46:

$$f_{C(max)} \le \frac{f_{SW}}{5} \tag{45}$$

$$f_{C(min)} \ge 5 \times f_{P(mod)} \tag{46}$$

When a crossover frequency, f_C, has been selected, the gain of the modulator at the crossover frequency is calculated. The gain of the modulator at the crossover frequency is calculated using Equation 47 .

$$G_{MOD(fc)} = \frac{gm_{(PS)} \times R_{LOAD} \times (2\pi \times f_C \times C_{OUT} \times R_{ESR} + 1)}{2\pi \times f_C \times C_{OUT} \times (R_{LOAD} + R_{ESR}) + 1} \tag{47}$$

For the example problem, the gain of the modulator at the crossover frequency is 0.542. Next, the compensation components are calculated. A resistor in series with a capacitor is used to create a compensating zero. A capacitor in parallel to these two components forms the compensating pole. However, calculating the values of these components varies depending on if the ESR zero is located above or below the crossover frequency. For ceramic or low ESR tantalum output capacitors, the zero will usually be located above the crossover frequency. For aluminum electrolytic and tantalum capacitors, the modulator zero is usually located lower in frequency than the crossover frequency. For cases where the modulator zero is higher than the crossover frequency (ceramic capacitors).

$$R_C = \frac{V_{OUT}}{G_{MOD(fc)} \times gm_{(EA)} \times V_{REF}} \tag{48}$$

$$C_C = \frac{1}{2\pi \times R_C \times f_{P(mod)}} \tag{49}$$

$$Cf = \frac{C_{OUT} \times R_{ESR}}{R_C} \tag{50}$$

For cases where the modulator zero is less than the crossover frequency (Aluminum or Tantalum capacitors), the equations are as follows:

$$R_C = \frac{V_{OUT}}{G_{MOD(fc)} \times f_{Z(mod)} \times gm_{(EA)} \times V_{REF}} \tag{51}$$

$$C_C = \frac{1}{2\pi \times R_C \times f_{P(mod)}} \tag{52}$$

$$Cf = \frac{1}{2\pi \times R_C \times f_{Z(mod)}} \tag{53}$$

For the example problem, the ESR zero is located at a higher frequency compared to the crossover frequency so Equation 50 through Equation 53 are used to calculate the compensation components. In this example, the calculated components values are:

- R_C= 76.2 kΩ
- C_C= 2710 pF
- C_f =6.17 pF

The calculated value of the C_f capacitor is not a standard value so a value of 2700 pF is used. 6.8 pF is used for C_C. The R_C resistor sets the gain of the error amplifier which determines the crossover frequency. The calculated R_C resistor is not a standard value, so 76.8 kΩ is used.

9.2.2.11 Power Dissipation

The following formulas show how to estimate power dissipation under continuous conduction mode (CCM) operation. These equations should not be used if the device is working in discontinuous conduction mode (DCM).

The power dissipation of the device includes conduction loss (P_{con}), switching loss (P_{sw}), gate drive loss (P_{gd}), and supply current loss (P_q).

$$P_{con} = I_O^2 \times R_{DS(on)} \times (V_{OUT} / V_{IN})$$

where

- I_O is the output current (A).
- $R_{DS(on)}$ is the on-resistance of the high-side MOSFET (Ω).
- V_{OUT} is the output voltage (V).
- V_{IN} is the input voltage (V). (54)

$$P_{SW} = V_{IN}^2 \times f_{SW} \times I_O \times 0.25 \times 10^{-9} sec/V$$

where

- f_{sw} is the switching frequency (Hz). (55)

$$P_{gd} = V_{IN} \times 3 \times 10^{-9} Asec \times f_{SW} \quad (56)$$

$$P_q = 116 \mu A \times V_{IN} \quad (57)$$

Therefore:

$$P_{tot} = P_{con} + P_{SW} + P_{gd} + P_q$$

where

- P_{tot} is the total device power dissipation (W). (58)

For given T_A,

$$T_J = T_A + \theta_{JA} \times P_{tot}$$

where

- T_A is the ambient temperature (°C).
- T_J is the junction temperature (°C).
- θ_{JA} is the thermal resistance of the package (°C/W). (59)

For given $T_{J(MAX)}$ = 150°C

$$T_{A(MAX)} = T_{J(MAX)} - \theta_{JA} \times P_{tot}$$

where

- $T_{J(MAX)}$ is maximum junction temperature (°C).
- $T_{A(MAX)}$ is maximum ambient temperature (°C). (60)

Additional power losses occur in the regulator circuit because of the inductor ac and dc losses, the catch diode, and trace resistance that impact the overall efficiency of the regulator.

9.2.3 Application Curves

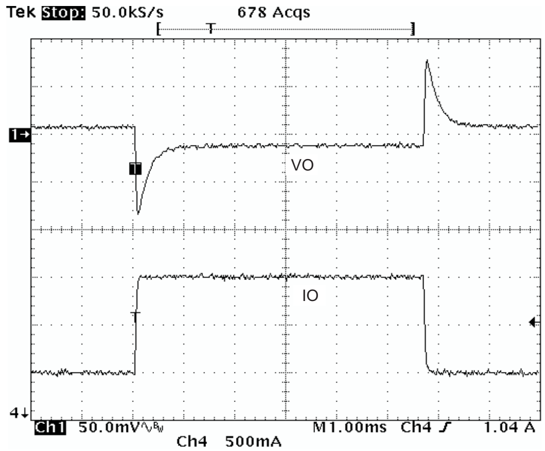


Figure 52. Load Transmit

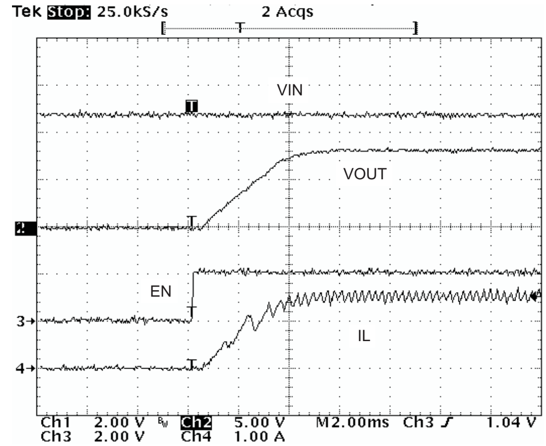


Figure 53. Startup With EN

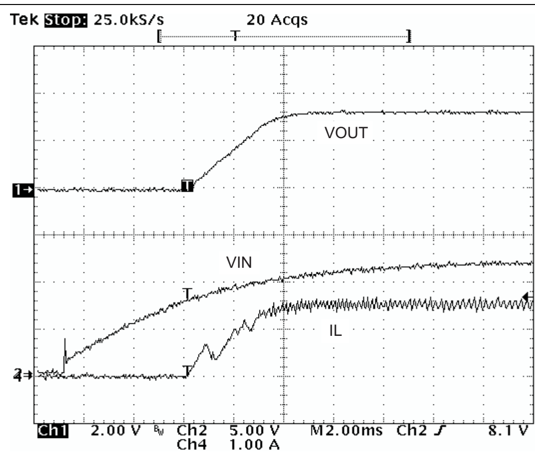


Figure 54. VIN Power Up

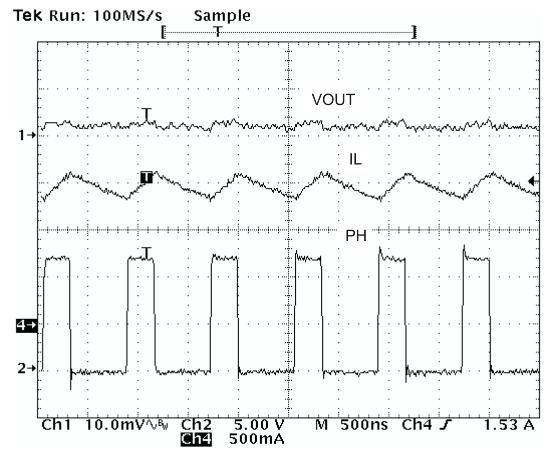


Figure 55. Output Ripple CCM

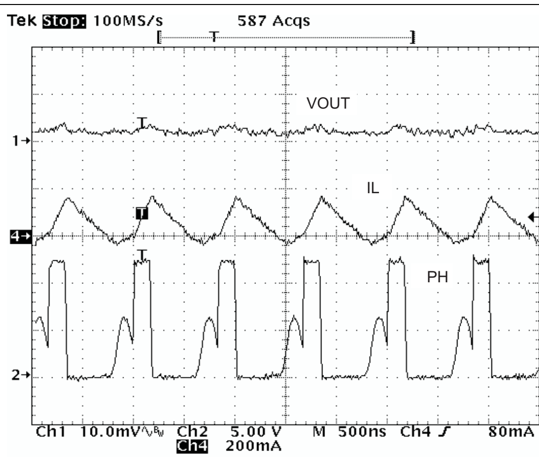


Figure 56. Output Ripple, DCM

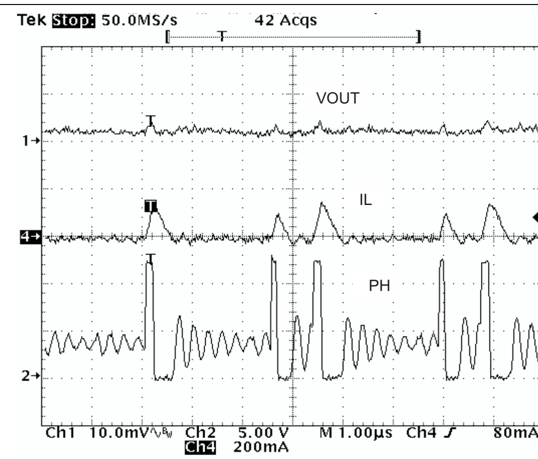


Figure 57. Output Ripple, PSM

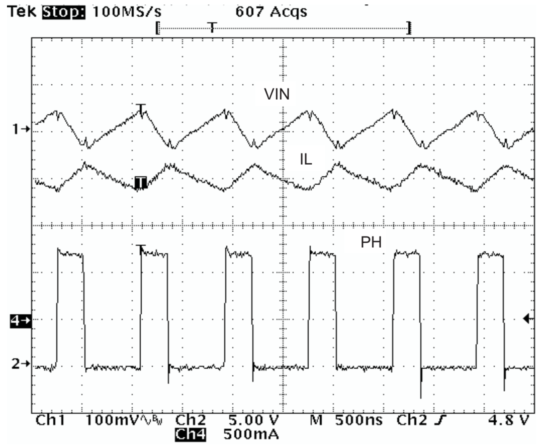


Figure 58. Input Ripple CCM

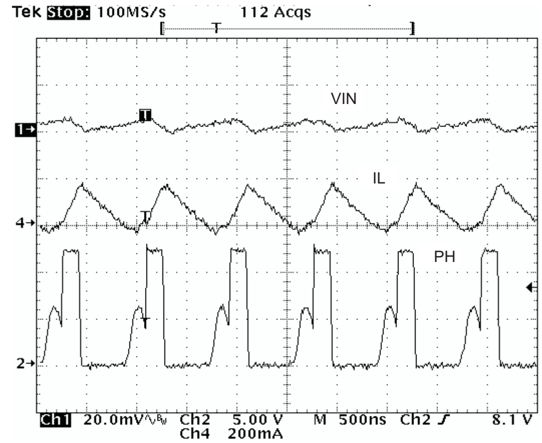


Figure 59. Input Ripple DCM

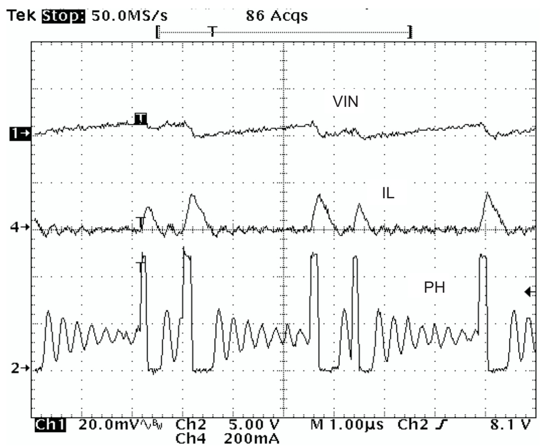


Figure 60. Input Ripple PSM

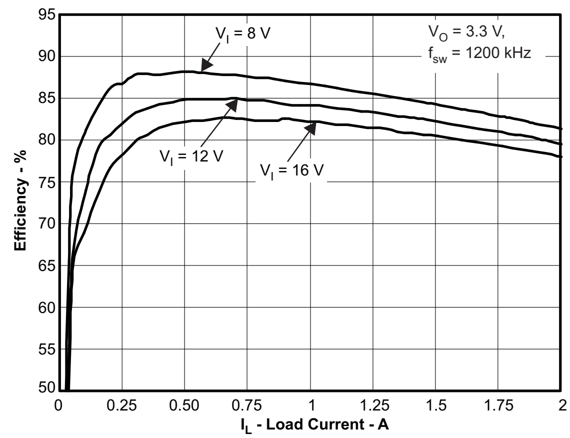


Figure 61. Efficiency vs Load Current

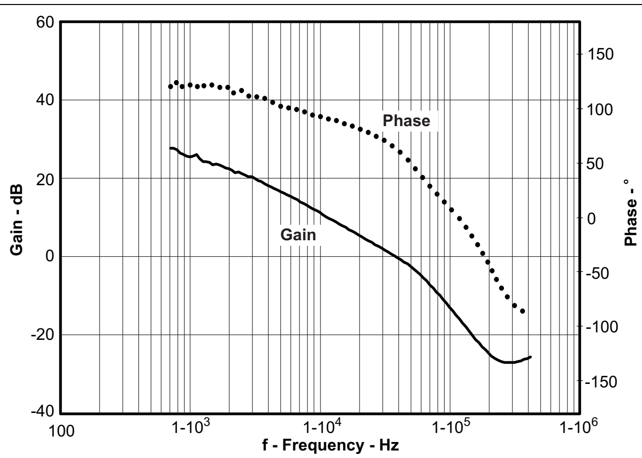


Figure 62. Overall Loop Frequency Response

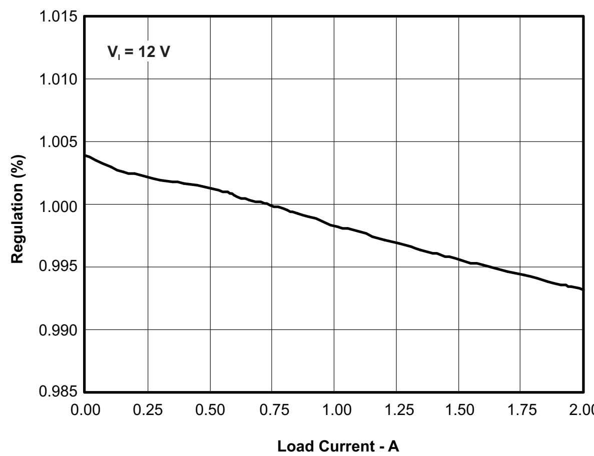


Figure 63. Regulation vs Load Current

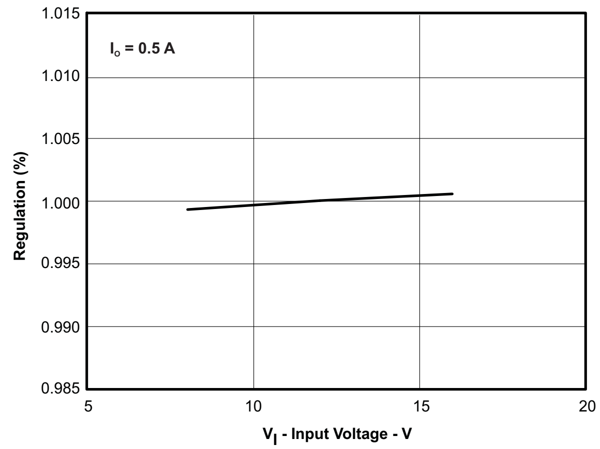


Figure 64. Regulation vs Input Voltage

10 Power Supply Recommendations

The input decoupling capacitors and bootstrap capacitor must be located as close as possible to the TPS57160-Q1 device. In addition, the voltage set-point resistor divider components must also be kept close to the device. This feedback-resistor voltage divider network ties the output voltage (V_{OUT}) to the VSENSE pin as a copper trace subsequent to the output capacitors. Ensure that input power supply is clean. TI recommends adding an additional input bulk capacitor depending on the board connection to the input supply.

11 Layout

11.1 Layout Guidelines

Layout is a critical portion of good power supply design. There are several signals paths that conduct fast changing currents or voltages that can interact with stray inductance or parasitic capacitance to generate noise or degrade the power supplies performance. To help eliminate these problems, the VIN pin should be bypassed to ground with a low ESR ceramic bypass capacitor with X5R or X7R dielectric. Care should be taken to minimize the loop area formed by the bypass capacitor connections, the VIN pin, and the anode of the catch diode. See Figure 65 for a PCB layout example. The GND pin should be tied directly to the PowerPAD and the IC.

The PowerPAD should be connected to any internal PCB ground planes using multiple vias directly under the IC. The PH pin should be routed to the cathode of the catch diode and to the output inductor. Because the PH connection is the switching node, the catch diode and output inductor should be located close to the PH pins, and the area of the PCB conductor minimized to prevent excessive capacitive coupling. For operation at full rated load, the top side ground area must provide adequate heat dissipating area. The RT/CLK pin is sensitive to noise so the RT resistor should be located as close as possible to the IC and routed with minimal lengths of trace. The additional external components can be placed approximately as shown. It may be possible to obtain acceptable performance with alternate PCB layouts, however this layout has been shown to produce good results and is meant as a guideline.

11.2 Layout Example

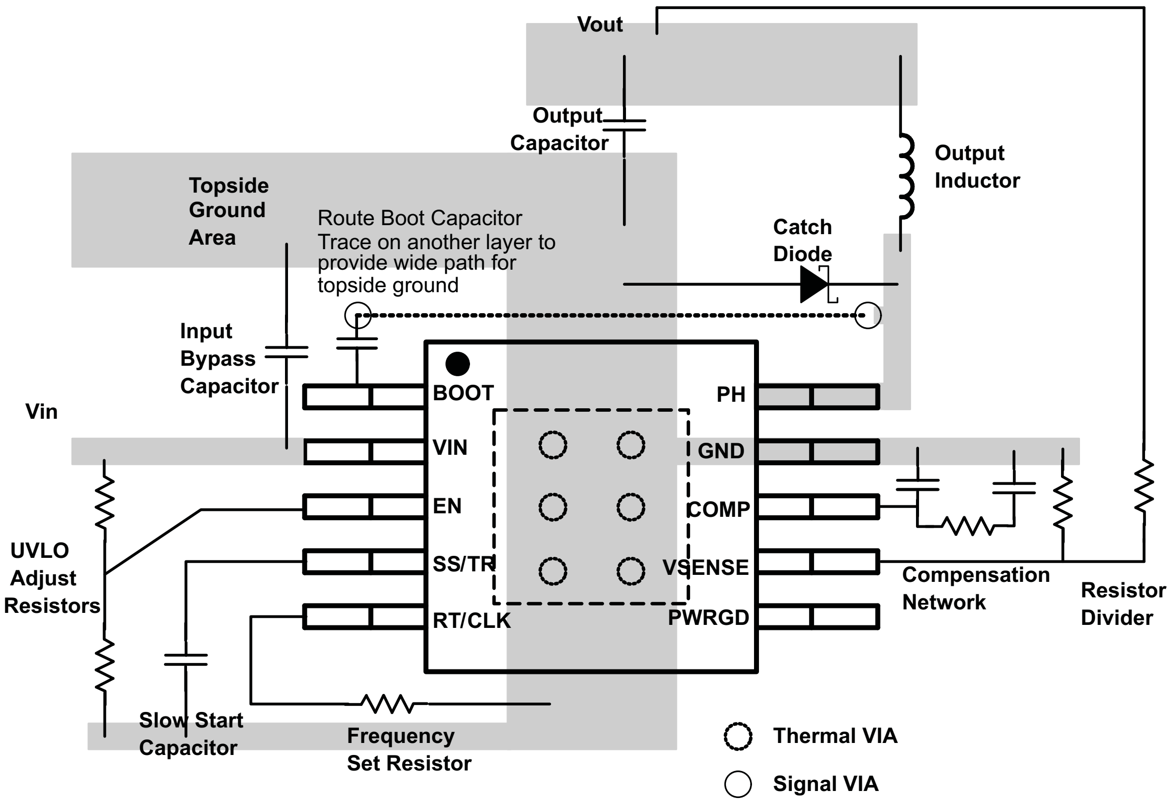


Figure 65. PCB Layout Example

Layout Example (continued)

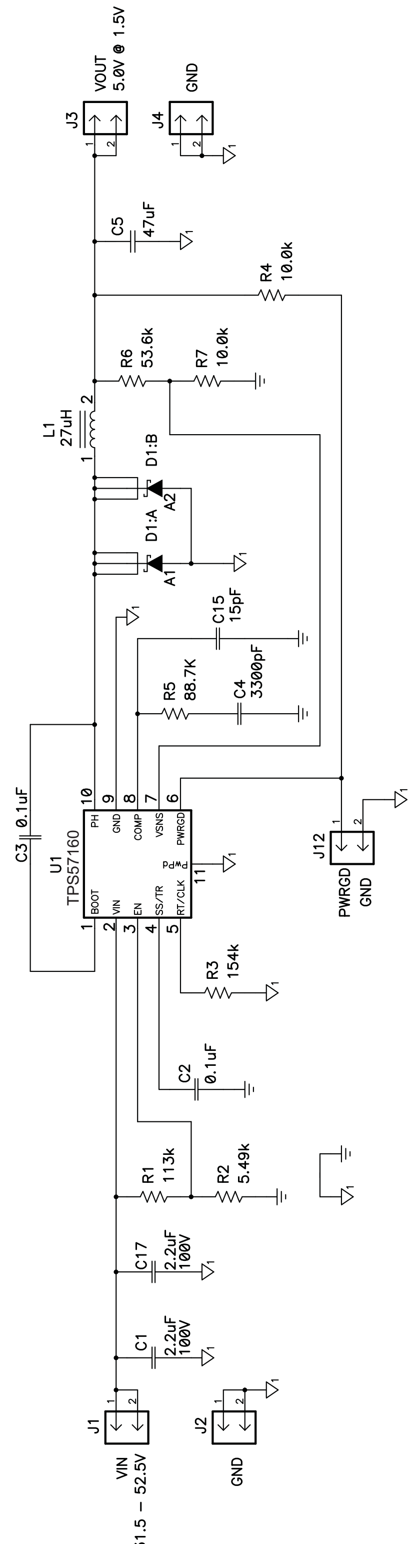


Figure 66. Wide Input Voltage Design

12 Device and Documentation Support

12.1 Device Support

12.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

12.1.2 Development Support

For the SwitcherPro Software Tool go to ti.com/tool/switcherpro.

12.2 Community Resource

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 Trademarks

Eco-mode, SwitcherPro, PowerPAD, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS57160QDGQRQ1	ACTIVE	HVSSOP	DGQ	10	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	5716Q	Samples
TPS57160QDRCRQ1	ACTIVE	VSON	DRC	10	3000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	5716Q	Samples
TPS57160ZQDGQRQ1	ACTIVE	HVSSOP	DGQ	10	2500	RoHS & Green	NIPDAUAG	Level-3-260C-168 HR	-40 to 125	5716Z	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

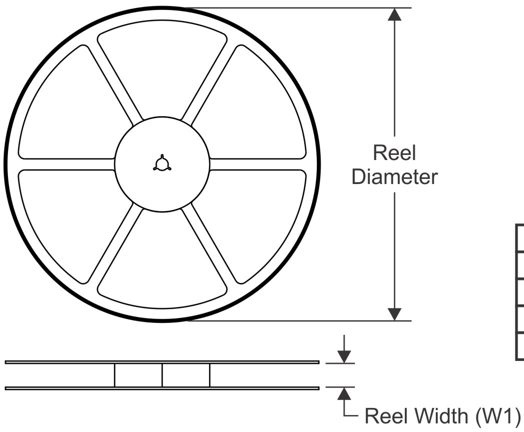
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

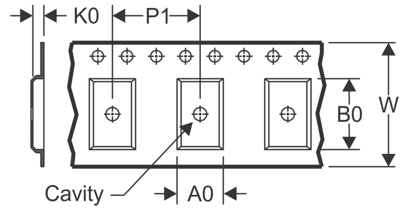
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

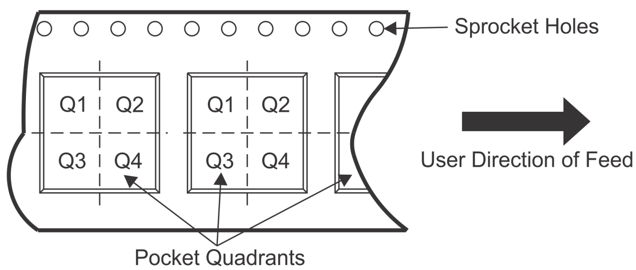


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

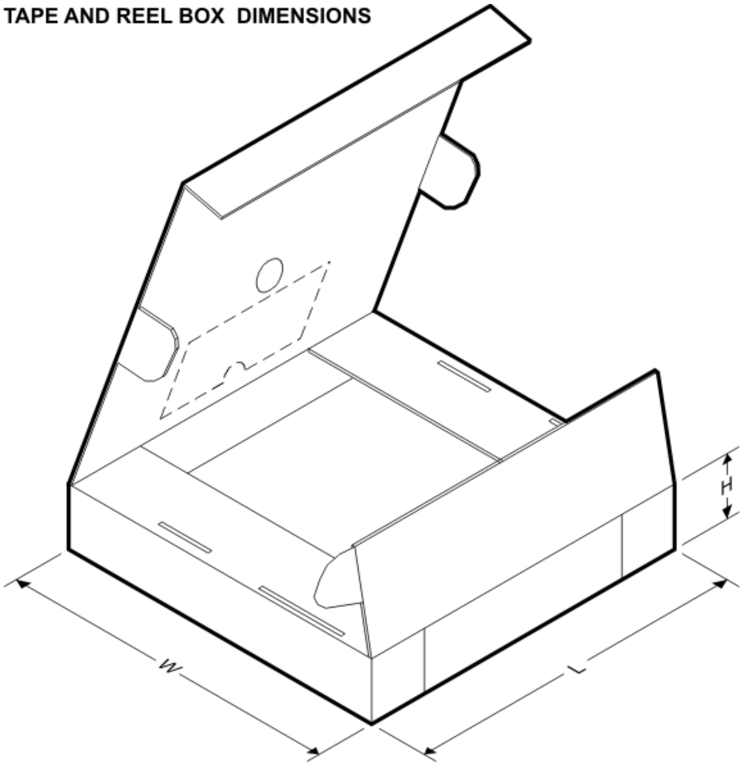
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS57160QDGQRQ1	HVSSOP	DGQ	10	2500	330.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1
TPS57160QDRCRQ1	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q2
TPS57160ZQDGQRQ1	HVSSOP	DGQ	10	2500	330.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

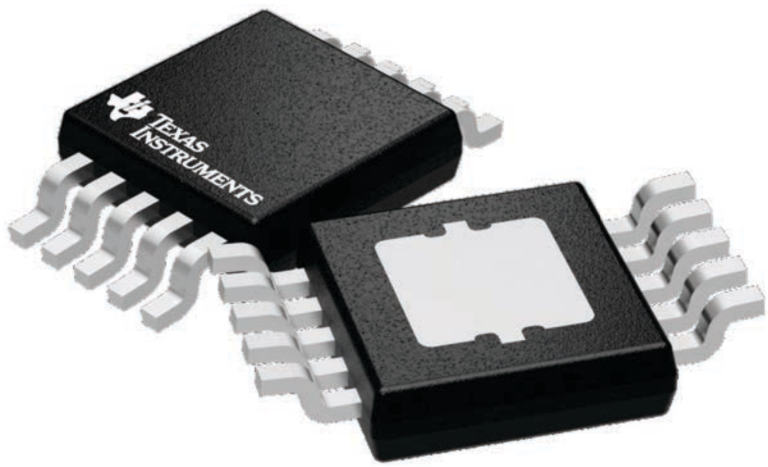
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS57160QDGQRQ1	HVSSOP	DGQ	10	2500	367.0	367.0	38.0
TPS57160QDRCRQ1	VSON	DRC	10	3000	367.0	367.0	38.0
TPS57160ZQDGQRQ1	HVSSOP	DGQ	10	2500	367.0	367.0	38.0

DGQ 10

PowerPAD™ HVSSOP - 1.1 mm max height

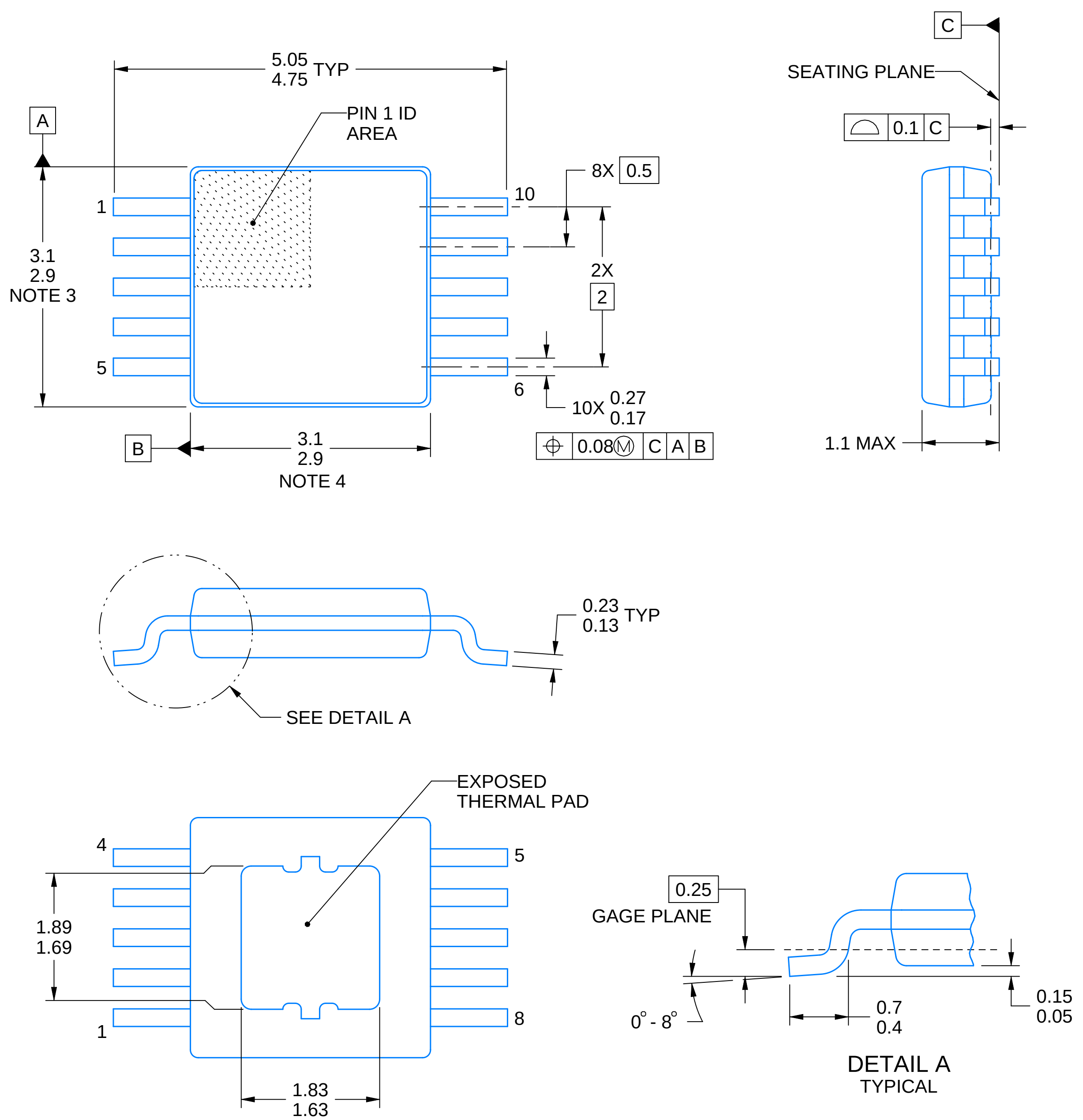
3 x 3, 0.5 mm pitch

PLASTIC SMALL OUTLINE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4224775/A

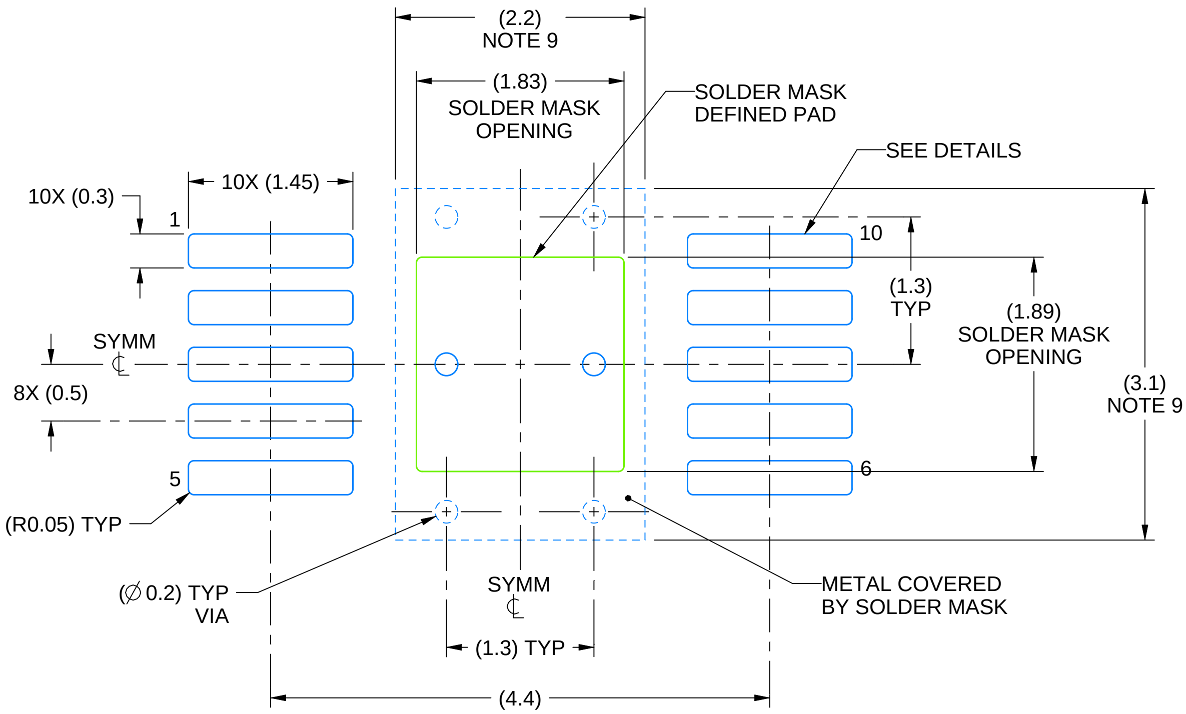


4218842/A 01/2019

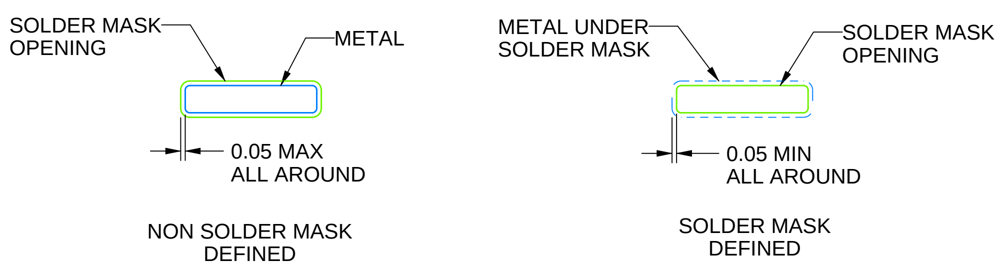
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA-T.



LAND PATTERN EXAMPLE
SCALE:15X

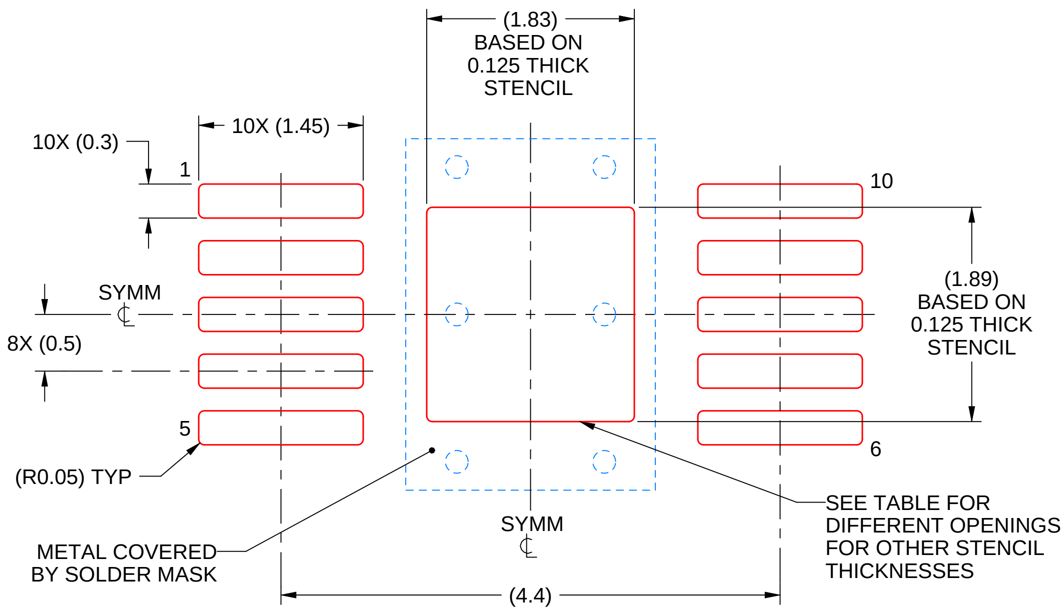


SOLDER MASK DETAILS

4218842/A 01/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.05 X 2.11
0.125	1.83 X 1.89 (SHOWN)
0.150	1.67 X 1.73
0.175	1.55 X 1.60

4218842/A 01/2019

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

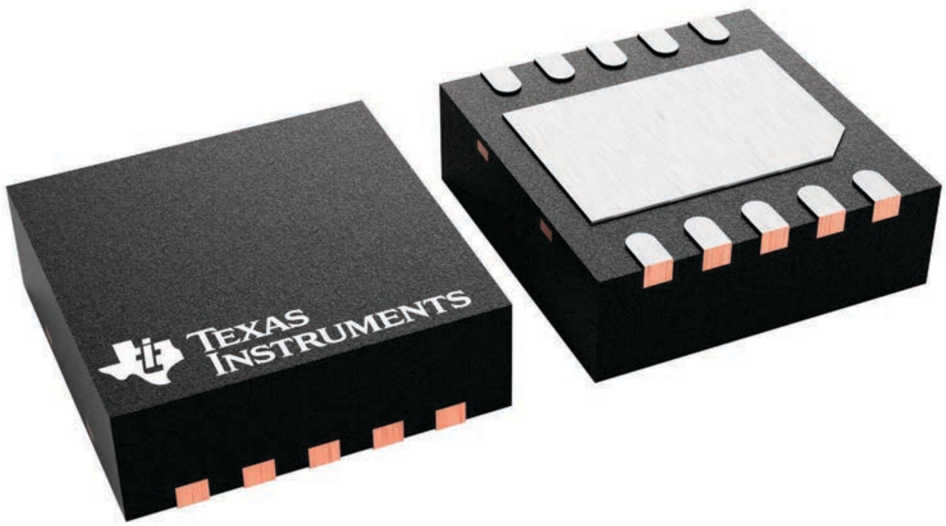
DRC 10

VSON - 1 mm max height

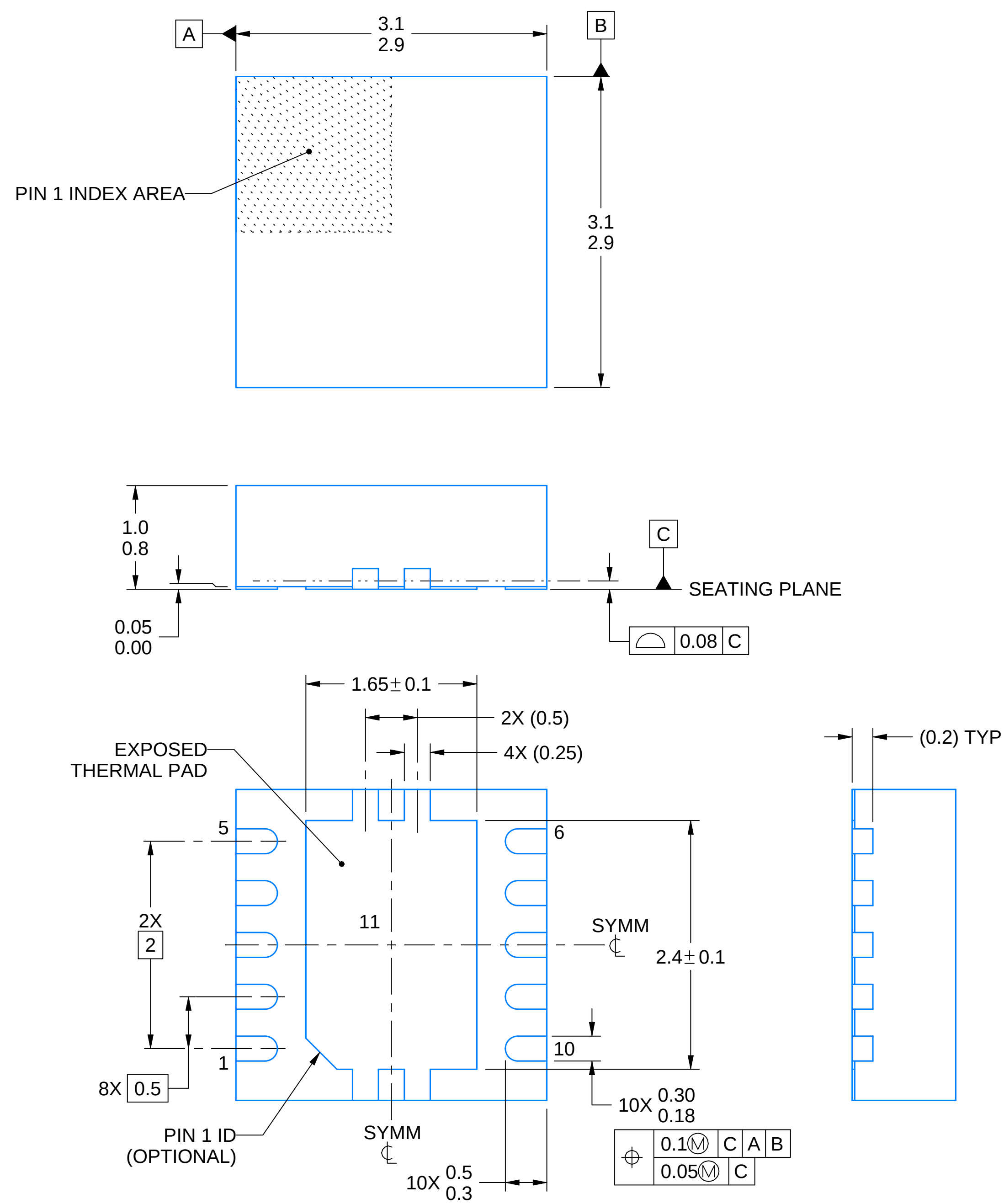
3 x 3, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



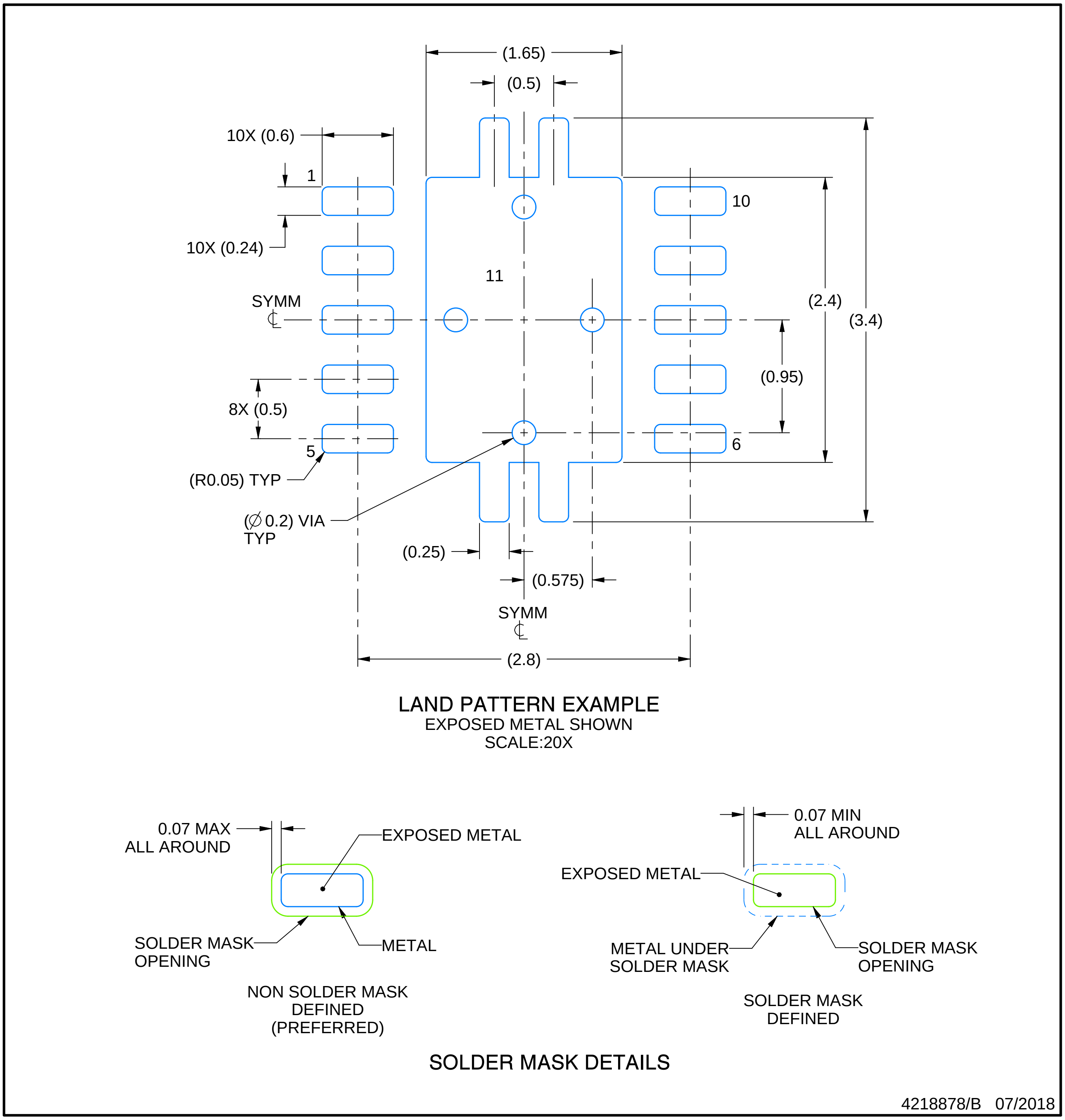
4226193/A



4218878/B 07/2018

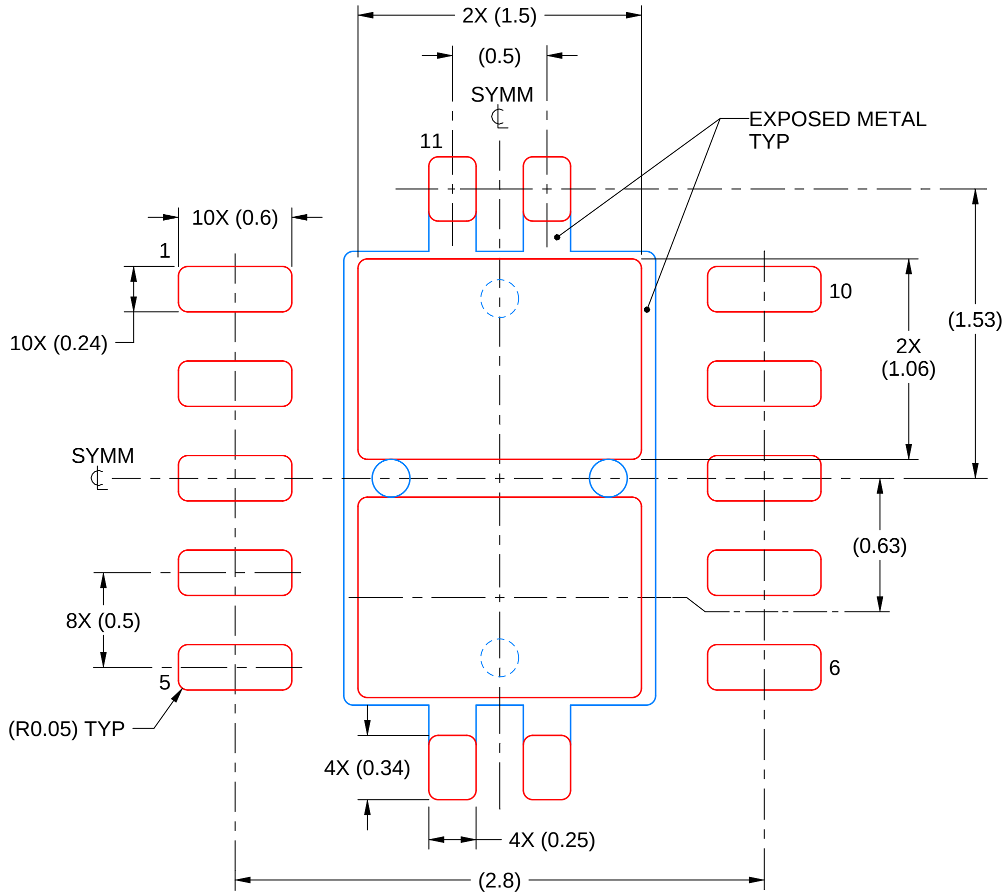
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 11:
80% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4218878/B 07/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.