**Design Note:**

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# Line and System Loopback with the MAX3840

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## 1 Introduction

The MAX3840 dual 2 x 2 asynchronous crosspoint switch is designed for high-speed signals up to 2.7Gbps. A typical application is protection or redundancy switching of clock and data signals for SDH/SONET line termination cards. Due to its low random and deterministic jitter, as well as the small channel-to-channel skew, this device is ideal to support serial data line and system diagnostic loopback in SDH/SONET line termination applications.

## 2 Line and System Loopback

In fiber optic transmission systems, the optical line (the fiber), together with the optical receiver and transmitter, are typically tested using serial line loopback diagnostics. Therefore, the signal must be routed from the receiver directly to the transmitter. To complete this loop, the recovered signals from the Clock and Data Recovery circuit (CDR) must be connected directly to the inputs of the laser driver (LD).

For serial system loopback, the diagnostics will test the system functions independently of the optical receiver and transmitter. In other words the serial clock and output of the multiplexer (MUX) must be connected directly to the inputs of the demultiplexer (DEMUX ).

## 3 Loopback with MAX3840

The MAX3840 provides two independent, 2 x 2 crosspoint switches. This IC can enable the switching of two independent data and clock signals by using one crosspoint switch for the data channels, and the other crosspoint switch for the clock channels.

To provide line and system loopback functions with the MAX3840, a configuration as shown in Figure 1 should be employed. Connect the data output of the MUX to the MAX3840 input DIA0, and the CDR data output to DIA1. Connect the MUX clock output to the MAX3840 input DIB0, and the CDR clock output to DIB1. The data input of the LD should be connected to DOA0, and the LD clock input to DOB0, while the DEMUX data input connects to DOA1 and the DEMUX clock input to DOB1.

For normal operation (no loopback) set all enable pins ENA0/1 and ENB0/1 to high, the routing select pins SELA0/SELB0 to low, and the routing select pins SELA1/SELB1 pins to high. This configures the data path such that the MUX clock and data signals will be routed to the LD, and the DEMUX will receive clock and data signals from the CDR.

Clock and data from the MUX are routed to the DEMUX by setting ENA0/1, ENB0/1, SELA0, and SELB0 to high, and SELA1, SELB1 to low. With these settings, clock and data from the CDR are applied to the LD. Both line and system loop diagnostic tests can be performed at the same time.

If line and system loopback are to be switched separately, the line loopback mode can be activated by setting all select and enable pins to high. In this case the clock and data outputs of the CDR will go to the LD and DEMUX. As a result, during line loopback testing the system can still receive data. If desired, the MAX3840 output, connected to the DEMUX, can be turned off by setting ENA1 and ENB1 to low.

If only the system loopback mode is required, all Select pins are set low and all Enable pins are set high. Analogous to the line loopback mode, the MUX will send data and clock to the LD and DEMUX. If it is not desired to transmit data during the system loop test, the MAX3840 output stages (connected to the LD) can be turned off by setting ENA0 and ENB0 to low.

All MAX3840 high-speed I/O's are CML compatible with on-chip termination. For interfacing to other standards, please refer to the Maxim application note, HFAN-1.0, Introduction to LVDS, PECL and CML. The MAX3840 is available in a 5mm x 5mm 32 Pin QFN package, minimizing the required board space to implement the loopback functions.

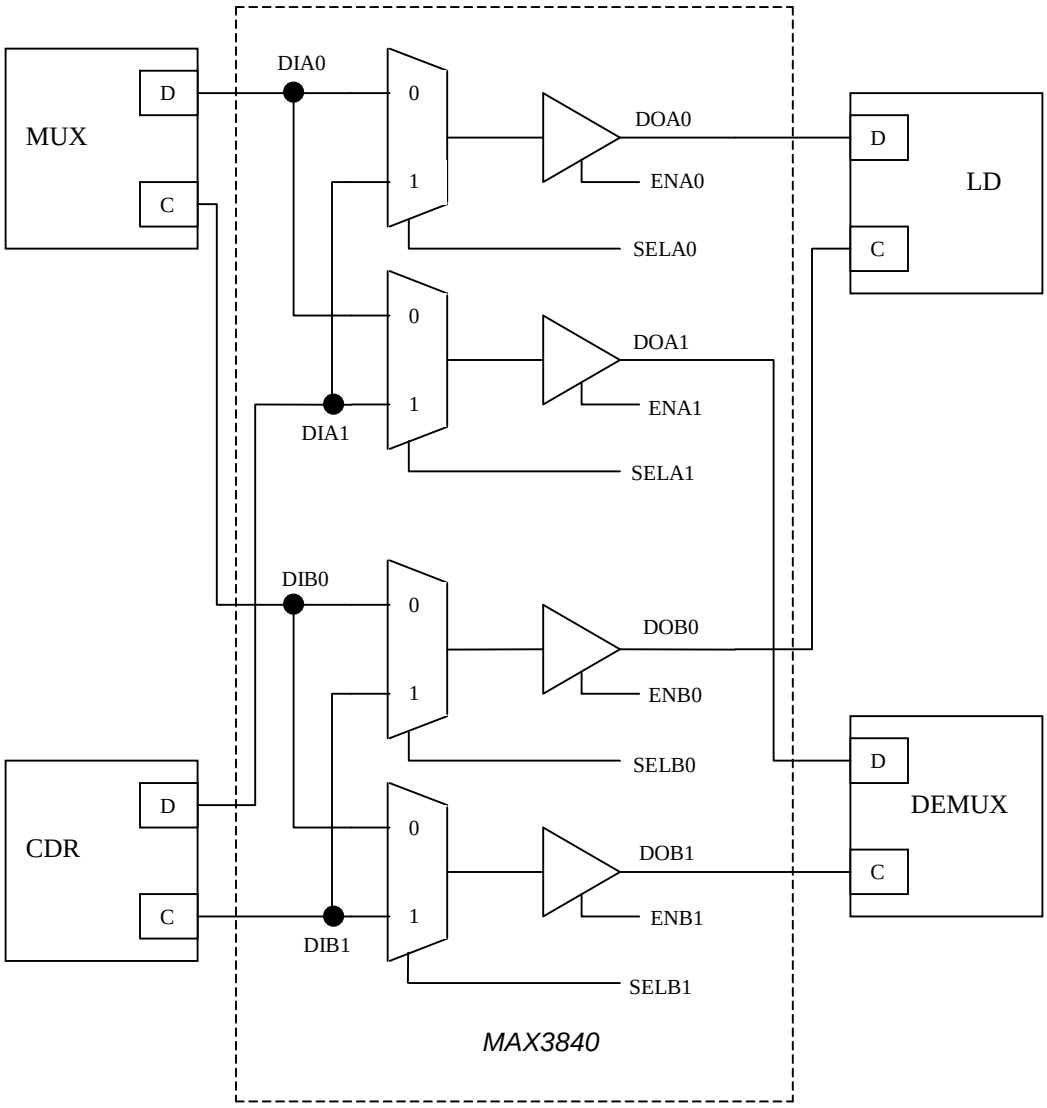


*Figure 1. Line and system loopback with the MAX3840 for line termination applications*