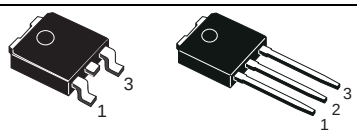
VND5N07-E

OMNIFET II
fully autoprotected Power MOSFET

Datasheet - production data



DPAK
TO-252

IPAK
TO-251

Features

Max. on-state resistance (per ch.)	$R_{DS\ (on)}$	0.2Ω
Current limitation (typ)	I_{LIMH}	5 A
Drain-Source clamp voltage	V_{CLAMP}	70V

- Linear current limitation
- Thermal shutdown
- Short circuit protection
- Integrated clamp
- Low current drawn from input pin
- Diagnostic feedback through input pin
- ESD protection
- Direct access to the gate of the power mosfet (analog driving)
- Compatible with standard Power MOSFET

Description

The VND5N07-E is a monolithic device designed using STMicroelectronics® VIPower® M0 technology, intended for replacement of standard Power MOSFETs from DC to 50 KHz applications. Built-in thermal shutdown, linear current limitation and overvoltage clamp protect the chip in harsh environments.

Fault feedback can be detected by monitoring the voltage at the input pin.

Table 1. Device summary

Package	Order codes	
	Tube	Tape and reel
DPAK	VND5N07-E	VND5N07TR-E
IPAK	VND5N07-1-E	

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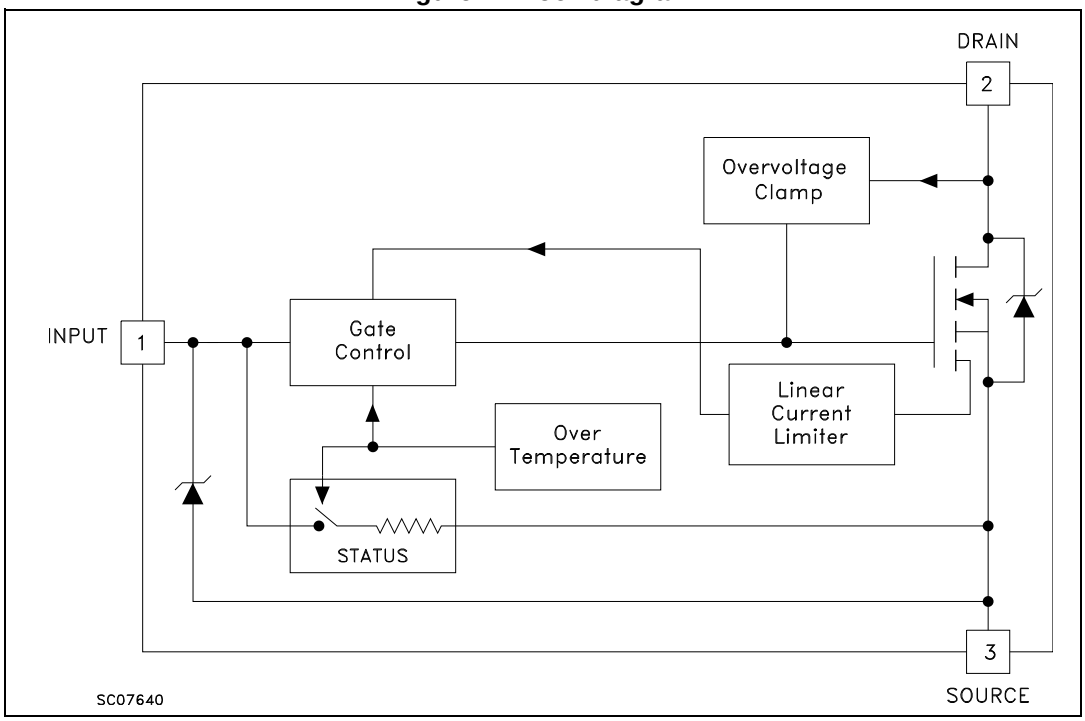
1 Block diagram and pin description

Figure 1. Block diagram



2 Electrical specifications

2.1 Absolute maximum ratings

Stressing the device above the rating listed in *Table 2* may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to Absolute maximum rating conditions for extended periods may affect device reliability.

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DSn}	Drain-Source voltage (V_{INn} = 0 V)	Internally clamped	V
V_{INn}	Input voltage	18	V
I_{Dn}	Drain current	Internally limited	A
I_{Rn}	Reverse DC output current	-7	A
V_{ESD}	Electrostatic discharge (R = 1.5 KΩ, C = 100 pF)	2000	V
P_{tot}	Total dissipation at T_c = 25°C	60	W
T_j	Operating junction temperature	Internally limited	°C
T_c	Case operating temperature	Internally limited	°C
T_{stg}	Storage temperature	-55 to 150	°C

2.2 Thermal data

Table 3. Thermal data

Symbol	Parameter	Max. value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case	3.75	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient	100	°C/W

2.3 Electrical characteristics

T_{case} = 25 °C unless otherwise stated.

Table 4. Off

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{CLAMP}	Drain-Source clamp voltage	V_{IN} = 0 V; I_D = 200 mA	60	70	80	V
V_{CLTH}	Drain-Source threshold voltage	V_{IN} = 0 V; I_D = 2 mA	55			V
I_{ISS}	Supply current from input pin	V_{DS} = 0 V; V_{IN} = 10 V		250	500	µA
V_{INCL}	Input-Source reverse clamp voltage	I_{IN} = 1 mA	-1.0		-0.3	V
I_{DSS}	Zero input voltage drain current (V_{IN} = 0 V)	V_{DS} = 13 V; V_{IN} = 0 V			50	µA
		V_{DS} = 25 V; V_{IN} = 0 V			200	µA

Table 5. On(1)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$R_{DS(on)}$	Static drain-source on resistance	V_{IN} =10 V; I_D = 2.5 A			200	mΩ
		V_{IN} = 5 V; I_D = 2.5 A			280	mΩ
$V_{IN(th)}$	Input threshold voltage	V_{DS} = V_{in}; I_D + I_{in} = 1 mA	0.8		3	V

1. Pulsed: pulse duration = 300 µs, duty cycle 1.5%.

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
g_{fs} (1)	Forward transconductance	V_{DS} = 13 V; I_D = 2.5 A	3	4		S
C_{OSS}	Output capacitance	V_{DS} = 13 V; f = 1 MHz; V_{IN} = 0 V		200	300	pF

1. Pulsed: pulse duration = 300µs, duty cycle 1.5%.

Table 7. Switching(1)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 15 V; I_D = 2.5 A; V_{gen} = 10 V; R_{gen} = 10 Ω		50	100	ns
t_r	Rise time			60	100	ns
$t_{d(off)}$	Turn-off delay time			150	300	ns
t_f	Fall time			40	80	ns

Table 7. Switching(1)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 15 V; I_D = 2.5 A; V_{gen} = 10 V; R_{gen} = 1 kΩ		150	250	ns
t_r	Rise time			400	600	ns
$t_{d(off)}$	Turn-off delay time			3900	5000	ns
t_f	Fall time			1100	1600	ns
$(dI/dt)_{on}$	Turn-on current slope	V_{DD} = 15 V; I_D = 2.5 A; V_{in} = 10 V; R_{gen} = 10 Ω		80		A/µS
Q_i	Total input charge	V_{DD} = 12 V; I_D = 2.5 A; V_{IN} = 10 V		18		nC

1. Parameters guaranteed by design / characterization.

Table 8. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{SD}(1)	Forward on voltage	I_{SD} = 2.5 A; V_{IN} = 0 V			1.6	V
t_{rr}(2)	Reverse recovery time	I_{SD} = 2.5 A; dI/dt = 100 A/µs; V_{DD} = 30 V		150		ns
Q_{rr} (2)	Reverse recovery charge			0.3		µC
I_{RRM}(2)	Reverse recovery current			5.7		A

1. Pulsed: pulse duration = 300µs, duty cycle 1.5%.
2. Parameters guaranteed by design / characterization.

Table 9. Protections (-40°C < T_j < 150°C, unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{lim}	Drain current limit	V_{IN} = 10 V; V_{DS} = 13 V	3.5	5	7	A
		V_{IN} = 5 V; V_{DS} = 13 V	3.5	5	7	A
t_{dlim} (1)	Step response current limit	V_{IN} = 10 V		15	20	µS
		V_{IN} = 5 V		40	60	µS
T_{jsh} (1)	Overtemperature shutdown		150			°C
T_{jrs}(1)	Overtemperature reset		135			°C
I_{gf}(1)	Fault sink current	V_{IN} = 10 V; V_{DS} = 13 V		50		mA
		V_{IN} = 5 V; V_{DS} = 13 V		20		mA
E_{as} (1)	Single pulse avalanche energy	Starting T_j = 25°C; V_{DD} = 20 V; V_{IN} = 10 V; R_{gen} = 1 kΩ; L = 10 mH	0.2			J

1. Parameters guaranteed by design / characterization.

Figure 2. Switching time test circuit for resistive load

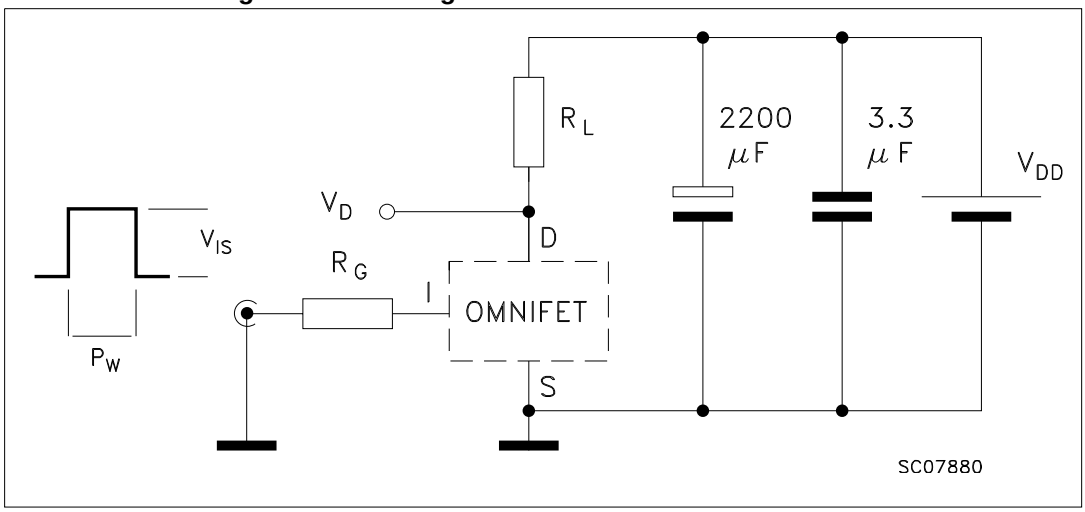


Figure 3. Test circuit for diode recovery times

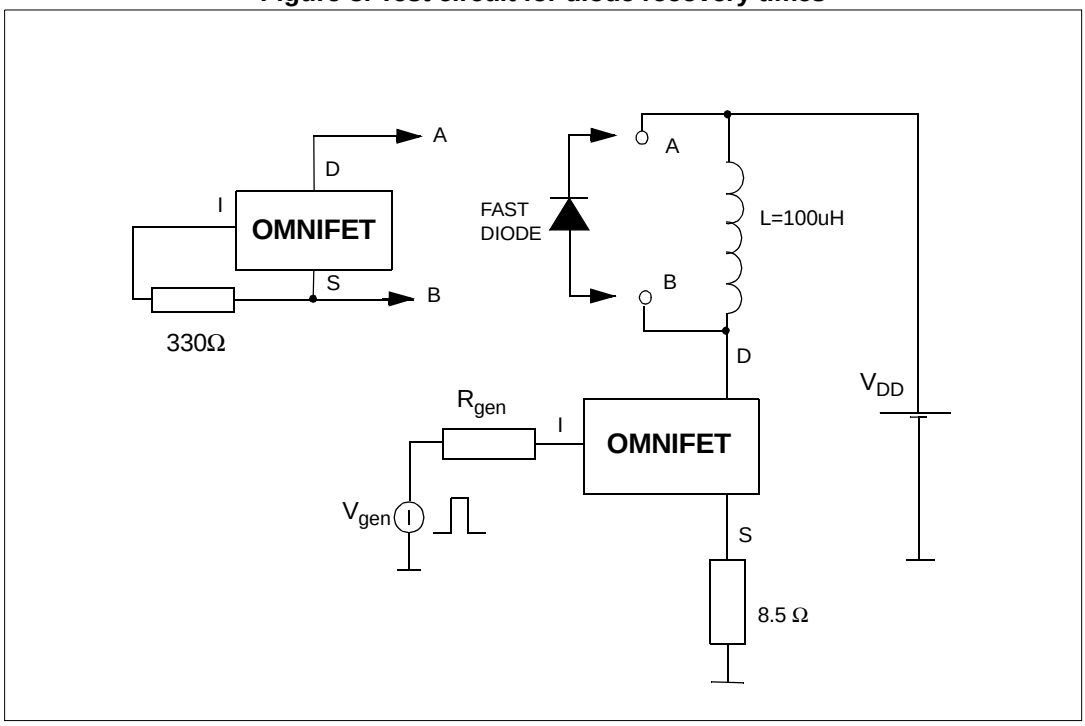


Figure 4. Unclamped inductive load test circuits

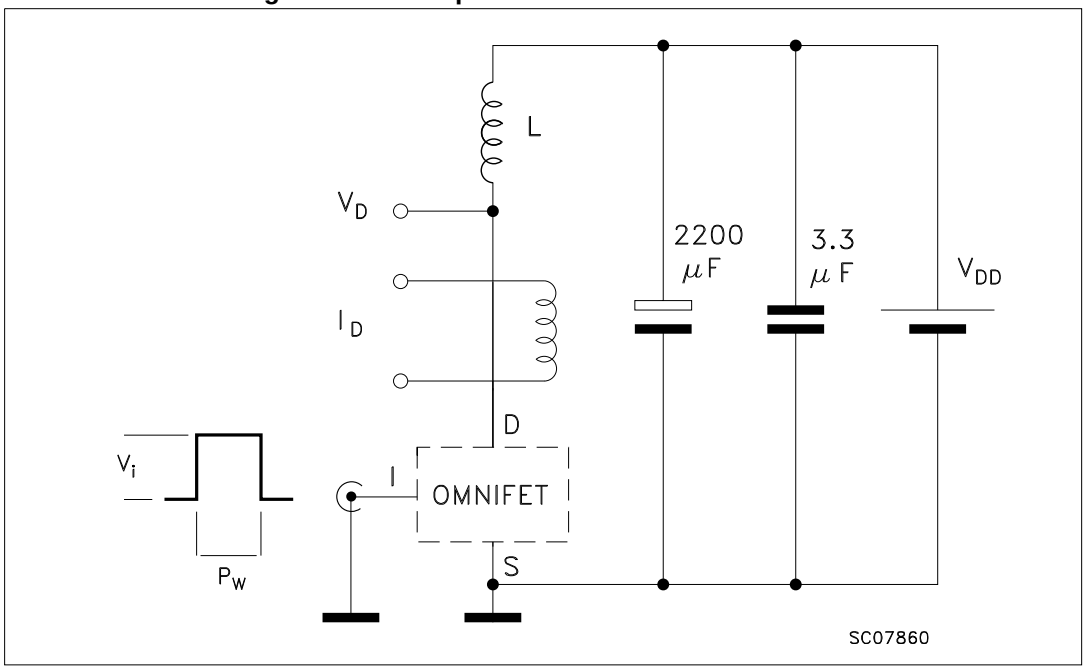


Figure 5. Input charge test circuit

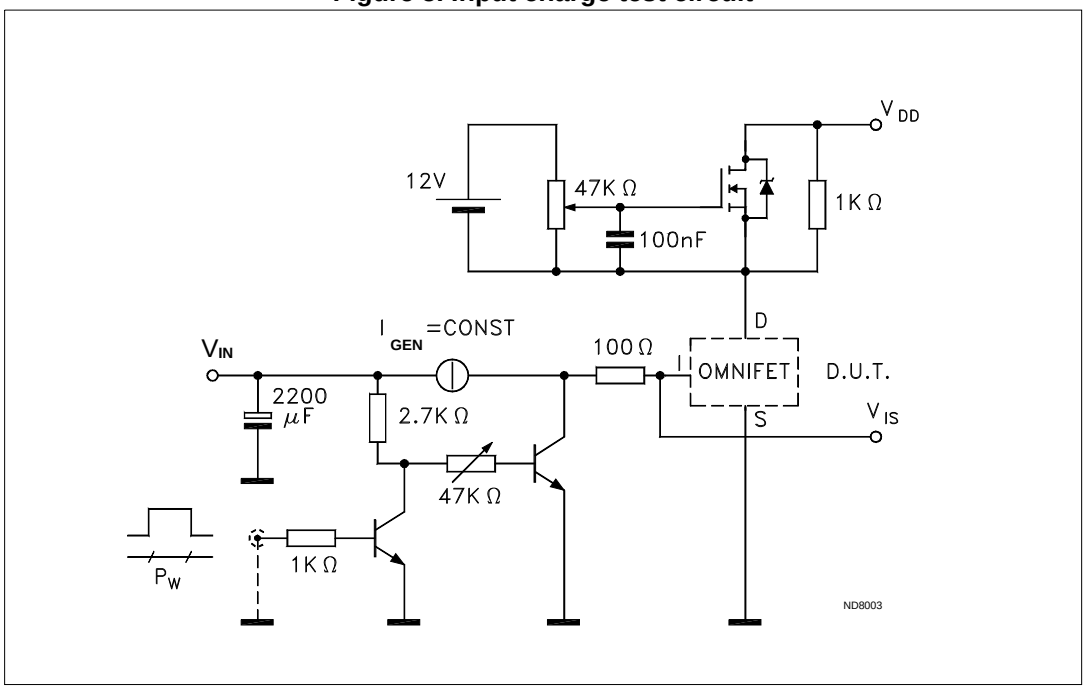


Figure 6. Unclamped inductive waveforms

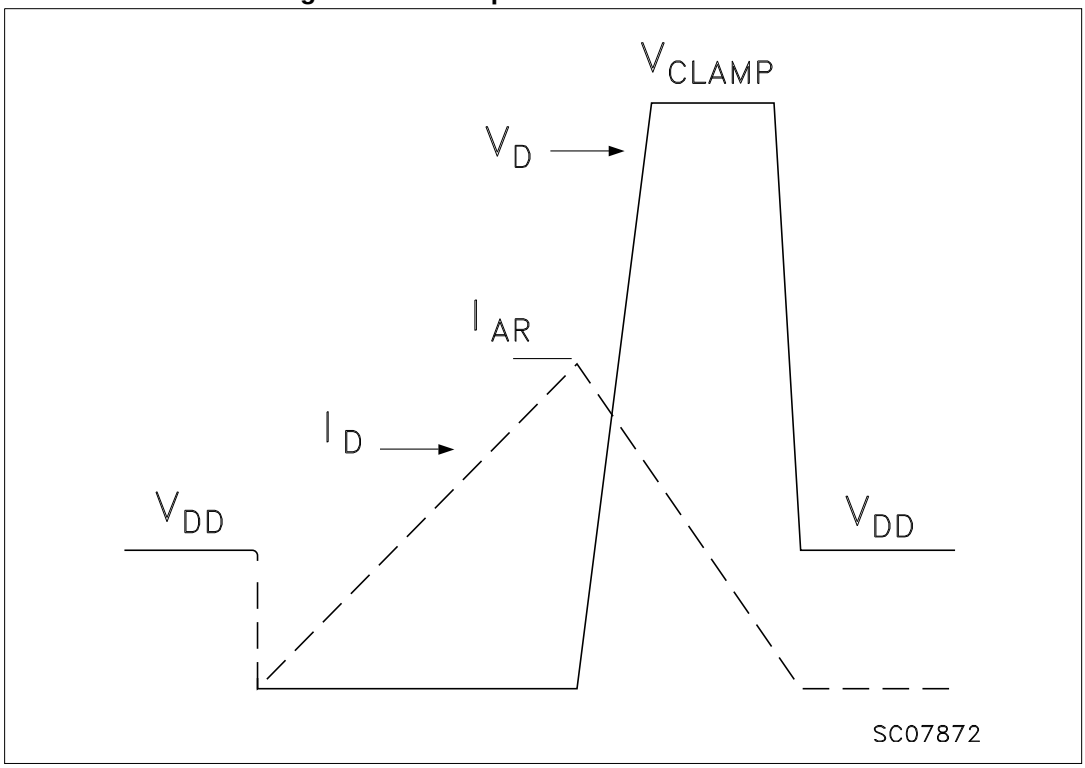


Figure 7. Switching waveforms

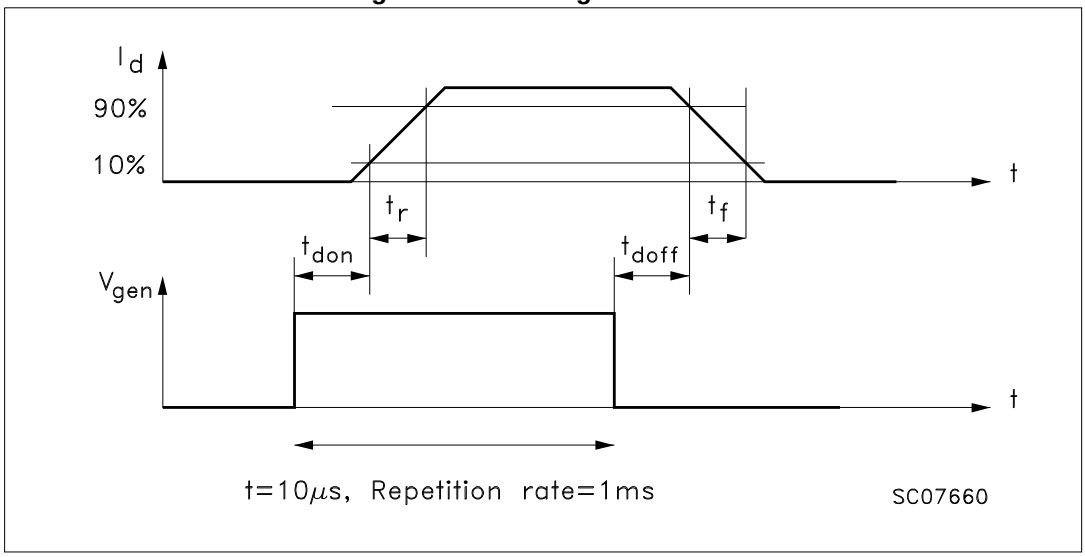
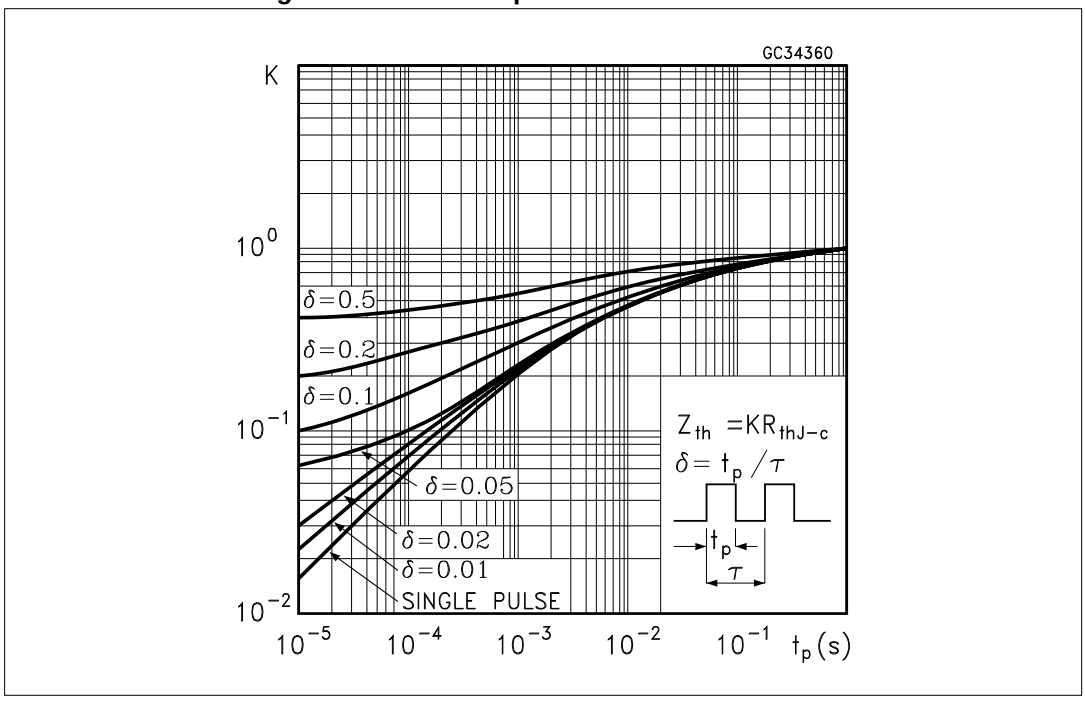


Figure 8. Thermal impedance for DPAK / IPAK



2.4 Electrical characteristics curves

Figure 9. Source-drain diode forward characteristics

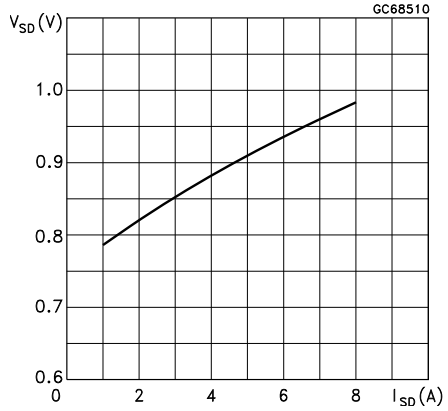


Figure 10. Static drain-source on resistance

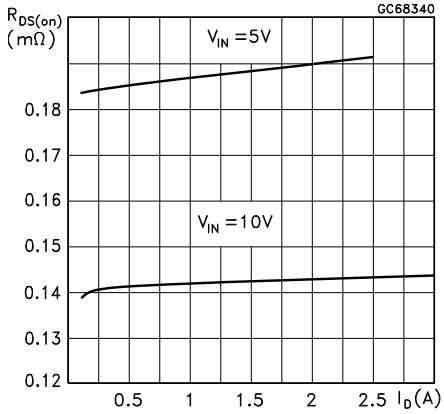


Figure 11. Derating curve

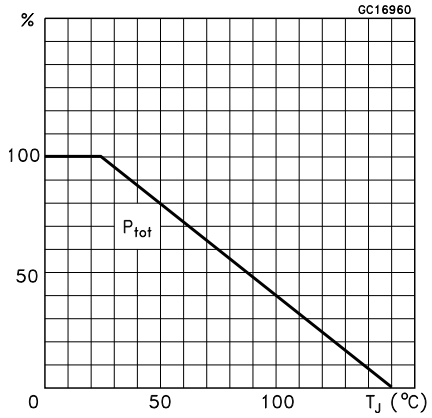


Figure 12. Static drain-source on resistance vs. input voltage

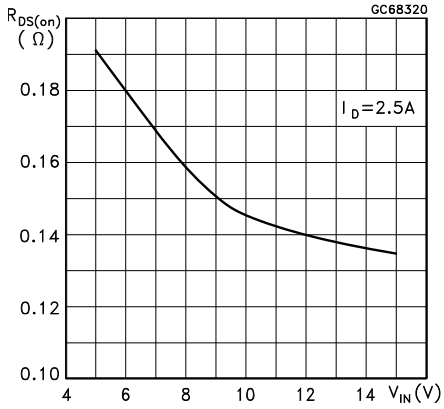


Figure 13. Normalized on resistance Vs temperature

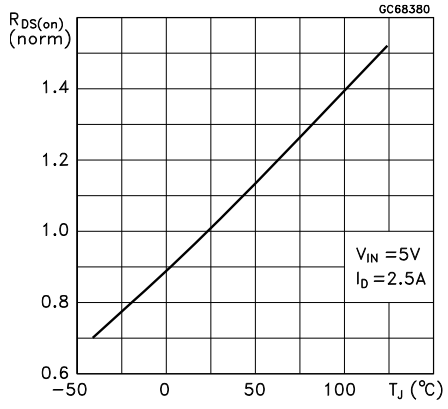


Figure 14. Transconductance

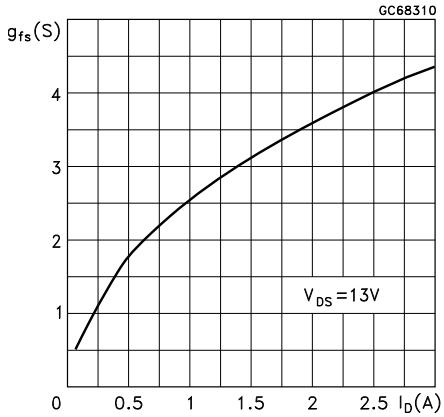


Figure 15. Static drain-source on resistance Vs. Id

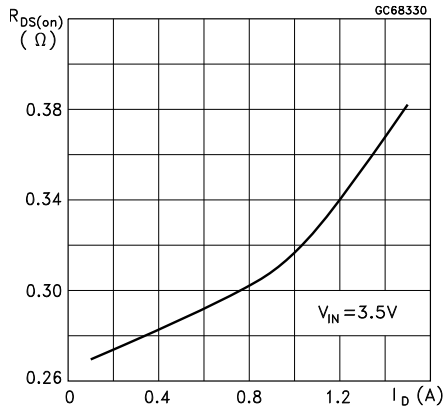


Figure 16. Switching time resistive load

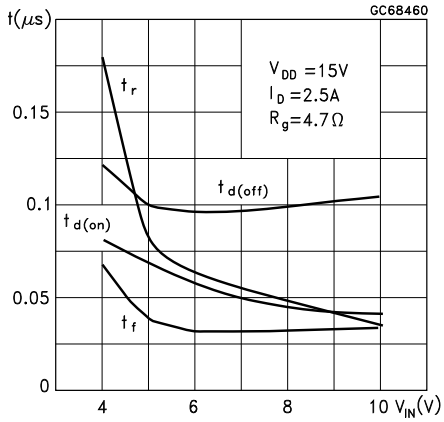


Figure 17. Turn-on current slope (V_{IN} = 10 V)

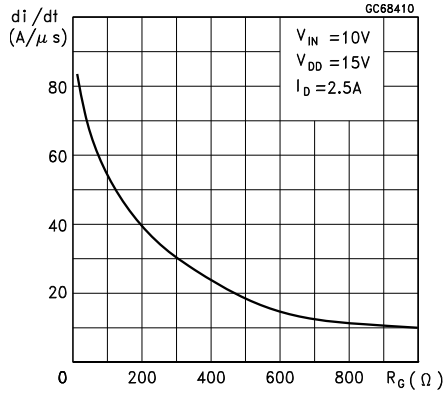


Figure 18. Turn-on current slope (V_{IN} = 5 V)

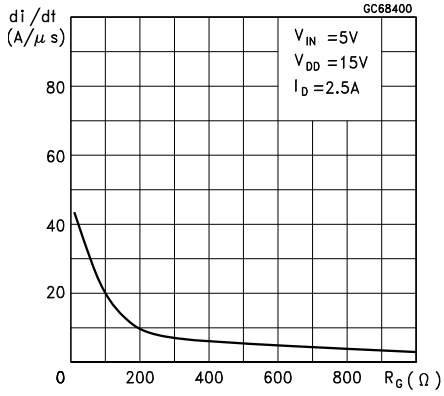


Figure 19. Input voltage vs. input charge

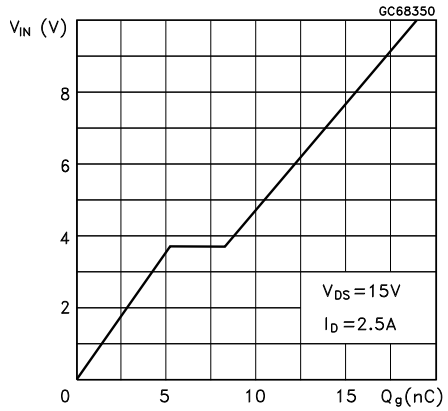


Figure 20. Turn-off drain source voltage slope

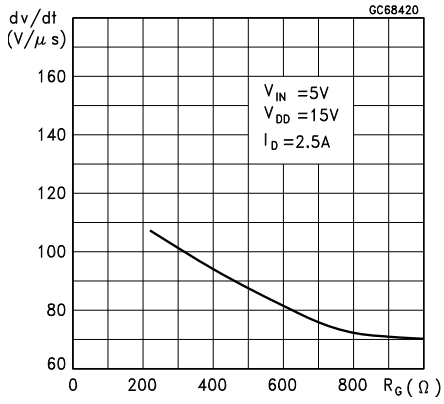


Figure 21. Turn-off drain-source voltage slope

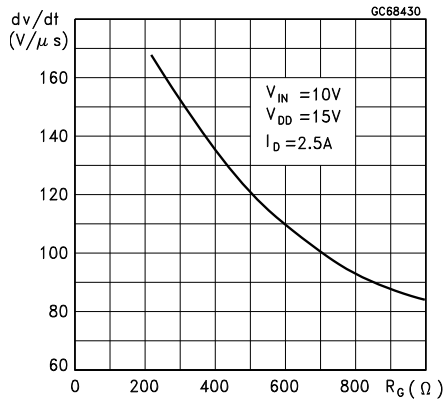


Figure 22. Capacitance variations

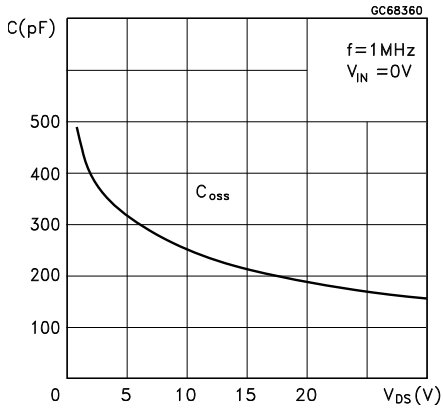


Figure 23. Switching time resistive load

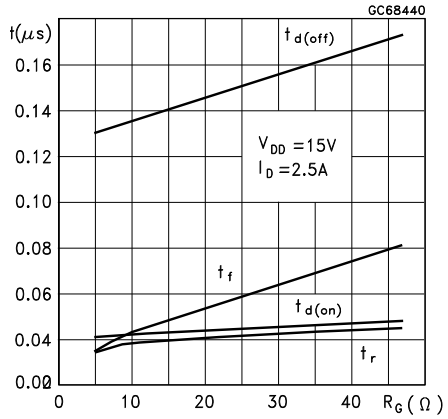


Figure 24. Step response current limit

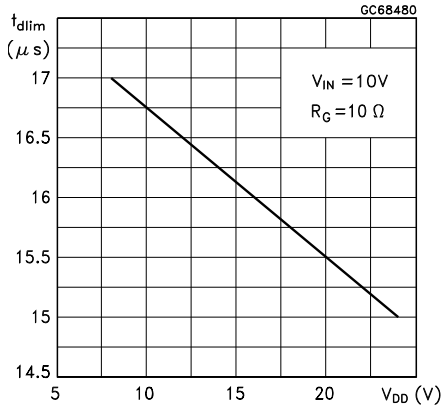


Figure 25. Output characteristics

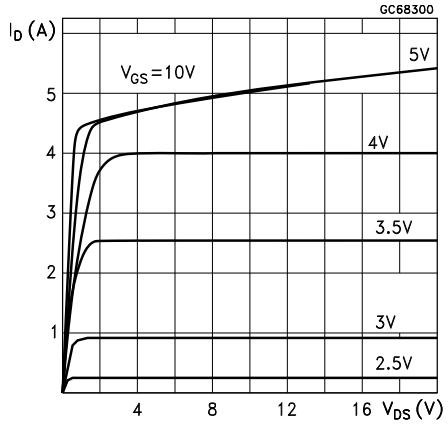


Figure 26. Normalized on resistance vs. temperature

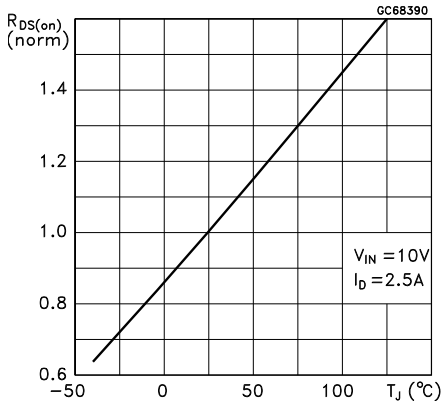


Figure 27. Normalized input threshold voltage vs. temperature

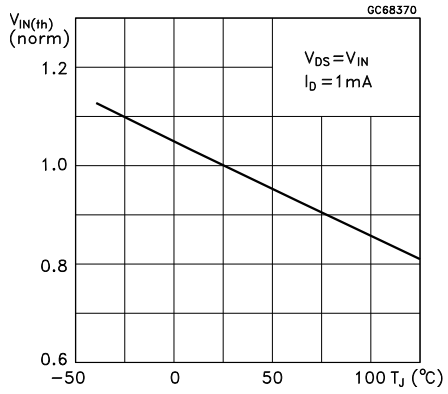
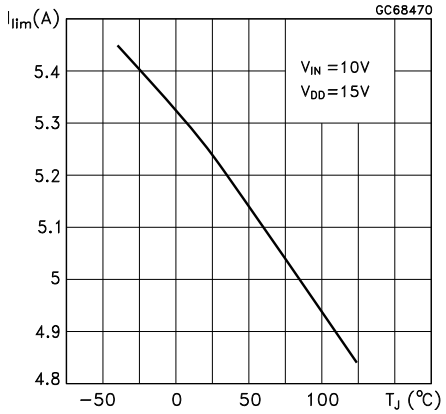


Figure 28. Normalized current limit vs. junction temperature



3 Protection features

During normal operation, the INPUT pin is electrically connected to the gate of the internal Power MOSFET.

The device then behaves like a standard Power MOSFET and can be used as a switch from DC to 50KHz. The only difference from the user's standpoint is that a small DC current I_{ISS} flows into the INPUT pin in order to supply the internal circuitry.

The device integrates:

3.1 Overvoltage clamp protection

Internally set at 70 V, along with the rugged avalanche characteristics of the Power MOSFET stage give this device unrivaled ruggedness and energy handling capability. This feature is mainly important when driving inductive loads.

3.2 Linear current limiter circuit

Limits the drain current I_D to I_{lim} whatever the INPUT pin voltages. When the current limiter is active, the device operates in the linear region, so power dissipation may exceed the capability of the heatsink. Both case and junction temperatures increase, and if this phase lasts long enough, junction temperature may reach the overtemperature threshold T_{jsh}.

3.3 Overtemperature and short circuit protection

These are based on sensing the chip temperature and are not dependent on the input voltage. The location of the sensing element on the chip in the power stage area ensures fast, accurate detection of the junction temperature. Overtemperature cutout occurs at minimum 150 °C. The device is automatically restarted when the chip temperature falls below 135 °C.

3.4 Status feedback

In case of an overtemperature fault condition, a Status Feedback is provided through the Input pin. The internal protection circuit disconnects the input from the gate and connects it instead to ground via an equivalent resistance of 100 Ω. The failure can be detected by monitoring the voltage at the Input pin, which will be close to ground potential.

Additional features of this device are ESD protection according to the Human Body model and the ability to be driven from a TTL Logic circuit (with a small increase in $R_{DS(on)}$).

4 Package and packing information

4.1 ECOPACK® packages

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.2 DPAK mechanical data

Figure 29. DPAK package dimensions

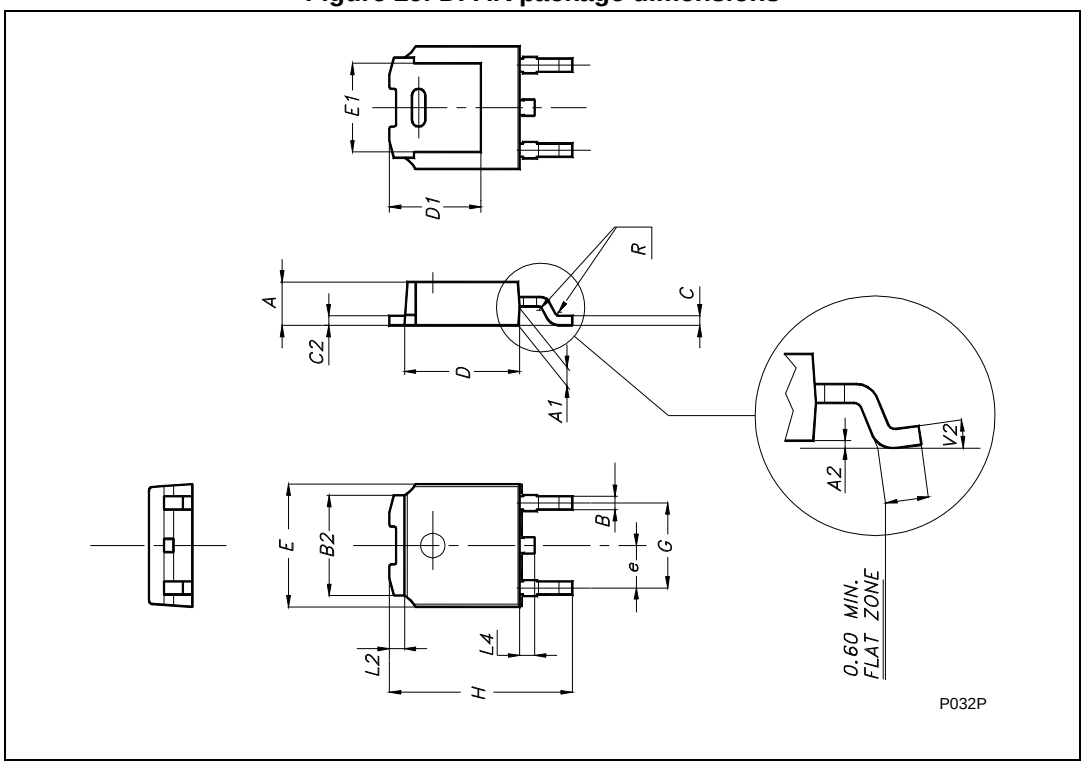


Table 10. DPAK mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
B	0.64		0.90
B2	5.20		5.40
C	0.45		0.60
C2	0.48		0.60
D	6.00		6.20
D1		5.1	
E	6.40		6.60
E1		4.7	
e		2.28	
G	4.40		4.60
H	9.35		10.10
L2		0.8	
L4	0.60		1.00
R		0.2	
V2	0°	8°	
Package weight	Gr. 0.29		

4.3 IPAK mechanical data

Figure 30. IPAK mechanical data and package outline

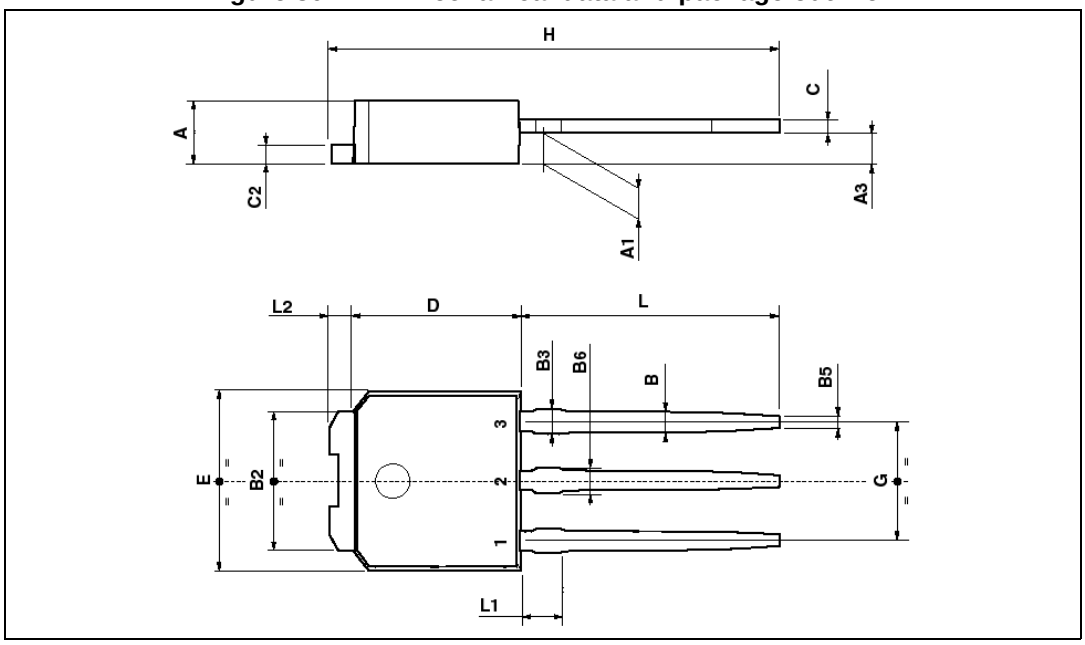


Table 11. IPAK mechanical data

Symbol	mm		
	Min.	Typ.	Max.
A	2.2		2.4
A1	0.9		1.1
A3	0.7		1.3
B	0.64		0.9
B2	5.2		5.4
B3			0.85
B5		0.3	
B6			0.95
C	0.45		0.6
C2	0.48		0.6
D	6		6.2
E	6.4		6.6
G	4.4		4.6
H	15.9		16.3
L	9		9.4
L1	0.8		1.2
L2		0.8	1

5 Revision history

Table 12. Document revision history

Date	Revision	Changes
01-Aug-2013	1	Initial release.
16-Sep-2013	2	Updated disclaimer.

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