ARM® Cortex®-M0

32-bit Microcontroller

NuMicro® Family
NUC123 Series
Datasheet

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1 GENERAL DESCRIPTION

The NuMicro® NUC123 series is a new 32-bit Cortex®-M0 microcontroller with USB 2.0 Full-speed devices and a 10-bit ADC. The NUC123 series provides the high 72 MHz operating speed, large 20 Kbytes SRAM, 8 USB endpoints and three sets of SPI controllers, which make it powerful in USB communication and data processing. The NUC123 series is ideal for industrial control, consumer electronics, and communication system applications such as printers, touch panel, gaming keyboard, gaming joystick, USB audio, PC peripherals, and alarm systems.

The NUC123 series runs up to 72 MHz and supports 32-bit multiplier, structure NVIC (Nested Vector Interrupt Control), dual-channel APB and PDMA (Peripheral Direct Memory Access) with CRC function. Besides, the NUC123 series is equipped with 36/68 Kbytes Flash memory, 12/20 Kbytes SRAM, and 4 Kbytes loader ROM for the ISP. It operates at a wide voltage range of 2.5V ~ 5.5V and temperature range of -40°C ~ +105°C and -40°C ~ +85°C. It is also equipped with plenty of peripheral devices, such as 8-channel 10-bit ADC, UART, SPI, I^2C, I^2S, USB 2.0 FS devices, and offers low-voltage reset and Brown-out detection, PWM (Pulse-width Modulation), capture and compare features, four sets of 32-bit timers, Watchdog Timer, and internal RC oscillator. All these peripherals have been incorporated into the NUC123 series to reduce component count, board space and system cost.

Additionally, the NUC123 series is equipped with ISP (In-System Programming), IAP (In-Application-Programming) and ICP (In-Circuit Programming) functions, which allows the user to update the program under software control through the on-chip connectivity interface, such as SWD, UART and USB.

Product Line	UART	SPI	I^2C	USB	PS/2	I^2S	PWM	ADC
NUC123	2	3	2	1	1	1	4	8

Table 1-1 Key Features Support Table

2 FEATURES

2.1 NuMicro® NUC123 Series Features

- Core
  - ARM® Cortex®-M0 core runs up to 72 MHz
  - One 24-bit system timer
  - Supports low power sleep mode
  - Single-cycle 32-bit hardware multiplier
  - NVIC for the 32 interrupt inputs, each with 4-levels of priority
  - Supports Serial Wire Debug with 2 watchpoints/4 breakpoints
- Built-in LDO for wide operating voltage ranges from 2.5 V to 5.5 V
- Flash Memory
  - 36/68 KB Flash for program code
  - 4 KB flash for ISP loader
  - Supports In-System Program (ISP) application code update
  - 512 byte page erase for flash
  - Configurable Data Flash address and size for both 36KB and 68KB system
  - Supports 2-wire ICP update through SWD/ICE interface
  - Supports fast parallel programming mode by external programmer
- SRAM Memory
  - 12/20 KB embedded SRAM
  - Supports PDMA mode
- PDMA (Peripheral DMA)
  - Supports 6 channels PDMA for automatic data transfer between SRAM and peripherals such as SPI, UART, I^2S, USB 2.0 FS device, PWM and ADC
  - Supports CRC calculation with four common polynomials, CRC-CCITT, CRC-8, CRC-16 and CRC-32
- Clock Control
  - Flexible selection for different applications
  - Built-in 22.1184 MHz high speed oscillator (Trimmed to 1%) for system operation, and low power 10 kHz low speed oscillator for watchdog and wake-up operation
  - Supports one PLL, up to 144 MHz, for high performance system operation
  - External 4~24 MHz high speed crystal input for precise timing operation
- GPIO
  - Four I/O modes:
    - Quasi bi-direction
    - Push-Pull output
    - Open-Drain output
    - Input only with high impendence
  - TTL/Schmitt trigger input selectable
  - I/O pin configured as interrupt source with edge/level setting
  - Supports High Driver and High Sink I/O mode
- Timer
  - Supports 4 sets of 32-bit timers with 24-bit up-timer and one 8-bit pre-scale counter
  - Independent clock source for each timer
  - Provides one-shot, periodic, toggle and continuous counting operation modes
  - Supports event counting function
- Watchdog/Windowed-Watchdog Timer
  - Multiple clock sources

- 8 selectable time-out period from 1.6ms ~ 26.0sec (depending on clock source)
- Wake-up from Power-down or Idle mode
- Interrupt or reset selectable on watchdog timer time-out
- Interrupt on windowed-watchdog timer time-out
- Reset on windowed-watchdog timer time-out or reload in an unexpected time window

- PWM/Capture
  - Up to two built-in 16-bit PWM generators provided with four PWM outputs or two complementary paired PWM outputs
  - Each PWM generator equipped with one clock source selector, one clock divider, one 8-bit prescaler and one Dead-zone generator for complementary paired PWM
  - Up to four 16-bit digital Capture timers (shared with PWM timers) provided with four rising/falling capture inputs
  - Supports Capture interrupt
- UART
  - Up to two UART controllers
  - UART ports with flow control (TXD, RXD, CTS and RTS)
  - UART0/1 with 16-byte FIFO for standard device
  - Support IrDA (SIR) function
  - Supports RS-485 9-bit mode and direction control.
  - Programmable baud-rate generator up to 1/16 system clock
  - Supports PDMA mode
- SPI
  - Up to three sets of SPI controllers
  - Supports SPI master/Slave mode
  - Full duplex synchronous serial data transfer
  - Variable length of transfer data from 8 to 32 bits
  - MSB or LSB first data transfer
  - Up to two slave/device select lines in Master mode
  - Supports Byte Suspend mode in 16/24/32-bit transmission
  - Supports PDMA transfer
- I^2C
  - Up to two sets of I^2C devices
  - Master/Slave mode
  - Bidirectional data transfer between masters and slaves
  - Multi-master bus (no central master)
  - Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
  - Serial clock synchronization allows devices with different bit rates to communicate via one serial bus
  - Serial clock synchronization used as a handshake mechanism to suspend and resume serial transfer
  - Programmable clocks allowing versatile rate control
  - Supports multiple address recognition (four slave address with mask option)
  - Supports wake-up by address recognition (for 1st slave address only)
- I^2S
  - Interface with external audio CODEC
  - Operated as either master or Slave mode
  - Capable of handling 8-, 16-, 24- and 32-bit word sizes
  - Supports Mono and stereo audio data
  - Supports I^2S and MSB justified data format
  - Two 8 word FIFO data buffers are provided, one for transmitting and the other for receiving

  - Generates interrupt requests when buffer levels cross a programmable boundary
  - Supports two DMA requests, one for transmitting and the other for receiving
- PS/2 Device Controller
  - Host communication inhibit and request to send detection
  - Reception frame error detection
  - Programmable 1 to 16 bytes transmit buffer to reduce CPU intervention
  - Double buffer for data reception
  - S/W override bus
- USB 2.0 Full-Speed Device
  - One set of USB 2.0 FS Device 12 Mbps
  - On-chip USB transceiver
  - Provides 1 interrupt source with 4 interrupt events
  - Supports Control, Bulk In/Out, Interrupt and Isochronous transfers
  - Auto suspend function when no bus signaling for 3 ms
  - Provides 8 programmable endpoints
  - Includes 512 bytes internal SRAM as USB buffer
  - Provides remote wake-up capability
- ADC
  - 10-bit SAR ADC with 150K SPS (for NUC123xxxANx)
  - 10-bit SAR ADC with 200K SPS (for NUC123xxxAEx)
  - Up to 8-ch single-end input
  - Single scan/single cycle scan/continuous scan
  - Each channel with individual result register
  - Scan on enabled channels
  - Threshold voltage detection
  - Conversion start by software programming or external input
  - Supports PDMA mode
- Brown-out detector
  - With 4 levels: 4.4 V/3.7 V/2.7 V/2.2 V
  - Supports Brown-out Interrupt and Reset option
- Low Voltage Reset
  - Threshold voltage levels: 2.0 V
- One built-in LDO
- Operating Temperature: -40°C~85°C (for NUC123xxxANx)
- Operating Temperature: -40°C~105°C (for NUC123xxxAEx)
- Packages:
  - All Green package (RoHS)
  - LQFP 64-pin
  - LQFP 48-pin
  - QFN 33-pin

3 ABBREVIATIONS

Acronym	Description
ACMP	Analog Comparator Controller
ADC	Analog-to-Digital Converter
AES	Advanced Encryption Standard
APB	Advanced Peripheral Bus
AHB	Advanced High-Performance Bus
BOD	Brown-out Detection
CAN	Controller Area Network
DAP	Debug Access Port
DES	Data Encryption Standard
EBI	External Bus Interface
EPWM	Enhanced Pulse Width Modulation
FIFO	First In, First Out
FMC	Flash Memory Controller
FPU	Floating-point Unit
GPIO	General-Purpose Input/Output
HCLK	The Clock of Advanced High-Performance Bus
HIRC	22.1184 MHz Internal High Speed RC Oscillator
HXT	4~20 MHz External High Speed Crystal Oscillator
IAP	In Application Programming
ICP	In Circuit Programming
ISP	In System Programming
LDO	Low Dropout Regulator
LIN	Local Interconnect Network
LIRC	10 kHz internal low speed RC oscillator (LIRC)
MPU	Memory Protection Unit
NVIC	Nested Vectored Interrupt Controller
PCLK	The Clock of Advanced Peripheral Bus
PDMA	Peripheral Direct Memory Access
PLL	Phase-Locked Loop
PWM	Pulse Width Modulation
QEI	Quadrature Encoder Interface
SD	Secure Digital
SPI	Serial Peripheral Interface

SPS	Samples per Second
TDES	Triple Data Encryption Standard
TK	Touch Key
TMR	Timer Controller
UART	Universal Asynchronous Receiver/Transmitter
UCID	Unique Customer ID
USB	Universal Serial Bus
WDT	Watchdog Timer
WWDT	Window Watchdog Timer

Table 3-1 List of Abbreviations

4 PARTS INFORMATION LIST AND PIN CONFIGURATION

4.1 NuMicro® NUC123 Series Naming Rule

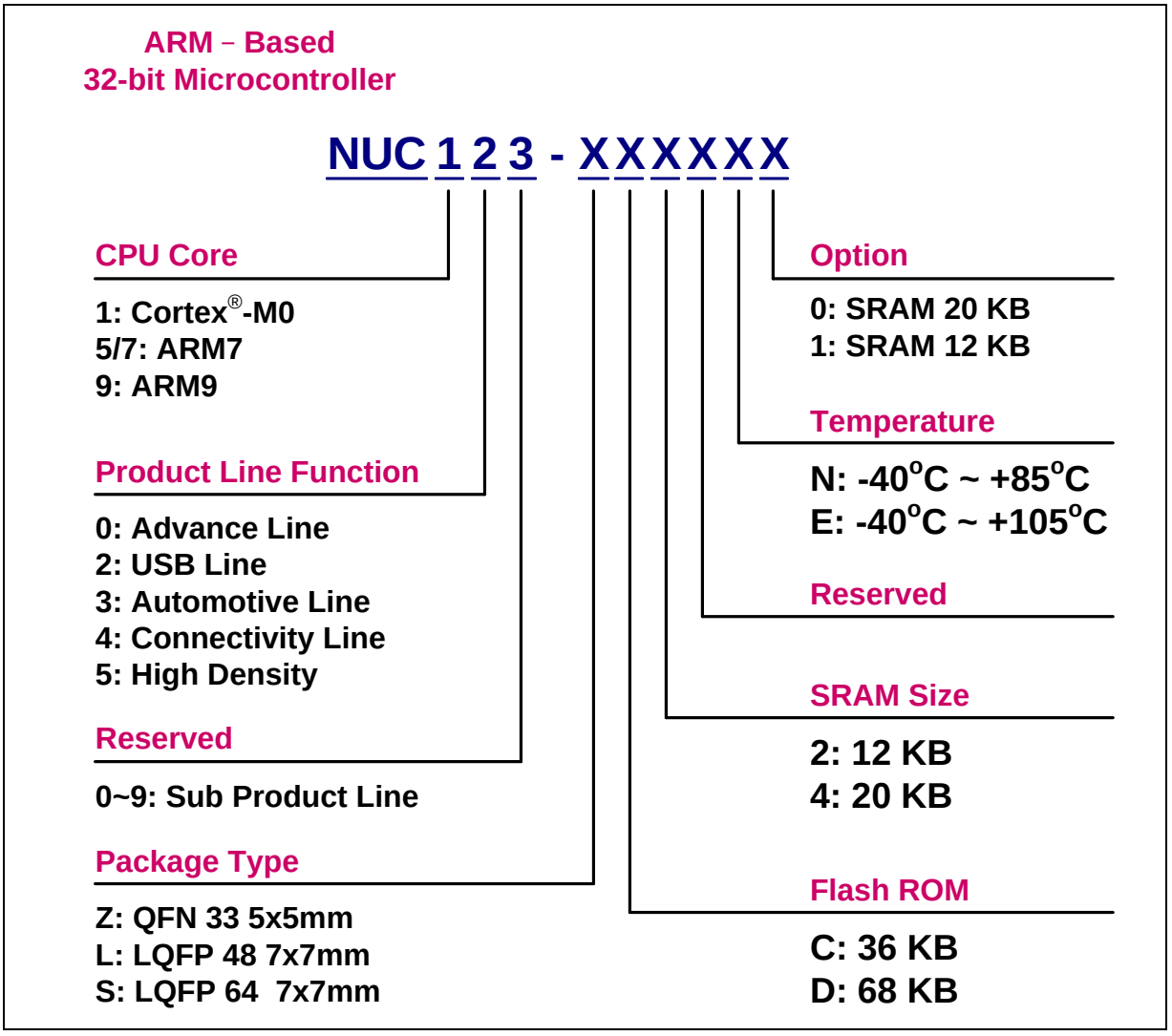


Figure 4-1 NuMicro® NUC123 Series Selection Code

4.2 NuMicro® NUC123 Series Selection Guide

4.2.1 NuMicro® NUC123xxxANx Selection Guide

Part Number	Flash (KB)	SRAM (KB)	ISP ROM (KB)	I/O	Timer	Connectivity						I²S	Comp.	PWM	ADC	RTC	EBI	ISP\ICP\IAP	1.8V Power Pin	Package
						UART	SPI	I²C	USB	LIN	PS/2									
NUC123ZD4AN0	68	20	4	Up to 20	4x32-bit	1	3	1	1	-	-	1	-	2	3x10-bit	-	-	v	-	QFN33
NUC123ZC2AN1	36	12	4	up to 20	4x32-bit	1	3	1	1	-	-	1	-	2	3x10-bit	-	-	v	-	QFN33
NUC123LD4AN0	68	20	4	up to 36	4x32-bit	2	3	2	1	-	1	1	-	4	8x10-bit	-	-	v	-	LQFP48
NUC123LC2AN1	36	12	4	up to 36	4x32-bit	2	3	2	1	-	1	1	-	4	8x10-bit	-	-	v	-	LQFP48
NUC123SD4AN0	68	20	4	up to 47	4x32-bit	2	3	2	1	-	1	1	-	4	8x10-bit	-	-	v	-	LQFP64
NUC123SC2AN1	36	12	4	up to 47	4x32-bit	2	3	2	1	-	1	1	-	4	8x10-bit	-	-	v	-	LQFP64

4.2.2 NuMicro® NUC123xxxAEx Selection Guide

Part Number	Flash (KB)	SRAM (KB)	ISP ROM (KB)	I/O	Timer	Connectivity						I²S	Comp.	PWM	ADC	RTC	EBI	ISP\ICP\IAP	1.8V Power Pin	Package
						UART	SPI	I²C	USB	LIN	PS/2									
NUC123ZD4AE0	68	20	4	Up to 20	4x32-bit	1	3	1	1	-	-	1	-	3	3x10-bit	-	-	v	-	QFN33
NUC123ZC2AE1	36	12	4	up to 20	4x32-bit	1	3	1	1	-	-	1	-	3	3x10-bit	-	-	v	-	QFN33
NUC123LD4AE0	68	20	4	up to 36	4x32-bit	2	3	2	1	-	1	1	-	4	8x10-bit	-	-	v	-	LQFP48
NUC123LC2AE1	36	12	4	up to 36	4x32-bit	2	3	2	1	-	1	1	-	4	8x10-bit	-	-	v	-	LQFP48
NUC123SD4AE0	68	20	4	up to 47	4x32-bit	2	3	2	1	-	1	1	-	4	8x10-bit	-	-	v	-	LQFP64
NUC123SC2AE1	36	12	4	up to 47	4x32-bit	2	3	2	1	-	1	1	-	4	8x10-bit	-	-	v	-	LQFP64

4.3 NuMicro® NUC123 Series Pin Configuration

4.3.1 NuMicro® NUC123xxxANx Pin Diagram

4.3.1.1 NuMicro® NUC123SxxANx LQFP 64 pin

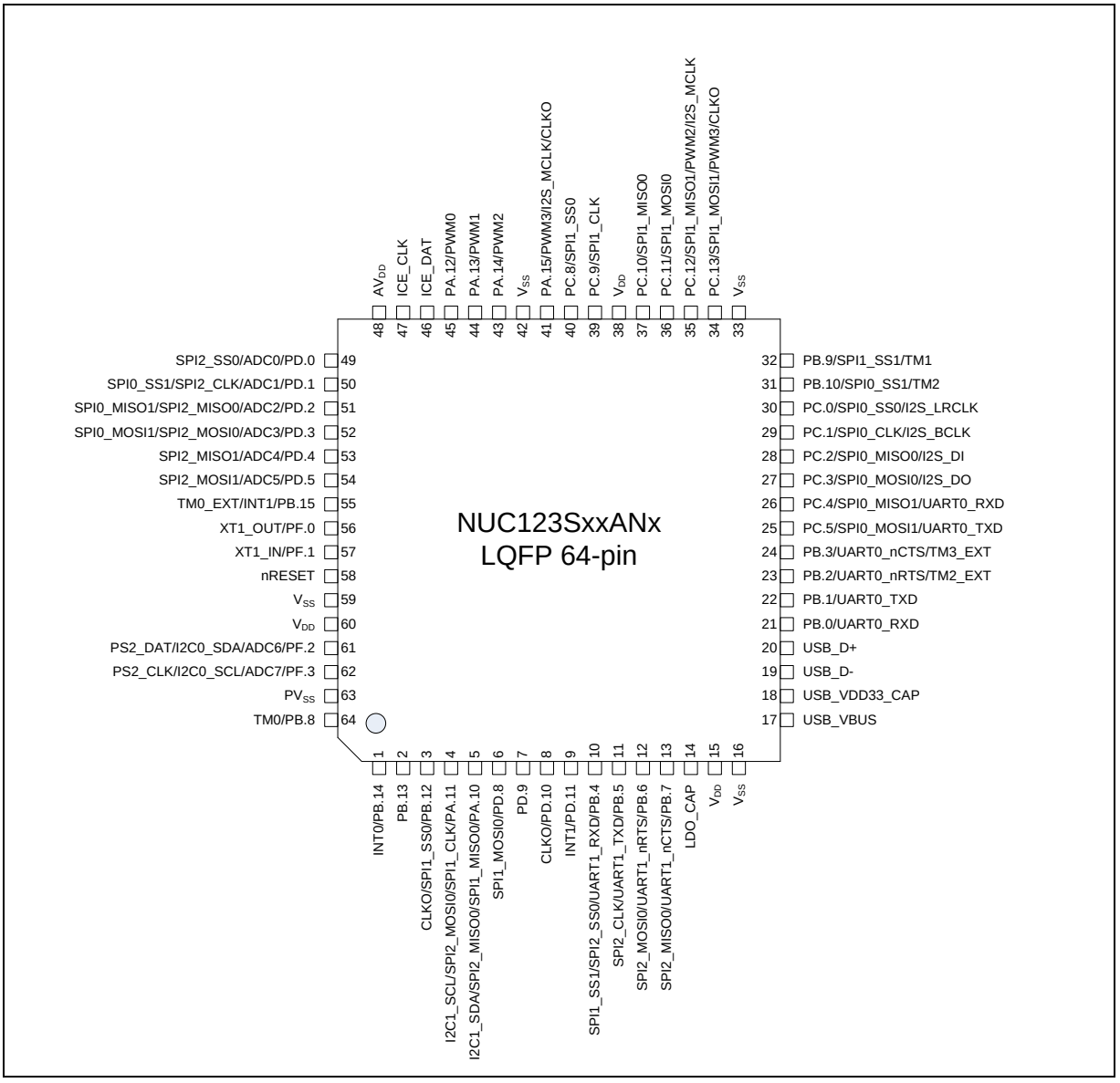


Figure 4-2 NuMicro® NUC123SxxANx LQFP 64-pin Diagram

4.3.1.2 NuMicro® NUC123LxxANx LQFP 48 pin

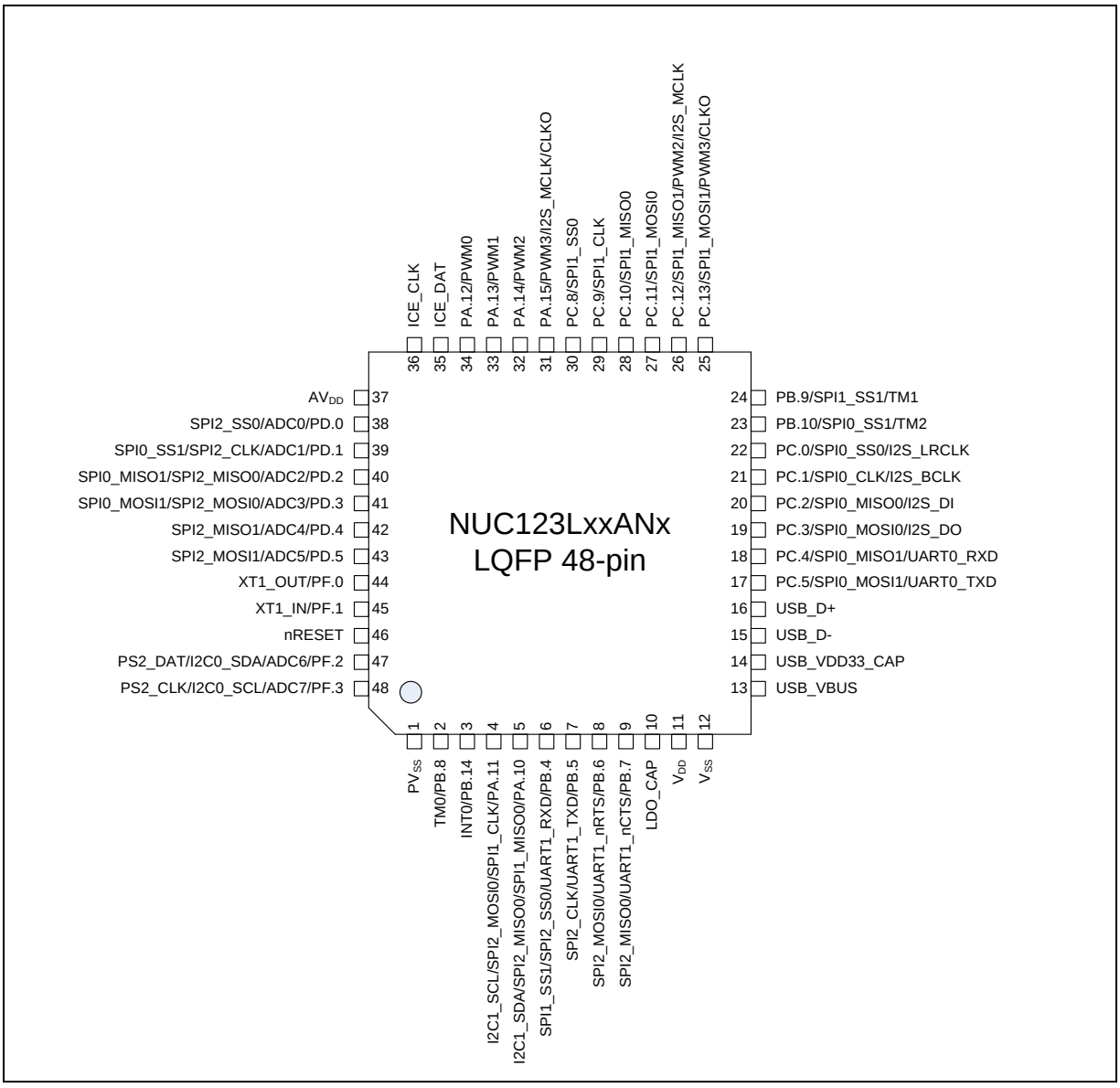


Figure 4-3 NuMicro® NUC123LxxANx LQFP 48-pin Diagram

4.3.1.3 NuMicro® NUC123ZxxANx QFN 33 pin

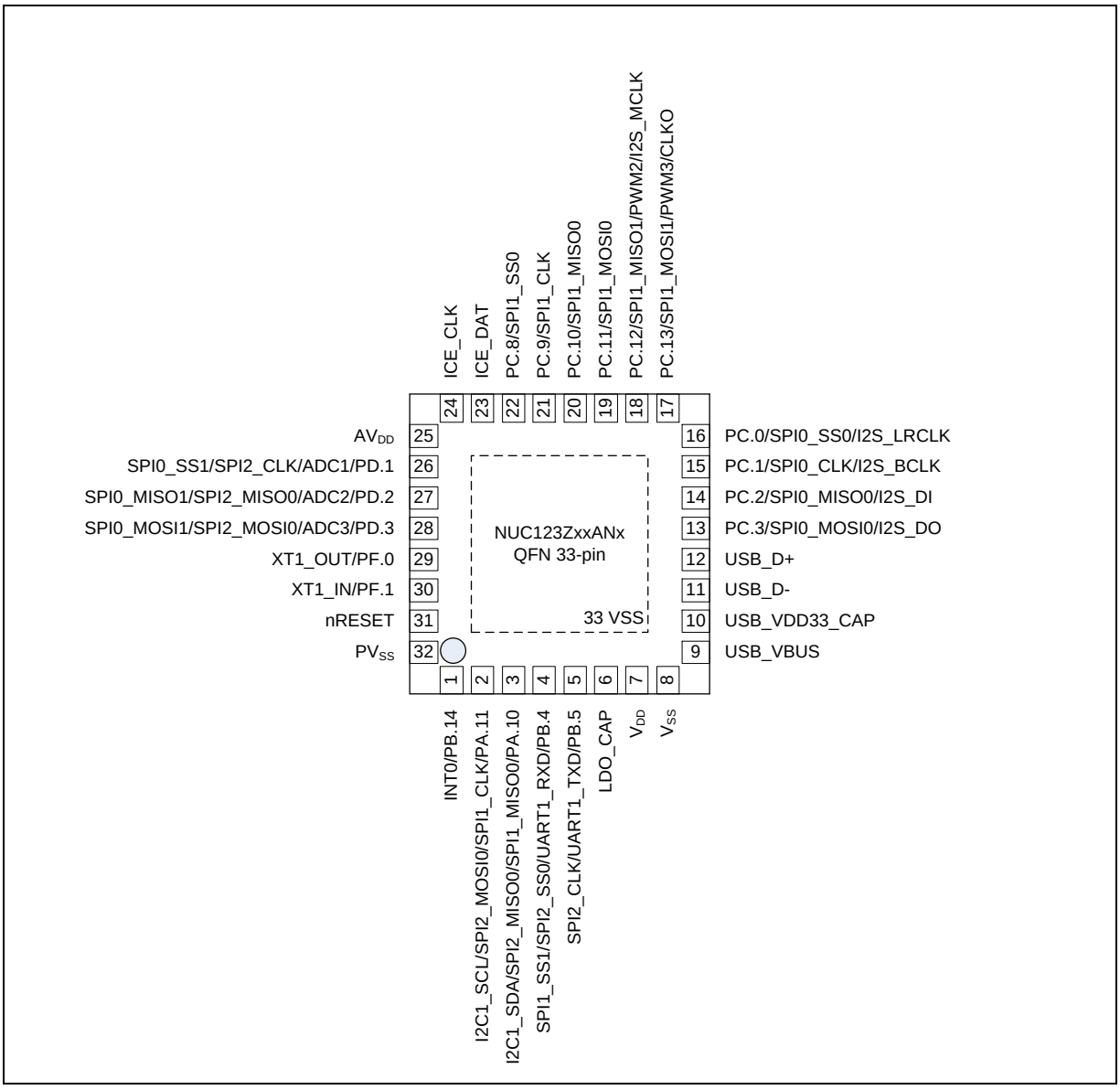


Figure 4-4 NuMicro® NUC123ZxxANx QFN 33-pin Diagram

4.3.2 NuMicro® NUC123xxxAEx Pin Diagram

4.3.2.1 NuMicro® NUC123SxxAEx LQFP 64 pin

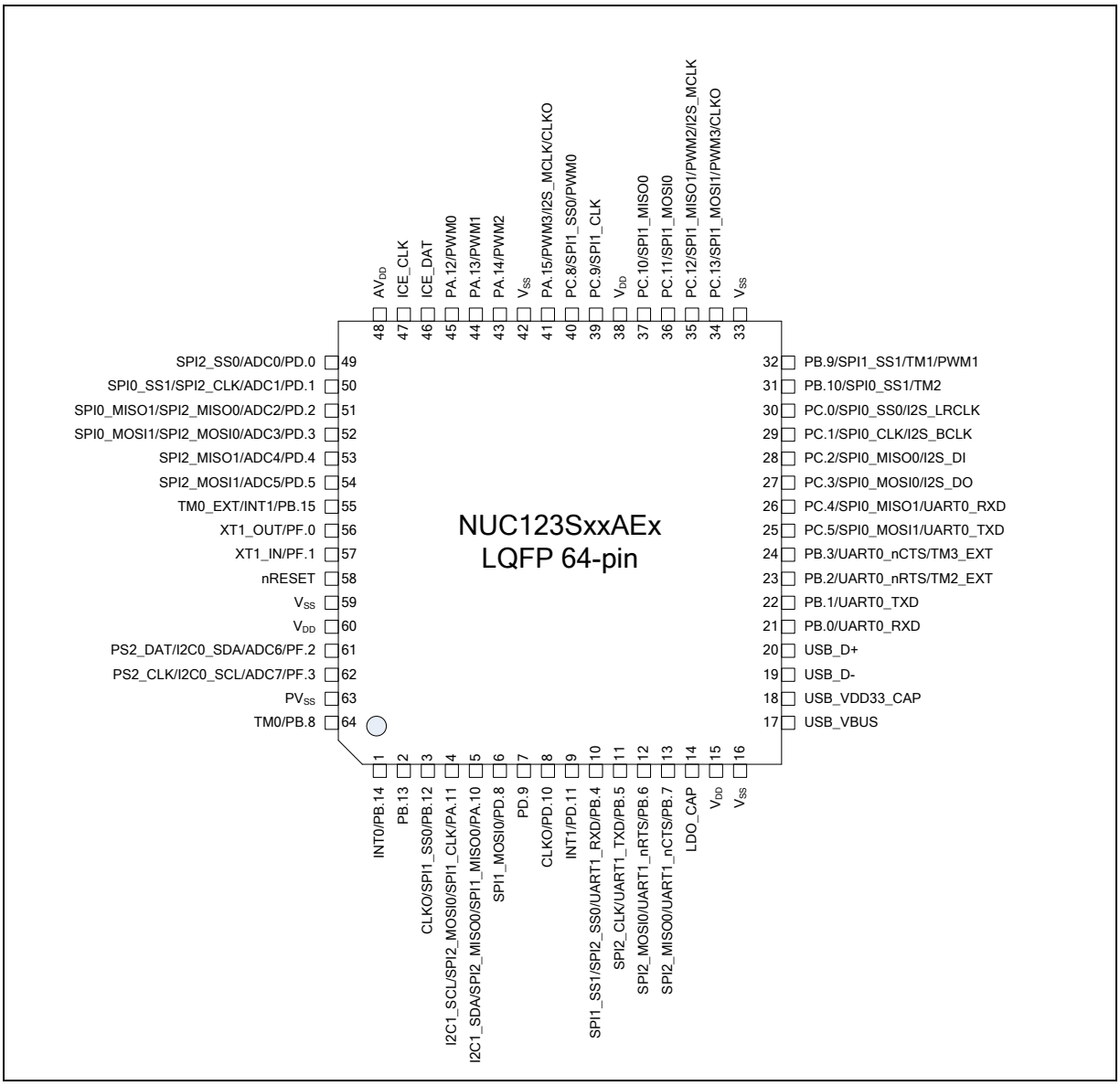


Figure 4-5 NuMicro® NUC123SxxAEx LQFP 64-pin Diagram

4.3.2.2 NuMicro® NUC123LxxAEx LQFP 48 pin

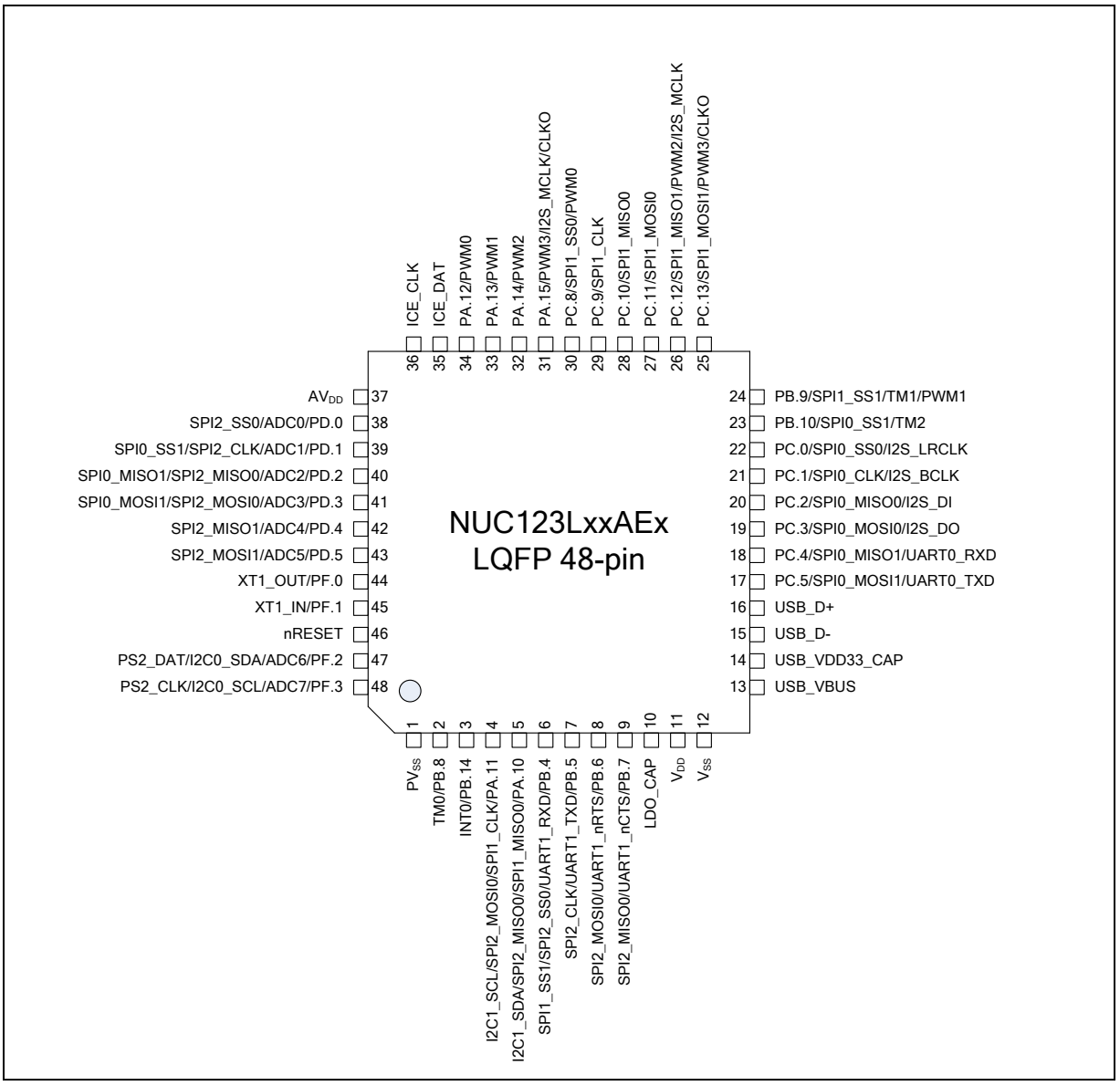


Figure 4-6 NuMicro® NUC123LxxAEx LQFP 48-pin Diagram

4.3.2.3 NuMicro® NUC123ZxxAEx QFN 33 pin

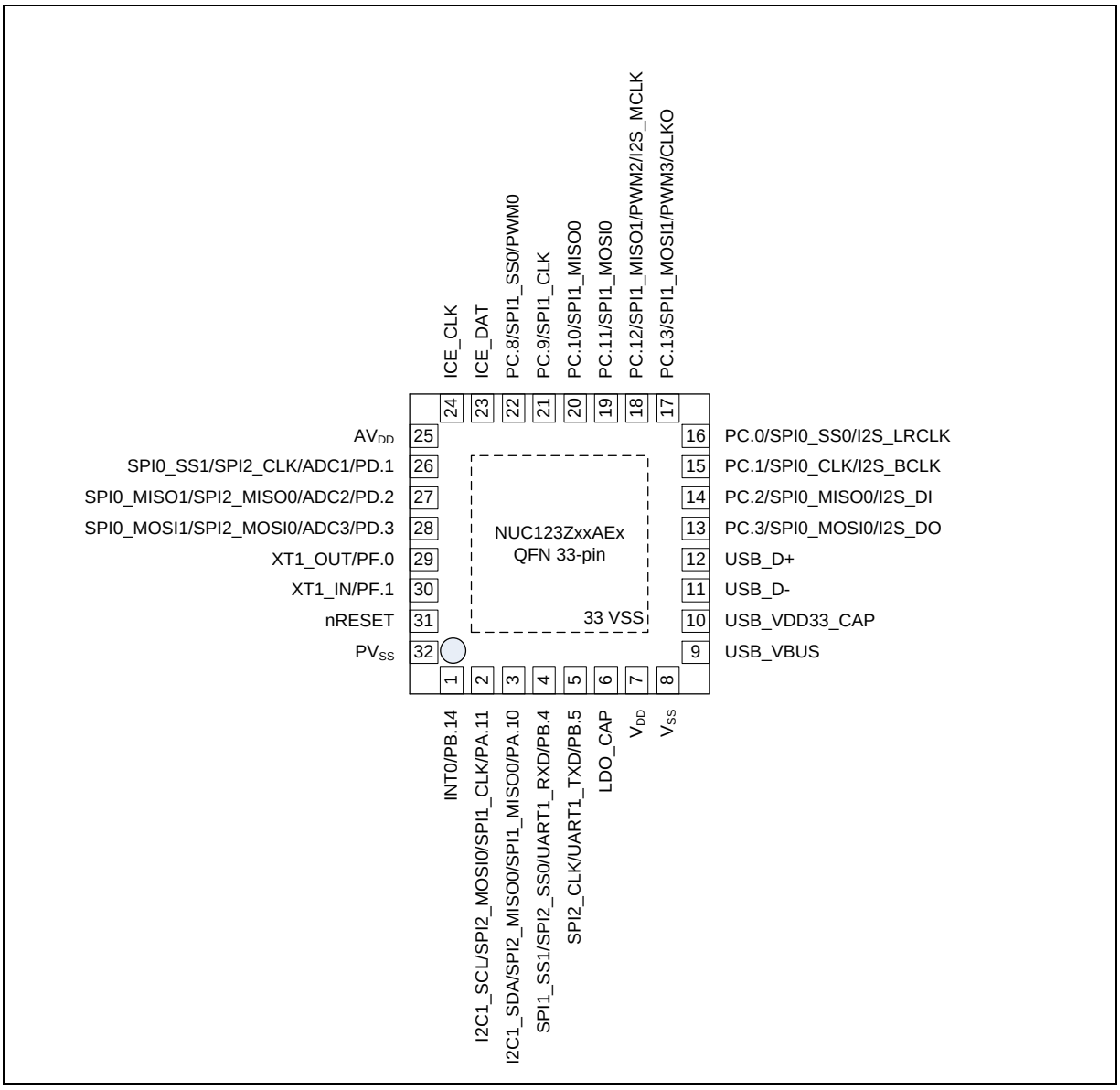


Figure 4-7 NuMicro® NUC123ZxxAEx QFN 33-pin Diagram

4.4 Pin Description

4.4.1 NuMicro® NUC123 Pin Description

Pin No			Pin Name	Type	Description
LQFP 64-pin	LQFP 48-pin	QFN 33-pin			
1	3	1	PB.14	I/O	Digital GPIO pin
			INT0	I	External interrupt 0 input pin
2			PB.13	I/O	Digital GPIO pin
3			PB.12	I/O	Digital GPIO pin
			SPI1_SS0	I/O	SPI1 1st slave select pin
			CLKO	O	Frequency Divider output pin
4	4	2	PA.11	I/O	Digital GPIO pin
			SPI1_CLK	I/O	SPI1 serial clock pin
			SPI2_MOSI0	I/O	SPI2 1st MOSI (Master Out, Slave In) pin
			I2C1_SCL	I/O	I^2C1 clock pin
5*	5*	3*	PA.10	I/O	Digital GPIO pin
			SPI1_MISO0	I/O	SPI1 1st MISO (Master In, Slave Out) pin
			SPI2_MISO0	I/O	SPI2 1st MISO (Master In, Slave Out) pin
			I2C1_SDA	I/O	I^2C1 data input/output pin
6			PD.8	I/O	Digital GPIO pin
			SPI1_MOSI0	I/O	SPI1 1st MOSI (Master Out, Slave In) pin
7			PD.9	I/O	Digital GPIO pin
8			PD.10	I/O	Digital GPIO pin
			CLKO	O	Frequency Divider output pin
9			PD.11	I/O	Digital GPIO pin
			INT1	I	External interrupt 1 input pin
10	6	4	PB.4	I/O	Digital GPIO pin
			UART1_RXD	I	UART1 data receiver input pin
			SPI2_SS0	I/O	SPI2 1st slave select pin
			SPI1_SS1	I/O	SPI1 2nd slave select pin
11	7	5	PB.5	I/O	Digital GPIO pin
			UART1_TXD	O	UART1 data transmitter output pin
			SPI2_CLK	I/O	SPI2 serial clock pin
12	8		PB.6	I/O	Digital GPIO pin
			UART1_nRTS	O	UART1 request to send output pin

			SPI2_MOSI0	**I/O**	SPI2 1st MOSI (Master Out, Slave In) pin
13	9		PB.7	**I/O**	Digital GPIO pin
			UART1_nCTS	**I**	UART1 clear to send input pin
			SPI2_MISO0	**I/O**	SPI2 1st MISO (Master In, Slave Out) pin
14	10	6	LDO_CAP	**P**	LDO output pin
15	11	7	V_{DD}	**P**	Power supply for I/O ports and LDO source for internal PLL and digital function. Voltage range is 2.5V ~ 5V.
16	12	8	V_{SS}	**P**	Ground
17	13	9	USB_VBUS	**USB**	Power supply from USB host or hub
18	14	10	USB_VDD33_CAP	**USB**	Internal power regulator output 3.3V decoupling pin
19	15	11	USB_D-	**USB**	USB differential signal D-
20	16	12	USB_D+	**USB**	USB differential signal D+
21			PB.0	**I/O**	Digital GPIO pin
			UART0_RXD	**I**	UART0 data receiver input pin
22			PB.1	**I/O**	Digital GPIO pin
			UART0_TXD	**O**	UART0 data transmitter output pin
23			PB.2	**I/O**	Digital GPIO pin
			UART0_nRTS	**O**	UART0 request to send output pin
			TM2_EXT	**I**	Timer2 external capture input pin
24			PB.3	**I/O**	Digital GPIO pin
			UART0_nCTS	**I**	UART0 clear to send input pin
			TM3_EXT	**I**	Timer3 external capture input pin
25	17		PC.5	**I/O**	Digital GPIO pin
			SPI0_MOSI1	**I/O**	SPI0 2nd MOSI (Master Out, Slave In) pin
			UART0_TXD	**O**	UART0 data transmitter output pin
26	18		PC.4	**I/O**	Digital GPIO pin
			SPI0_MISO1	**I/O**	SPI0 2nd MISO (Master In, Slave Out) pin
			UART0_RXD	**I**	UART0 data receiver input pin
27	19	13	PC.3	**I/O**	Digital GPIO pin
			SPI0_MOSI0	**I/O**	SPI0 1st MOSI (Master Out, Slave In) pin
			I2S_DO	**O**	I^2S data output pin
28	20	14	PC.2	**I/O**	Digital GPIO pin
			SPI0_MISO0	**I/O**	SPI0 1st MISO (Master In, Slave Out) pin
			I2S_DI	**I**	I^2S data input pin
29	21	15	PC.1	**I/O**	Digital GPIO pin
			SPI0_CLK	**I/O**	SPI0 serial clock pin

			I2S_BCLK	**I/O**	I^2S bit clock pin
30	22	16	PC.0	**I/O**	Digital GPIO pin
			SPI0_SS0	**I/O**	SPI0 1st slave select pin
			I2S_LRCLK	**I/O**	I^2S left/right channel clock pin
31	23		PB.10	**I/O**	Digital GPIO pin
			SPI0_SS1	**I/O**	SPI0 2nd slave select pin
			TM2	**I/O**	Timer2 event counter input / toggle output pin
32	24		PB.9	**I/O**	Digital GPIO pin
			SPI1_SS1	**I/O**	SPI1 2nd slave select pin
			TM1	**I/O**	Timer1 event counter input / toggle output pin
			PWM1	**I/O**	PWM1 PWM output / capture input pin (NUC123xxxAEx Only)
33			V_{SS}	**P**	Ground
34	25	17	PC.13	**I/O**	Digital GPIO pin
			SPI1_MOSI1	**I/O**	SPI1 2nd MOSI (Master Out, Slave In) pin
			PWM3	**I/O**	PWM3 PWM output / capture input pin
			CLKO	**O**	Frequency Divider output pin
35	26	18	PC.12	**I/O**	Digital GPIO pin
			SPI1_MISO1	**I/O**	SPI1 2nd MISO (Master In, Slave Out) pin
			PWM2	**I/O**	PWM2 PWM output / capture input pin
			I2S_MCLK	**O**	I^2S master clock output pin
36	27	19	PC.11	**I/O**	Digital GPIO pin
			SPI1_MOSI0	**I/O**	SPI1 1st MOSI (Master Out, Slave In) pin
37	28	20	PC.10	**I/O**	Digital GPIO pin
			SPI1_MISO0	**I/O**	SPI1 1st MISO (Master In, Slave Out) pin
38			V_{DD}	**P**	Power supply for I/O ports and LDO source for internal PLL and digital function. Voltage range is 2.5V ~ 5V.
39	29	21	PC.9	**I/O**	Digital GPIO pin
			SPI1_CLK	**I/O**	SPI1 serial clock pin
40	30	22	PC.8	**I/O**	Digital GPIO pin
			SPI1_SS0	**I/O**	SPI1 1st slave select pin
			PWM0	**I/O**	PWM0 PWM output / capture input pin (NUC123xxxAEx Only)
41	31		PA.15	**I/O**	Digital GPIO pin
			PWM3	**I/O**	PWM3 PWM output / capture input pin
			I2S_MCLK	**O**	I^2S master clock output pin
			CLKO	**O**	Frequency Divider output pin

42			V_{SS}	**P**	Ground
43	32		PA.14	**I/O**	Digital GPIO pin
			PWM2	**I/O**	PWM2 PWM output / capture input pin
44	33		PA.13	**I/O**	Digital GPIO pin
			PWM1	**I/O**	PWM1 PWM output / capture input pin
45	34		PA.12	**I/O**	Digital GPIO pin
			PWM0	**I/O**	PWM0 PWM output / capture input pin
46	35	23	ICE_DAT	**I/O**	Serial wired debugger data pin **Note:** It is recommended to use 100 kΩ pull-up resistor on ICE_DAT pin.
47	36	24	ICE_CLK	**I**	Serial wired debugger clock input pin **Note:** It is recommended to use 100 kΩ pull-up resistor on ICE_CLK pin.
48	37	25	AV_{DD}	**AP**	Power supply for internal analog circuit
49	38		PD.0	**I/O**	Digital GPIO pin
			ADC0	**AI**	ADC channel 0 analog input pin
			SPI2_SS0	**I/O**	SPI2 1st slave select pin
50	39	26	PD.1	**I/O**	Digital GPIO pin
			SPI2_CLK	**I/O**	SPI2 serial clock pin
			SPI0_SS1	**I/O**	SPI0 2nd slave select pin
			ADC1	**AI**	ADC channel 1 analog input pin
51	40	27	PD.2	**I/O**	Digital GPIO pin
			SPI2_MISO0	**I/O**	SPI2 1st MISO (Master In, Slave Out) pin
			SPI0_MISO1	**I/O**	SPI0 2nd MISO (Master In, Slave Out) pin
			ADC2	**AI**	ADC channel 2 analog input pin
52	41	28	PD.3	**I/O**	Digital GPIO pin
			SPI2_MOSI0	**I/O**	SPI2 1st MOSI (Master Out, Slave In) pin
			SPI0_MOSI1	**I/O**	SPI0 2nd MOSI (Master Out, Slave In) pin
			ADC3	**AI**	ADC channel 3 analog input pin
53	42		PD.4	**I/O**	Digital GPIO pin
			ADC4	**AI**	ADC channel 4 analog input pin
			SPI2_MISO1	**I/O**	SPI2 2nd MISO (Master In, Slave Out) pin
54	43		PD.5	**I/O**	Digital GPIO pin
			ADC5	**AI**	ADC channel 5 analog input pin
			SPI2_MOSI1	**I/O**	SPI2 2nd MOSI (Master Out, Slave In) pin
55			PB.15	**I/O**	Digital GPIO pin
			INT1	**I**	External interrupt 1 input pin

			TM0_EXT	**I**	Timer0 external capture input pin
56	44	29	PF.0	**I/O**	Digital GPIO pin
			XT1_OUT	**O**	External 4~24 MHz high speed crystal output pin
57	45	30	PF.1	**I/O**	Digital GPIO pin
			XT1_IN	**I**	External 4~24 MHz high speed crystal input pin
58	46	31	nRESET	**I**	External reset input: Low active, set this pin low reset chip to initial state. With internal pull-up. **Note:** It is recommended to use 10 kΩ pull-up resistor and 10 μF capacitor on nRESET pin.
59			V_{SS}	**P**	Ground
60			V_{DD}	**P**	Power supply for I/O ports and LDO source for internal PLL and digital circuit. Voltage range is 2.5 V ~ 5V.
61	47		PF.2	**I/O**	Digital GPIO pin
			ADC6	**AI**	ADC channel 6 analog input pin
			I2C0_SDA	**I/O**	I^2C0 data input/output pin
			PS2_DAT	**I/O**	PS/2 data pin
62	48		PF.3	**I/O**	Digital GPIO pin
			ADC7	**AI**	ADC channel 7 analog input pin
			I2C0_SCL	**I/O**	I^2C0 clock pin
			PS2_CLK	**I/O**	PS/2 clock pin
63	1	32	PV_{SS}	**P**	PLL ground
64	2		PB.8	**I/O**	Digital GPIO pin
			TM0	**I/O**	Timer0 event counter input / toggle output pin

Note: Pin Type I = Digital Input, O = Digital Output; AI = Analog Input; P = Power Pin; AP = Analog Power

5 BLOCK DIAGRAM

5.1 NuMicro® NUC123 Block Diagram

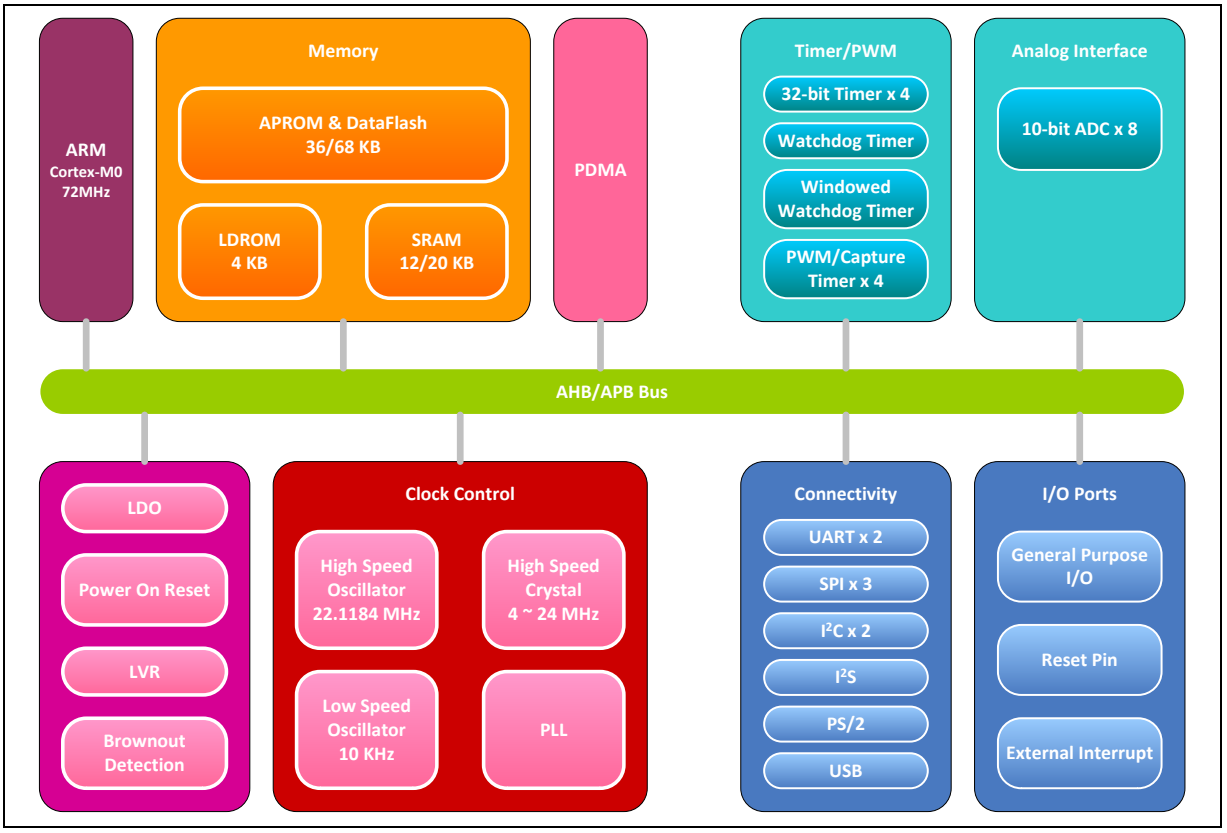


Figure 5-1 NuMicro® NUC123 Block Diagram

6 FUNCTIONAL DESCRIPTION

6.1 ARM® Cortex®-M0 Core

The Cortex®-M0 processor, a configurable, multistage, 32-bit RISC processor, has an AMBA AHB-Lite interface and includes an NVIC component. The processor has optional hardware debug functionality, can execute Thumb code, and is compatible with other Cortex®-M profile processors. The profile supports two modes -Thread mode and Handler mode. Handler mode is entered as a result of an exception. An exception return can only be issued in Handler mode. Thread mode is entered on Reset, and can be entered as a result of an exception return. Figure 6-1 shows the functional controller of processor.

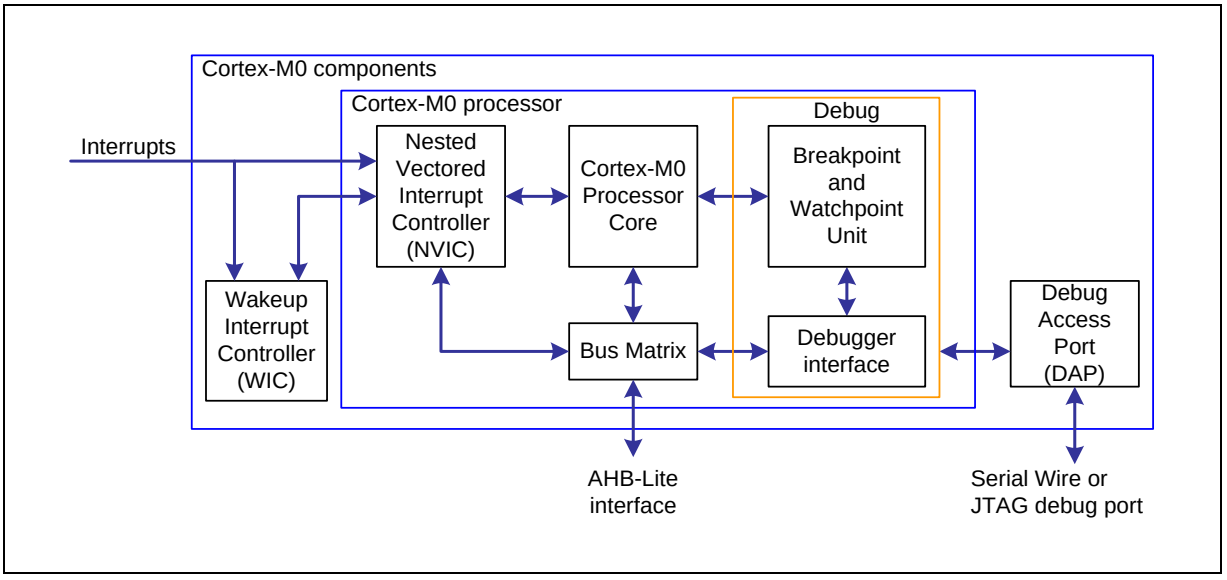


Figure 6-1 Functional Controller Diagram

The implemented device provides:

- A low gate count processor:
  - ARMv6-M Thumb® instruction set
  - Thumb-2 technology
  - ARMv6-M compliant 24-bit SysTick timer
  - A 32-bit hardware multiplier
  - System interface supporting little-endian data accesses
  - Ability to have deterministic, fixed-latency, interrupt handling
  - Load/store-multiples and multicycle-multiplies abandoned and restarted to facilitate rapid interrupt handling
  - C Application Binary Interface compliant exception model, which is the ARMv6-M, C Application Binary Interface (C-ABI) compliant exception model that enables the use of pure C functions as interrupt handlers
  - Low power sleep mode entry using Wait For Interrupt (WFI), Wait For Event (WFE) instructions, or the return from interrupt sleep-on-exit feature
- NVIC :

  - 32 external interrupt inputs, each with four levels of priority
  - Dedicated Non-Maskable Interrupt (NMI) input
  - Supports both level-sensitive and pulse-sensitive interrupt lines
  - Supports Wake-up Interrupt Controller (WIC) with ultra-low power sleep mode
- Debug support
  - Four hardware breakpoints
  - Two watchpoints
  - Program Counter Sampling Register (PCSR) for non-intrusive code profiling
  - Single step and vector catch capabilities
- Bus interfaces:
  - Single 32-bit AMBA-3 AHB-Lite system interface providing simple integration to all system peripherals and memory
  - Single 32-bit slave port supporting the DAP (Debug Access Port)

6.2 System Manager

6.2.1 Overview

The system manager provides the functions of system control, power modes, wake-up sources, reset sources, system memory map, product ID and multi-function pin control. The following sections describe the functions for

- System Reset
- System Power Architecture
- System Memory Map
- System management registers for Part Number ID, chip reset and on-chip controllers reset, and multi-functional pin control
- System Timer (SysTick)
- Nested Vectored Interrupt Controller (NVIC)
- System Control registers

6.2.2 System Reset

The system reset can be issued by one of the events listed below. These reset event flags can be read from RSTSRC register to determine the reset source. Hardware reset can reset chip through peripheral reset signals. Software reset can trigger reset through control registers.

- Hardware Reset Sources
  - Power-on Reset (POR)
  - Low level on the nRESET pin
  - Watchdog Time-out Reset and Window Watchdog Reset (WDT/WWDT Reset)
  - Low Voltage Reset (LVR)
  - Brown-out Detector Reset (BOD Reset)
- Software Reset Sources
  - CHIP Reset will reset whole chip by writing 1 to CHIPRST (IPRSTC1[0])
  - MCU Reset to reboot but keeping the booting setting from APROM or LDROM by writing 1 to SYSRESETREQ (AIRCR[2])
  - CPU Reset for Cortex®-M0 core Only by writing 1 to CPURST (IPRSTC1[1])

Power-on Reset or CHIP_RST (IPRST1[0]) resets the whole chip including all peripherals, external crystal circuit and BS (ISPCON[1]) bit.

SYSRESETREQ (AIRCR[2]) resets the whole chip including all peripherals, but does not reset external crystal circuit and BS (ISPCON[1]) bit.

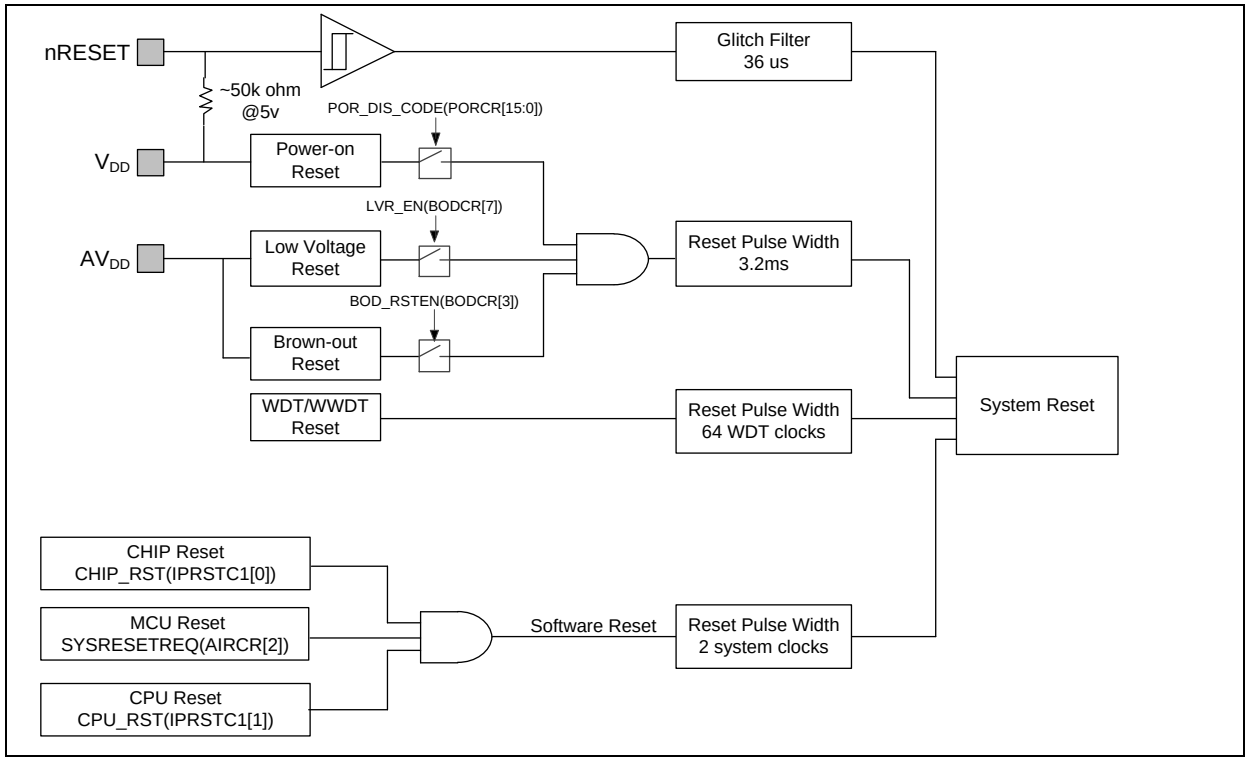


Figure 6-2 System Reset Resources

There are a total of 8 reset sources in the NuMicro® family. In general, CPU reset is used to reset Cortex®-M0 only; the other reset sources will reset Cortex®-M0 and all peripherals. However, there are small differences between each reset source and they are listed in Table 6-1.

Reset Sources / Register	POR	NRESET	WDT	LVR	BOD	CHIP	MCU	CPU
RSTSRC	Bit 0 = 1	Bit 1 = 1	Bit 2 = 1	Bit 3 = 1	Bit 4 = 1	Bit 0 = 1	Bit 5 = 1	Bit 7 = 1
CHIP_RST (IPRSTC1[0])	0x0	-	-	-	-	-	-	-
BOD_EN (BODCR[0])	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	-	Reload from CONFIG0	Reload from CONFIG0	-
BOD_VL (BODCR[2:1])								
BOD_RSTEN (BODCR[3])								
XTL12M_EN (PWRCON [0])	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	-
WDT_EN (APBCLK[0])	0x1	-	0x1	-	-	0x1	-	-
HCLK_S (CLKSEL0[2:0])	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	-

WDT_S (CLKSEL1[1:0])	0x3	0x3	-	-	-	-	-	-
XTL12M_STB (CLKSTATUS[0])	0x0	-	-	-	-	-	-	-
PLL_STB (CLKSTATUS[2])	0x0	-	-	-	-	-	-	-
OSC10K_STB (CLKSTATUS[3])	0x0	-	-	-	-	-	-	-
OSC22M_STB (CLKSTATUS[4])	0x0	-	-	-	-	-	-	-
CLK_SW_FAIL (CLKSTATUS[7])	0x0	0x0	0x0	0x0	0x0	0x0	0x0	-
WTE (WTCR[7])	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0		
WTCR	0x0700	0x0700	0x0700	0x0700	0x0700	0x0700	-	-
WTCRALT	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000	-	-
WWDTRLD	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000	-	-
WWDTCR	0x3F0800	0x3F0800	0x3F0800	0x3F0800	0x3F0800	0x3F0800	-	-
WWDTSR	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000	-	-
WWDTCVR	0x3F	0x3F	0x3F	0x3F	0x3F	0x3F	-	-
BS (ISPCON[1])	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	-	-
DFBADR	Reload from CONFIG1	Reload from CONFIG1	Reload from CONFIG1	Reload from CONFIG1	Reload from CONFIG1	Reload from CONFIG1	-	-
CBS (ISPSTA[2:1])	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	-	-
VECMAP (ISPSTA[20:9]) (NUC123xxxAEx Only)	Reload base on CONFIG0	Reload base on CONFIG0	Reload base on CONFIG0	Reload base on CONFIG0	Reload base on CONFIG0	Reload base on CONFIG0	-	-
Other Peripheral Registers	Reset Value							-
FMC Registers	Reset Value							
Note: '-' means that the value of register keeps original setting.								

Table 6-1 Reset Value of Registers

6.2.2.1 nRESET Reset

The nRESET reset means to generate a reset signal by pulling low nRESET pin, which is an asynchronous reset input pin and can be used to reset system at any time. When the nRESET voltage is lower than 0.2 V_{DD} and the state keeps longer than 36 us (glitch filter), chip will be reset. The

nRESET reset will control the chip in reset state until the nRESET voltage rises above 0.7 V_{DD} and the state keeps longer than 36 us (glitch filter). The RSTS_RESET (RSTSRC[1]) will be set to 1 if the previous reset source is nRESET reset.

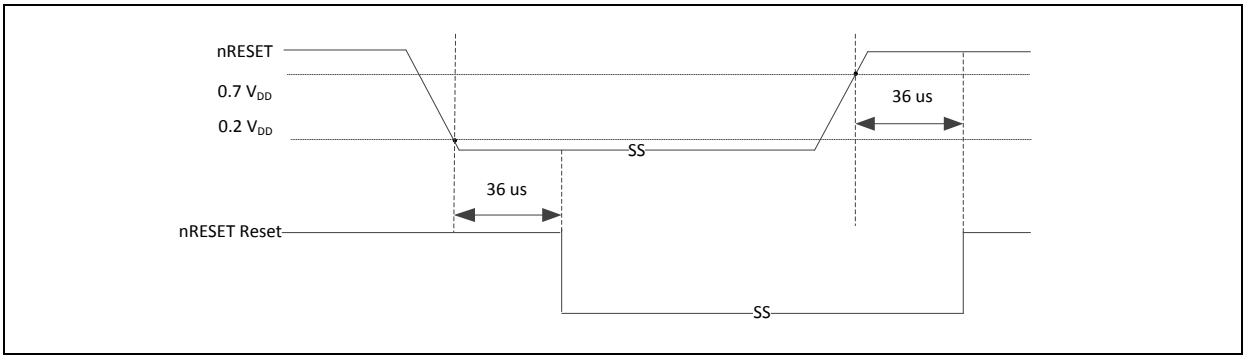


Figure 6-3 shows the nRESET reset waveform.

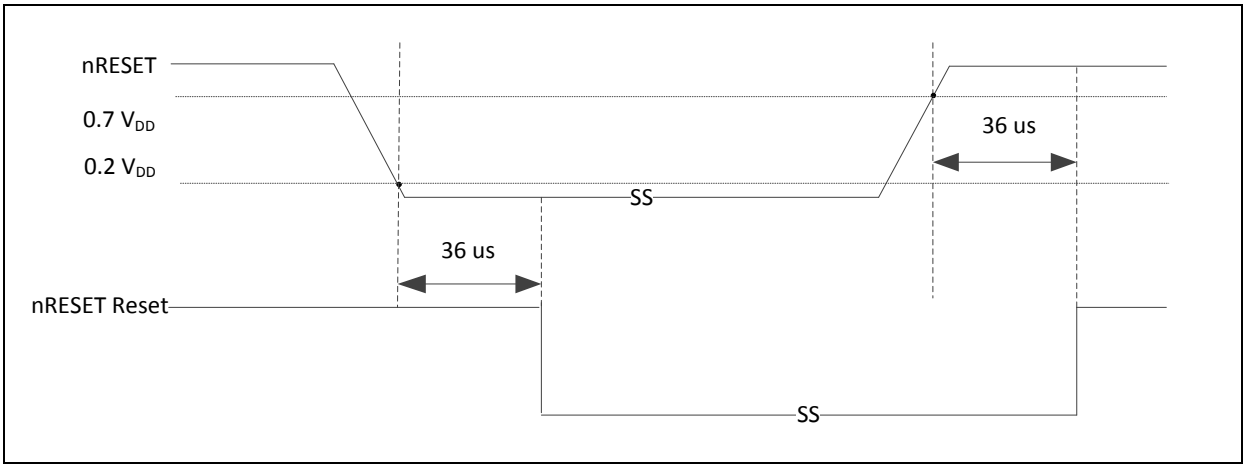


Figure 6-3 nRESET Reset Waveform

6.2.2.2 Power-On Reset (POR)

The Power-on reset (POR) is used to generate a stable system reset signal and forces the system to be reset when power-on to avoid unexpected behavior of MCU. When applying the power to MCU, the POR module will detect the rising voltage and generate reset signal to system until the voltage is ready for MCU operation. At POR reset, the RSTS_POR (RSTSRC[0]) will be set to 1 to indicate there is a POR reset event. The RSTS_POR (RSTSRC[0]) bit can be cleared by writing 1 to it. Figure 6-4 shows the waveform of Power-On reset.

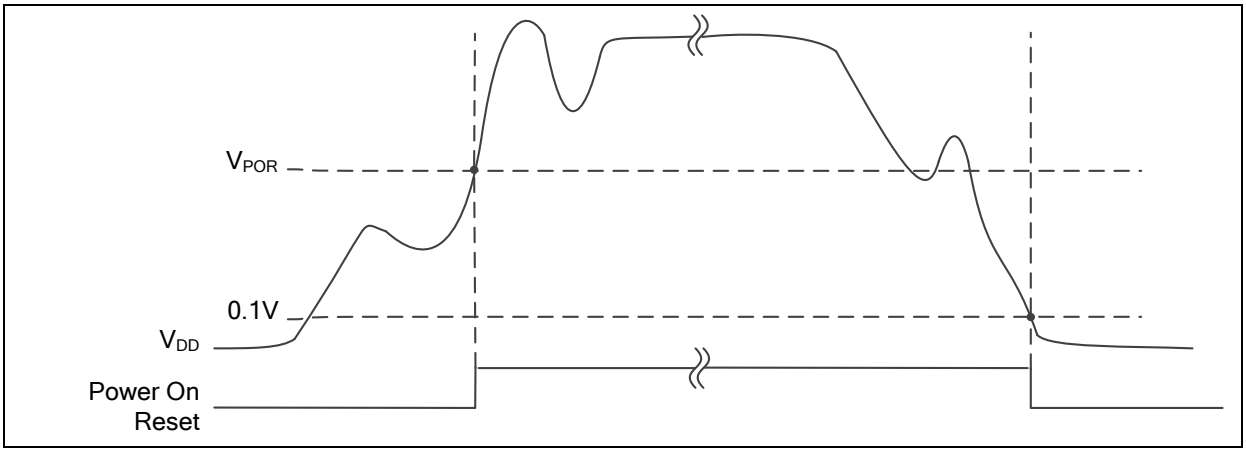


Figure 6-4 Power-on Reset (POR) Waveform

6.2.2.3 Low Voltage Reset (LVR)

If the Low Voltage Reset function is enabled by setting the Low Voltage Reset Enable Bit LVR_EN (BODCR[7]) to 1, after 100us delay, LVR detection circuit will be stable and the LVR function will be active. Then LVR function will detect AV_{DD} during system operation. When the AV_{DD} voltage is lower than V_{LVR} and the state keeps longer than De-glitch time (16*HCLK cycles), chip will be reset. The LVR reset will control the chip in reset state until the AV_{DD} voltage rises above V_{LVR} and the state keeps longer than De-glitch time. The RSTS_RESET (RSTSRC[1]) will be set to 1 if the previous reset source is nRESET reset. Figure 6-5 shows the Low Voltage Reset waveform.

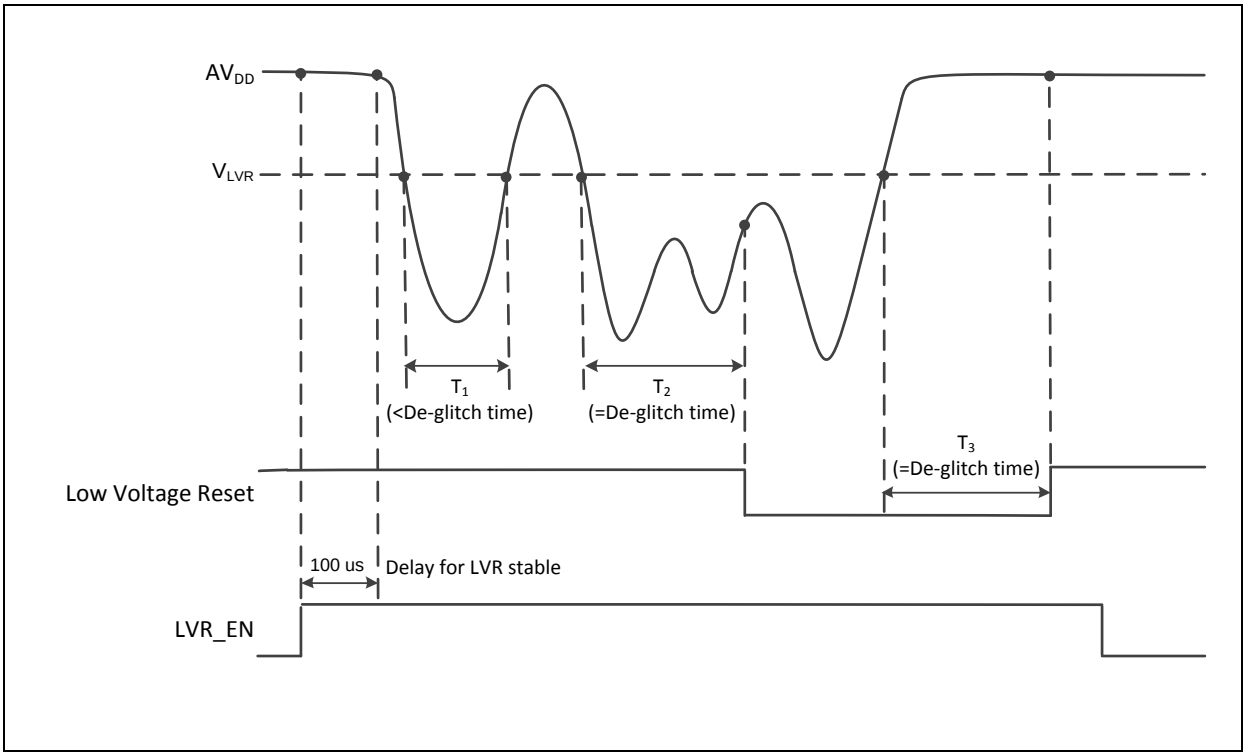


Figure 6-5 Low Voltage Reset Waveform

6.2.2.4 Brown-out Detector Reset (BOD Reset)

If the Brown-out Detector (BOD) function is enabled by setting the Brown-out Detector Enable Bit BOD_EN (BODCR[0]), Brown-Out Detector function will detect AV_{DD} during system operation. When the AV_{DD} voltage is lower than V_{BOD} which is decided by BOD_EN (BODCR[0]) and BOD_VL (BODCR[2:1]) and the state keeps longer than De-glitch time (Max(20*HCLK cycles, 1*LIRC cycle)), chip will be reset. The BOD reset will control the chip in reset state until the AV_{DD} voltage rises above V_{BOD} and the state keeps longer than De-glitch time. The default value of BOD_EN, BOD_VL and BOD_RSTEN is set by flash controller user configuration register CBODEN (CONFIG0[23]), CBOV1-0 (CONFIG0[22:21]) and CBORST (CONFIG0[20]) respectively. User can determine the initial BOD setting by setting the CONFIG0 register. Figure 6-6 shows the Brown-Out Detector waveform.

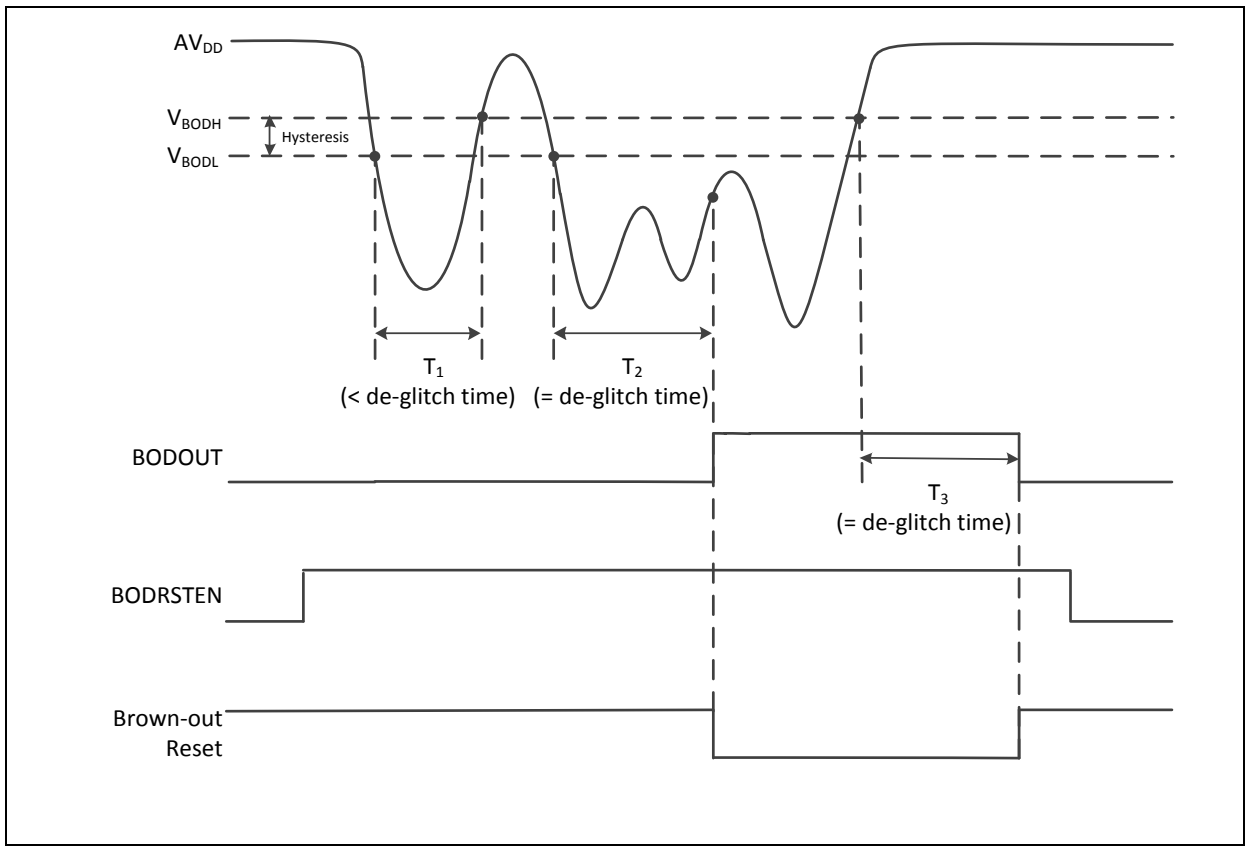


Figure 6-6 Brown-Out Detector Waveform

6.2.2.5 Watch Dog Timer Reset

In most industrial applications, system reliability is very important. To automatically recover the MCU from failure status is one way to improve system reliability. The watch dog timer (WDT) is widely used to check if the system works fine. If the MCU is crashed or out of control, it may cause the watch dog time-out. User may decide to enable system reset during watch dog time-out to recover the system and take action for the system crash/out-of-control after reset.

Software can check if the reset is caused by watch dog time-out to indicate the previous reset is a watch dog reset and handle the failure of MCU after watch dog time-out reset by checking RSTS_WDT (RSTSRC[2]).

6.2.2.6 CPU Reset, CHIP Reset and MCU Reset

The CPU Reset means only Cortex®-M0 core is reset and all other peripherals remain the same status

after CPU reset. User can set the CPU Reset CPU_RST (IPRSTC1[1]) to 1 to assert the CPU Reset signal.

The CHIP Reset is same with Power-On Reset. The CPU and all peripherals are reset and BS (ISPCON[1]) bit is automatically reloaded from CONFIG0 setting. User can set the CHIP Reset CHIP_RST (IPRSTC1[0]) to 1 to assert the CHIP Reset signal.

The MCU Reset is similar with CHIP Reset. The difference is that BS (ISPCON[1]) will not be reloaded from CONFIG0 setting and keep its original software setting for booting from APROM or LDROM. User can set the MCU Reset SYSRESETREQ(AIRCR[2]) to 1 to assert the MCU Reset.

6.2.3 Power modes and Wake-up sources

There are several wake-up sources in Idle mode and Power-down mode. Table 6-2 lists the available clocks for each power mode.

Power Mode	Normal Mode	Idle Mode	Power-Down Mode
Definition	CPU is in active state	CPU is in sleep state	CPU is in sleep state and all clocks stop except LIRC. SRAM content retended.
Entry Condition	Chip is in normal mode after system reset released	CPU executes WFI instruction.	CPU sets sleep mode enable and power down enable and executes WFI instruction.
Wake-up Sources	N/A	All interrupts	WDT, I²C, Timer, UART, BOD and GPIO
Available Clocks	All	All except CPU clock	LIRC
After Wake-up	N/A	CPU back to normal mode	CPU back to normal mode

Table 6-2 Power Mode Difference Table

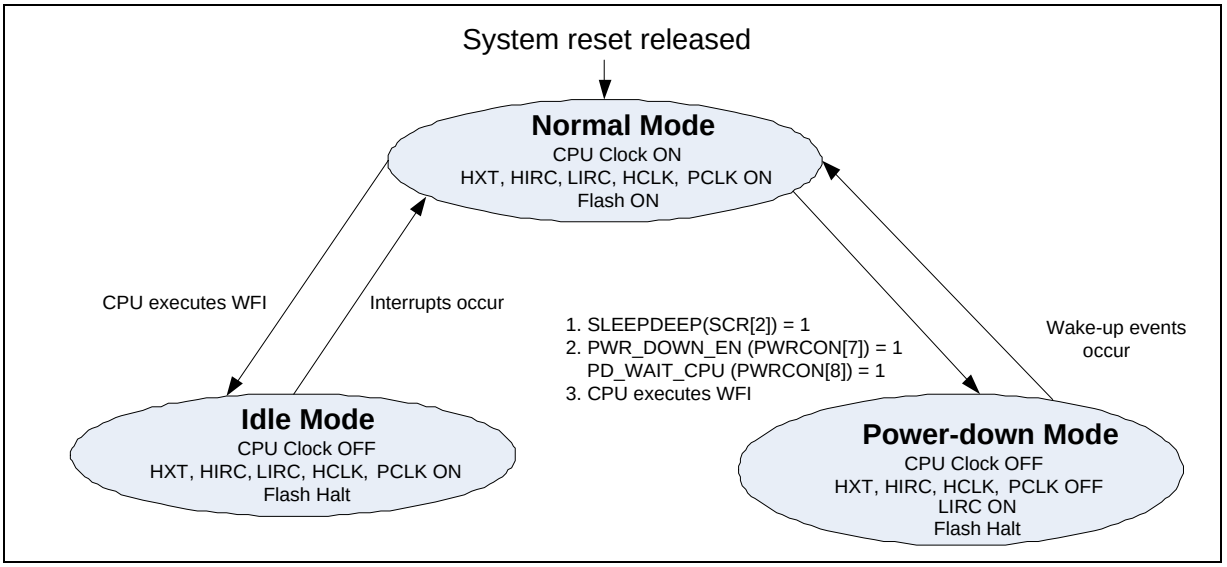


Figure 6-7 Power Mode State Machine

1. LIRC (10 kHz OSC) ON or OFF depends on Software setting in run mode.
2. If TIMER clock source is selected as LIRC and LIRC is on.
3. If WDT clock source is selected as LIRC and LIRC is on.

	Normal Mode	Idle Mode	Power-Down Mode
HXT (4~20 MHz XTL)	ON	ON	Halt
HIRC (12/16 MHz OSC)	ON	ON	Halt
LIRC (10 kHz OSC)	ON	ON	ON/OFF[1]
PLL	ON	ON	Halt
LDO	ON	ON	ON
CPU	ON	Halt	Halt
HCLK/PCLK	ON	ON	Halt
SRAM retention	ON	ON	ON
FLASH	ON	ON	Halt
GPIO	ON	ON	Halt
PDMA	ON	ON	Halt
TIMER	ON	ON	ON/OFF[2]
PWM	ON	ON	Halt
WDT	ON	ON	ON/OFF[3]
WWDT	ON	ON	Halt
UART	ON	ON	Halt
PS/2	ON	ON	Halt
I^2C	ON	ON	Halt
SPI	ON	ON	Halt
I^2S	ON	ON	Halt
USB	ON	ON	Halt
ADC	ON	ON	Halt

Table 6-3 Clocks in Power Modes

Wake-up sources in Power-down mode:

WDT, I²C, Timer, UART, BOD, GPIO and USB

After chip enters power down, the following wake-up sources can wake chip up to normal mode.

Wake-Up Source	Wake-Up Condition	System Can Enter Power-Down Mode Again Condition*
BOD	Brown-Out Detector Interrupt	After software writes 1 to clear BOD_INTF (BODCR[4]).
GPIO	GPIO Interrupt	After software write 1 to clear the ISRC[n] bit.
TIMER	Timer Interrupt	After software writes 1 to clear TWF (TISRx[1]) and TIF (TISRx[0]).
WDT	WDT Interrupt	After software writes 1 to clear WTWKF (WTCR[5]) (Write Protect).
UART	nCTS wake-up	After software writes 1 to clear DCTSF (UA_MSR[0]).
I2C	Addressing I2C device	After software writes 1 to clear WKUPIF (I2CWKUPSTS[0]).
USB	Remote Wake-up	After software writes 1 to clear BUS_STS (USBD_INTSTS[0]).

Table 6-4Table 6-4 lists the condition about how to enter Power-down mode again for each peripheral.

*User needs to wait this condition before setting PWR_DOWN_EN (PWRCON[7]) and execute WFI to enter Power-down mode.

Wake-Up Source	Wake-Up Condition	System Can Enter Power-Down Mode Again Condition*
BOD	Brown-Out Detector Interrupt	After software writes 1 to clear BOD_INTF (BODCR[4]).
GPIO	GPIO Interrupt	After software write 1 to clear the ISRC[n] bit.
TIMER	Timer Interrupt	After software writes 1 to clear TWF (TISRx[1]) and TIF (TISRx[0]).
WDT	WDT Interrupt	After software writes 1 to clear WTWKF (WTCR[5]) (Write Protect).
UART	nCTS wake-up	After software writes 1 to clear DCTSF (UA_MSR[0]).
I^2C	Addressing I^2C device	After software writes 1 to clear WKUPIF (I2CWKUPSTS[0]).
USB	Remote Wake-up	After software writes 1 to clear BUS_STS (USBD_INTSTS[0]).

Table 6-4 Condition of Entering Power-down Mode Again

6.2.4 System Power Distribution

In this chip, power distribution is divided into three segments:

- Analog power from AV_{DD} and AV_{SS} provides the power for analog components operation.
- Digital power from V_{DD} and V_{SS} supplies the power to the internal regulator which provides a fixed 1.8 V power for digital operation and I/O pins.
- USB transceiver power from VBUS offers the power for operating the USB transceiver.

The outputs of internal voltage regulators, LDO and USB_VDD33_CAP, require an external capacitor which should be located close to the corresponding pin. Analog power (AV_{DD}) should be the same voltage level of the digital power (V_{DD}). Figure 6-8 shows the power distribution of the NuMicro® NUC123 series.

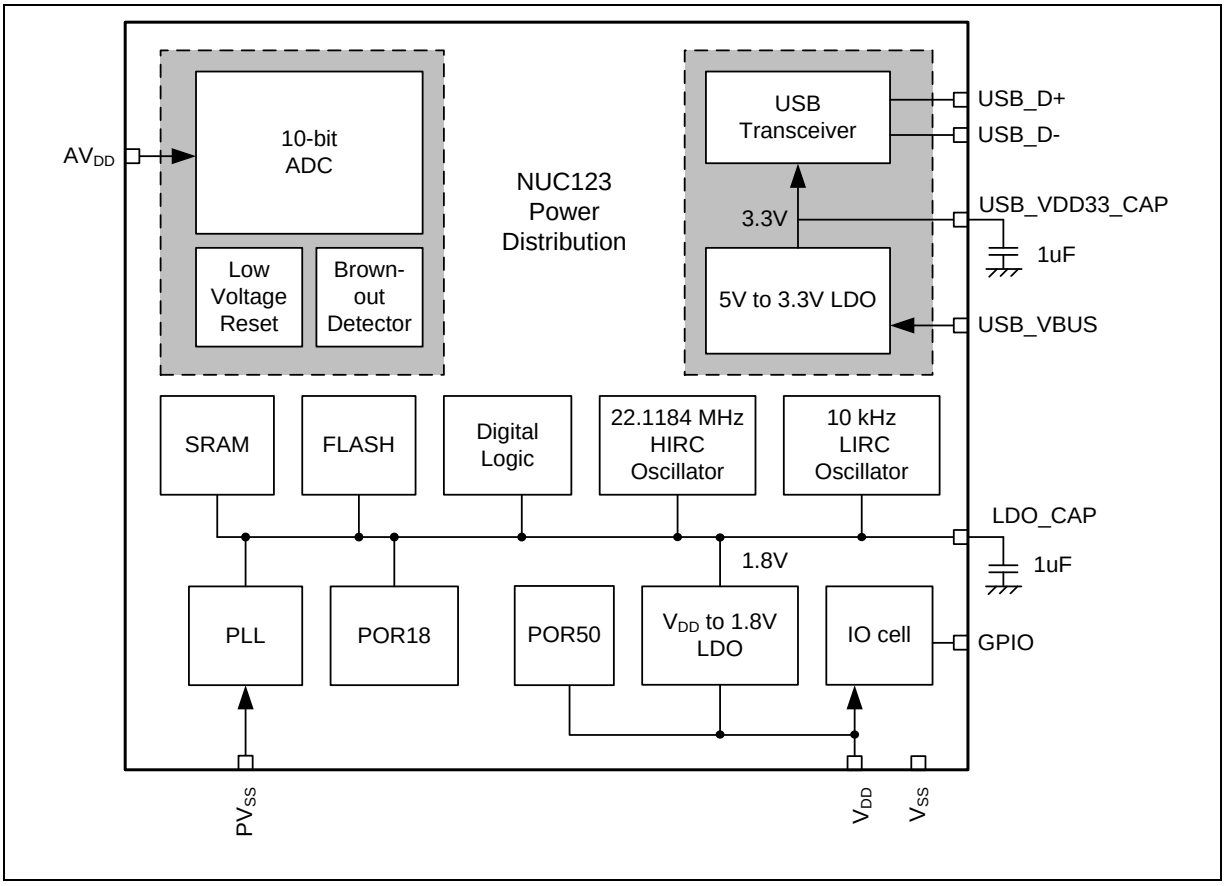


Figure 6-8 NuMicro® NUC123 Power Distribution Diagram

6.2.5 System Memory Map

The NuMicro® NUC123 series provides 4G-byte addressing space. The memory locations assigned to each on-chip controllers are shown in the Table 6-5. The detailed register definition, memory space, and programming detailed will be described in the following sections for each on-chip peripherals. The NuMicro® NUC123 Series only supports little-endian data format.

Address Space	Token	Controllers
Flash and SRAM Memory Space		
0x0000_0000 – 0x0000_FFFF	FLASH_BA	FLASH Memory Space (64KB)
0x2000_0000 – 0x2000_4FFF	SRAM_BA	SRAM Memory Space (20KB)
AHB Controllers Space (0x5000_0000 – 0x501F_FFFF)		
0x5000_0000 – 0x5000_01FF	GCR_BA	System Global Control Registers
0x5000_0200 – 0x5000_02FF	CLK_BA	Clock Control Registers
0x5000_0300 – 0x5000_03FF	INT_BA	Interrupt Multiplexer Control Registers
0x5000_4000 – 0x5000_7FFF	GPIO_BA	GPIO Control Registers
0x5000_8000 – 0x5000_BFFF	PDMA_BA	Peripheral DMA Control Registers
0x5000_C000 – 0x5000_FFFF	FMC_BA	Flash Memory Control Registers
APB1 Controllers Space (0x4000_0000 ~ 0x400F_FFFF)		
0x4000_4000 – 0x4000_7FFF	WDT_BA	Watchdog/Window Watchdog Timer Control Registers
0x4001_0000 – 0x4001_3FFF	TMR01_BA	Timer0/Timer1 Control Registers
0x4002_0000 – 0x4002_3FFF	I2C0_BA	I^2C0 Interface Control Registers
0x4003_0000 – 0x4003_3FFF	SPI0_BA	SPI0 with master/slave function Control Registers
0x4003_4000 – 0x4003_7FFF	SPI1_BA	SPI1 with master/slave function Control Registers
0x4004_0000 – 0x4004_3FFF	PWMA_BA	PWM0/1/2/3 Control Registers
0x4005_0000 – 0x4005_3FFF	UART0_BA	UART0 Control Registers
0x4006_0000 – 0x4006_3FFF	USBD_BA	USB 2.0 FS device Controller Registers
0x400E_0000 – 0x400E_FFFF	ADC_BA	Analog-Digital-Converter (ADC) Control Registers
APB2 Controllers Space (0x4010_0000 ~ 0x401F_FFFF)		
0x4010_0000 – 0x4010_3FFF	PS2_BA	PS/2 Interface Control Registers
0x4011_0000 – 0x4011_3FFF	TMR23_BA	Timer2/Timer3 Control Registers
0x4012_0000 – 0x4012_3FFF	I2C1_BA	I^2C1 Interface Control Registers
0x4013_0000 – 0x4013_3FFF	SPI2_BA	SPI2 with master/slave function Control Registers
0x4015_0000 – 0x4015_3FFF	UART1_BA	UART1 Control Registers
0x401A_0000 – 0x401A_3FFF	I2S_BA	I^2S Interface Control Registers
System Controllers Space (0xE000_E000 ~ 0xE000_EFFF)		
0xE000_E010 – 0xE000_E0FF	SCS_BA	System Timer Control Registers

0xE000_E100 – 0xE000_ECFF	SCS_BA	External Interrupt Controller Control Registers
0xE000_ED00 – 0xE000_ED8F	SCS_BA	System Control Registers

Table 6-5 Address Space Assignments for On-Chip Controllers

6.2.6 System Timer (SysTick)

The Cortex®-M0 includes an integrated system timer, SysTick, which provides a simple, 24-bit clear-on-write, decrementing, wrap-on-zero counter with a flexible control mechanism. The counter can be used as a Real Time Operating System (RTOS) tick timer or as a simple counter.

When system timer is enabled, it will count down from the value in the SysTick Current Value Register (SYST_CVR) to zero, and reload (wrap) to the value in the SysTick Reload Value Register (SYST_RVR) on the next clock cycle, and then decrement on subsequent clocks. When the counter transitions to zero, the COUNTFLAG status bit is set. The COUNTFLAG bit clears on reads.

The SYST_CVR value is UNKNOWN on reset. Software should write to the register to clear it to zero before enabling the feature. This ensures the timer will count from the SYST_RVR value rather than an arbitrary value when it is enabled.

If the SYST_RVR is zero, the timer will be maintained with a current value of zero after it is reloaded with this value. This mechanism can be used to disable the feature independently from the timer enable bit.

For more detailed information, please refer to the “ARM® Cortex®-M0 Technical Reference Manual” and “ARM® v6-M Architecture Reference Manual”.

6.2.7 Nested Vectored Interrupt Controller (NVIC)

Cortex®-M0 provides an interrupt controller as an integral part of the exception mode, named as "Nested Vectored Interrupt Controller (NVIC)". It is closely coupled to the processor kernel and provides following features:

- Nested and Vectored interrupt support
- Automatic processor state saving and restoration
- Dynamic priority changing
- Reduced and deterministic interrupt latency

The NVIC prioritizes and handles all supported exceptions. All exceptions are handled in Handler mode. This NVIC architecture supports 32 (IRQ[31:0]) discrete interrupts with 4 levels of priority. All of the interrupts and most of the system exceptions can be configured to different priority levels. When an interrupt occurs, the NVIC will compare the priority of the new interrupt to the current running one's priority. If the priority of the new interrupt is higher than the current one, the new interrupt handler will override the current handler.

When any interrupts is accepted, the starting address of the interrupt service routine (ISR) is fetched from a vector table in memory. There is no need to determine which interrupt is accepted and branch to the starting address of the correlated ISR by software. While the starting address is fetched, NVIC will also automatically save processor state including the registers "PC, PSR, LR, R0~R3, R12" to the stack. At the end of the ISR, the NVIC will restore the mentioned registers from stack and resume the normal execution. Thus it will take less and deterministic time to process the interrupt request.

The NVIC supports "Tail Chaining" which handles back-to-back interrupts efficiently without the overhead of states saving and restoration and therefore reduces delay time in switching to pending ISR at the end of current ISR. The NVIC also supports "Late Arrival" which improves the efficiency of concurrent ISRs. When a higher priority interrupt request occurs before the current ISR starts to execute (at the stage of state saving and starting address fetching), the NVIC will give priority to the higher one without delay penalty. Thus it advances the real-time capability.

For more detailed information, please refer to the "ARM® Cortex®-M0 Technical Reference Manual" and "ARM® v6-M Architecture Reference Manual".

6.2.7.1 *Exception Model and System Interrupt Map*

Table 6-6 lists the exception model supported by the NuMicro® NUC123 Series. Software can set four levels of priority on some of these exceptions as well as on all interrupts. The highest user-configurable priority is denoted as “0” and the lowest priority is denoted as “3”. The default priority of all the user-configurable interrupts is “0”. Note that priority “0” is treated as the fourth priority on the system, after three system exceptions “Reset”, “NMI” and “Hard Fault”.

Exception Name	Vector Number	Priority
Reset	1	-3
NMI	2	-2
Hard Fault	3	-1
Reserved	4 ~ 10	Reserved
SVCall	11	Configurable
Reserved	12 ~ 13	Reserved
PendSV	14	Configurable
SysTick	15	Configurable
Interrupt (IRQ0 ~ IRQ31)	16 ~ 47	Configurable

Table 6-6 Exception Model

Vector Number	Interrupt Number (Bit In Interrupt Registers)	Interrupt Name	Source IP	Interrupt Description
0 ~ 15	-	-	-	System exceptions
16	0	**BOD_OUT**	Brown-out	Brown-out low voltage detected interrupt
17	1	**WDT_INT**	WDT	Watchdog/Window Watchdog Timer interrupt
18	2	**EINT0**	GPIO	External signal interrupt from PB.14 pin
19	3	**EINT1**	GPIO	External signal interrupt from PB.15 or PD.11 pin
20	4	**GPAB_INT**	GPIO	External signal interrupt from PA[15:0]/PB[13:0]
21	5	**GPCDF_INT**	GPIO	External interrupt from PC[15:0]/PD[15:0]/PF[3:0]
22	6	**PWMA_INT**	PWM0~3	PWM0, PWM1, PWM2 and PWM3 interrupt
23	7	**Reserved**	Reserved	Reserved
24	8	**TMR0_INT**	TMR0	Timer 0 interrupt
25	9	**TMR1_INT**	TMR1	Timer 1 interrupt
26	10	**TMR2_INT**	TMR2	Timer 2 interrupt
27	11	**TMR3_INT**	TMR3	Timer 3 interrupt
28	12	**UART0_INT**	UART0	UART0 interrupt
29	13	**UART1_INT**	UART1	UART1 interrupt
30	14	**SPI0_INT**	SPI0	SPI0 interrupt

31	15	**SPI1_INT**	SPI1	SPI1 interrupt
32	16	**SPI2_INT**	SPI2	SPI2 interrupt
33	17	**Reserved**	Reserved	Reserved
34	18	**I2C0_INT**	I^2C0	I^2C0 interrupt
35	19	**I2C1_INT**	I^2C1	I^2C1 interrupt
36	20	**Reserved**	Reserved	Reserved
37	21	**Reserved**	Reserved	Reserved
38	22	**Reserved**	Reserved	Reserved
39	23	**USB_INT**	USBD	USB 2.0 FS Device interrupt
40	24	**PS2_INT**	PS/2	PS/2 interrupt
41	25	**Reserved**	Reserved	Reserved
42	26	**PDMA_INT**	PDMA	PDMA interrupt
43	27	**I2S_INT**	I^2S	I^2S interrupt
44	28	**PWRWU_INT**	CLKC	Clock controller interrupt for chip wake-up from Power-down state
45	29	**ADC_INT**	ADC	ADC interrupt
46	30	**Reserved**	Reserved	Reserved
47	31	**Reserved**	Reserved	Reserved

Table 6-7 System Interrupt Map

6.2.7.2 Vector Table

When any interrupts is accepted, the processor will automatically fetch the starting address of the interrupt service routine (ISR) from a vector table in memory. For ARMv6-M, the vector table base address is fixed at 0x00000000. The vector table contains the initialization value for the stack pointer on reset, and the entry point addresses for all exception handlers. The vector number on previous page defines the order of entries in the vector table associated with exception handler entry as illustrated in previous section.

Vector Table Word Offset	Description
0	SP_main – The Main stack pointer
Vector Number	Exception Entry Pointer using that Vector Number

Table 6-8 Vector Table Format

6.2.7.3 Operation Description

NVIC interrupts can be enabled and disabled by writing to their corresponding Interrupt Set-Enable or Interrupt Clear-Enable register bit-field. The registers use a write-1-to-enable and write-1-to-clear policy, both registers reading back the current enabled state of the corresponding interrupts. When an interrupt is disabled, interrupt assertion will cause the interrupt to become Pending; however, the interrupt will not activate. If an interrupt is Active when it is disabled, it remains in its Active state until cleared by reset or an exception return. Clearing the enable bit prevents new activations of the associated interrupt.

NVIC interrupts can be pended/un-pended using a complementary pair of registers to those used to enable/disable the interrupts, named the Set-Pending Register and Clear-Pending Register respectively. The registers use a write-1-to-enable and write-1-to-clear policy, both registers reading back the current pended state of the corresponding interrupts. The Clear-Pending Register has no effect on the execution status of an Active interrupt.

NVIC interrupts are prioritized by updating an 8-bit field within a 32-bit register (each register supporting four interrupts).

The general registers associated with the NVIC are all accessible from a block of memory in the System Control Space and will be described in next section.

6.3 Clock Controller

6.3.1 Overview

The clock controller generates the clocks for the whole chip, including system clocks and all peripheral clocks. The clock controller also implements the power control function with the individually clock ON/OFF control, clock source selection and clock divider. The chip enters Power-down mode when Cortex®-M0 core executes the WFI instruction only if the PWR_DOWN_EN (PWRCON[7]) bit and PD_WAIT_CPU (PWRCON[8]) bit are both set to 1. After that, chip enters Power-down mode and wait for wake-up interrupt source triggered to leave Power-down mode. In the Power-down mode, the clock controller turns off the 4~24 MHz external high speed crystal oscillator and 22.1184 MHz internal high speed RC oscillator to reduce the overall system power consumption. The Figure 6-9 and Figure 6-10 show the clock generator and the overview of the clock source control.

The clock generator consists of 4 clock sources as listed below:

- 4~24 MHz external high speed crystal oscillator (HXT)
- Programmable PLL output clock frequency(PLL FOUT), PLL source can be from 4~24 MHz external high speed crystal oscillator (HXT) or 22.1184 MHz internal high speed RC oscillator (HIRC))
- 22.1184 MHz internal high speed RC oscillator (HIRC)
- 10 kHz internal low speed RC oscillator (LIRC)

Each of these clock sources has certain stable time to wait for clock operating at stable frequency. When clock source is enabled, a stable counter start counting and correlated clock stable index (OSC22M_STB(CLKSTATUS[4]), OSC10K_STB(CLKSTATUS[3]), PLL_STB(CLKSTATUS[2]) and XTL12M_STB(CLKSTATUS[0])) are set to 1 after stable counter value reach a define value asshown in Table 6-9. System and peripheral can use the clock as its operating clock only when correlate clock stable index is set to 1. The clock stable index will auto clear when user disables the clock source (OSC10K_EN(PWRCON[3]), OSC22M_EN(PWRCON[2]), XTL12M_EN(PWRCON[0]) and PD(PLLCON[16])). Besides, the clock stable index of HXT, HIRC and PLL will auto clear when chip enter power-down and clock stable counter will re-counting after chip wake-up if correlate clock is enabled.

Clock Source	Clock Stable Count Value
HXT	4096 HXT clock
PLL	6144 PLL source (PLL source is HXT if PLL_SRC(PLLCON[19]) = 0, or HIRC if PLL_SRC(PLLCON[19]) = 1)
HIRC	256 HIRC clock
LIRC	1 LIRC

Table 6-9 Clock Stable Count Value Table

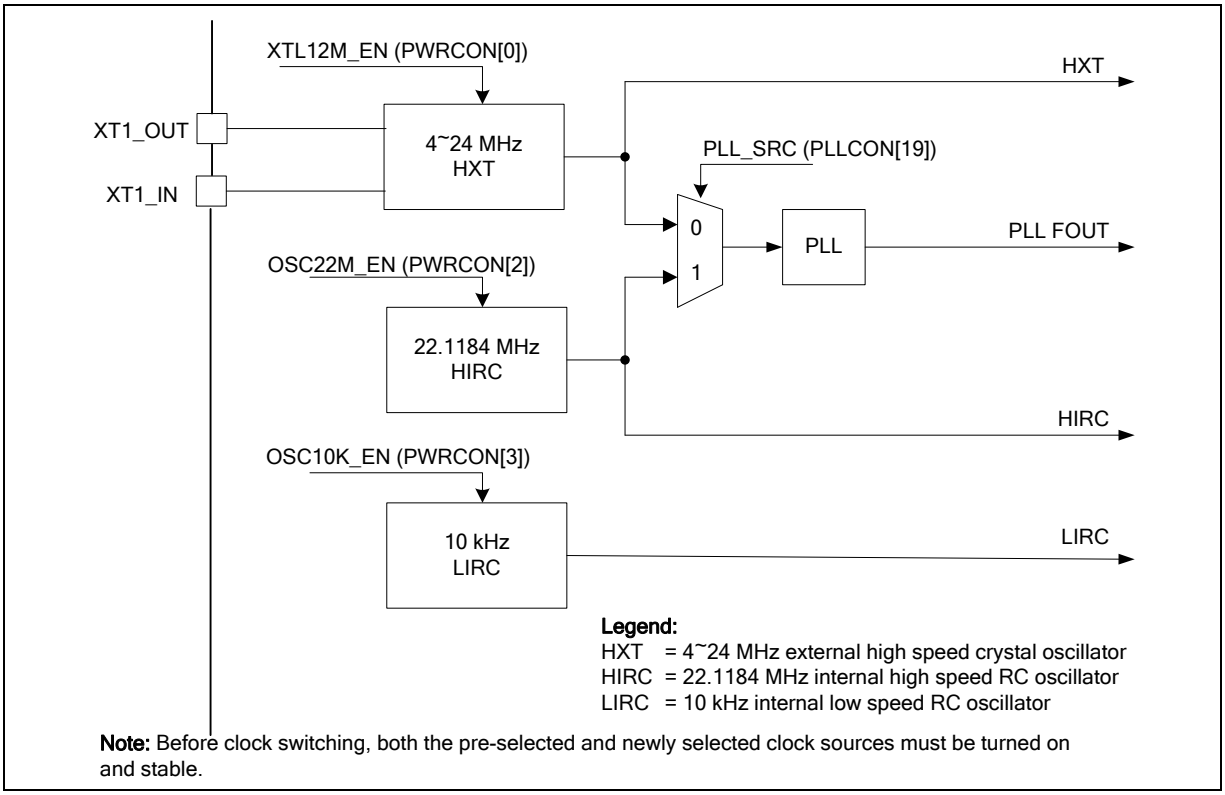
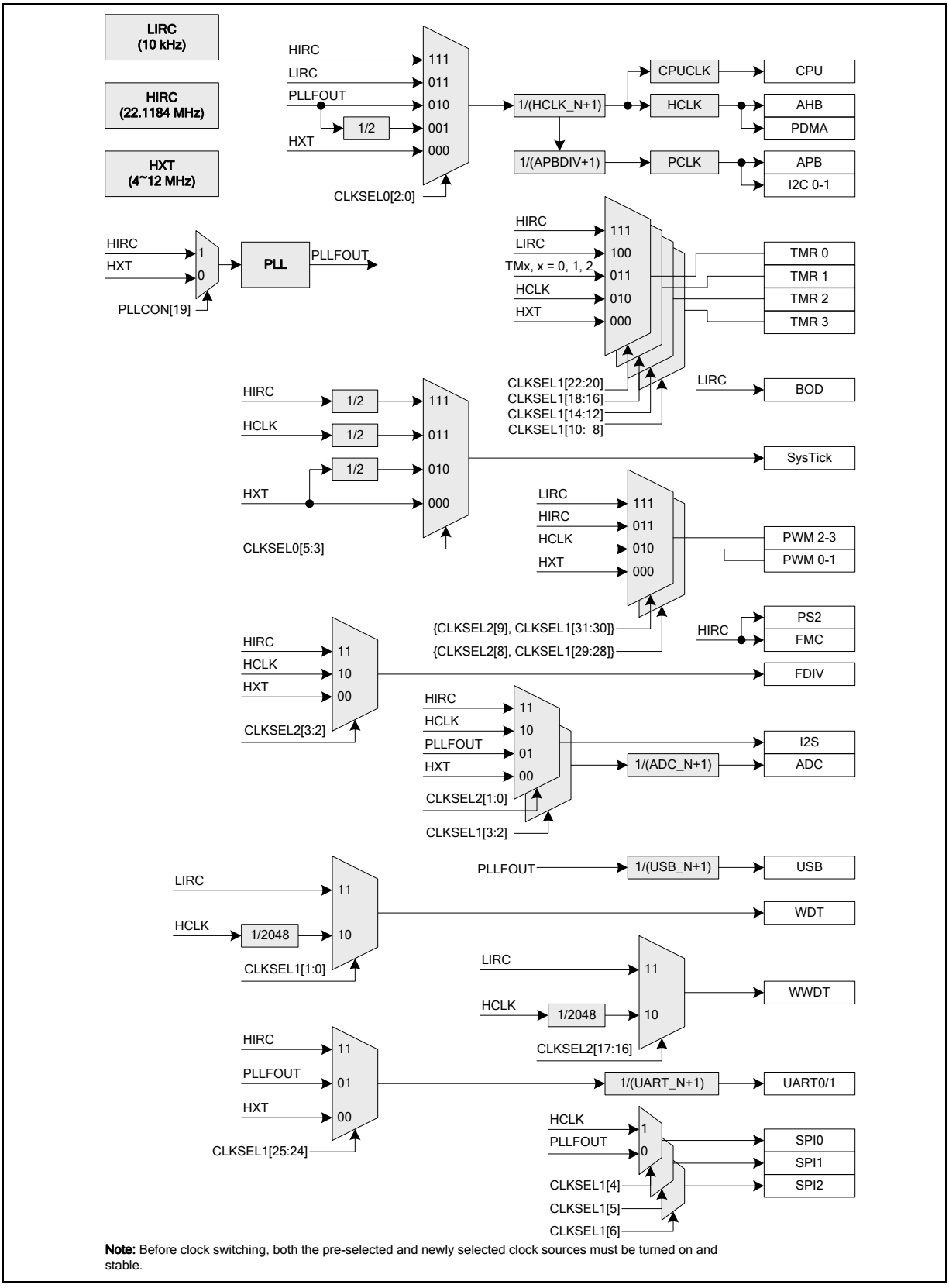


Figure 6-9 Clock Generator Global View Diagram



Note: Before clock switching, both the pre-selected and newly selected clock sources must be turned on and stable.

Figure 6-10 Clock Generator Global View Diagram

6.3.2 System Clock and SysTick Clock

The system clock has 5 clock sources which were generated from clock generator block. The clock source switch depends on the register HCLK_S (CLKSEL0[2:0]). The block diagram is shown in Figure 6-11.

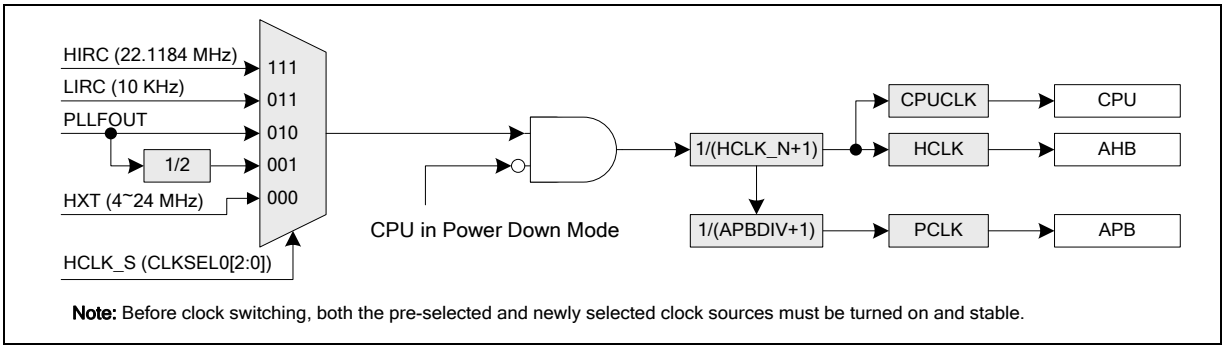


Figure 6-11 System Clock Block Diagram

The clock source of SysTick in Cortex®-M0 core can use CPU clock or external clock (SYST_CSR[2]). If using external clock, the SysTick clock (STCLK) has 4 clock sources. The clock source switch depends on the setting of the register STCLK_S (CLKSEL0[5:3]). The block diagram is shown in Figure 6-12.

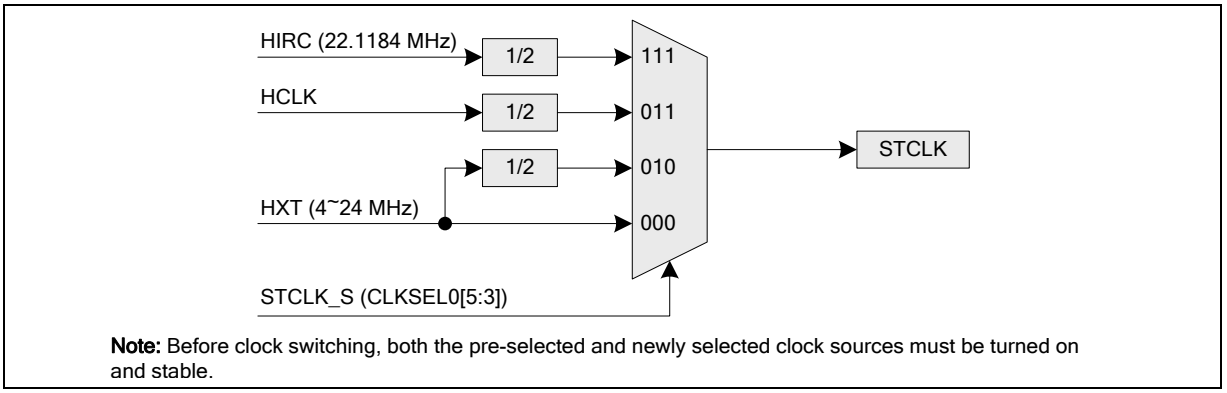


Figure 6-12 SysTick Clock Control Block Diagram

6.3.3 Peripherals Clock

The peripherals clock had different clock source switch setting depending on different peripherals. Please refer to the CLKSEL1 and CLKSEL2 register description in TRM.

6.3.4 Power-down Mode Clock

When chip enters into Power-down mode, system clocks, some clock sources, and some peripheral clocks will be disabled. Some clock sources and peripherals clock are still active in Power-down mode.

The clocks kept active are listed below:

- Clock Generator
  - Internal 10 kHz low speed oscillator clock

- WDT/Timer/PWM Peripherals Clock (when 10 kHz intertnal low speed RC oscillator (LIRC) is adopted as clock source)

6.3.5 Frequency Divider Output

This device is equipped with a power-of-2 frequency divider which is composed by16 chained divide-by-2 shift registers. One of the 16 shift register outputs selected by a sixteen to one multiplexer is reflected to CLKO function pin. Therefore there are 16 options of power-of-2 divided clocks with the frequency from $F_{in}/2^{1}$ to $F_{in}/2^{16}$ where Fin is input clock frequency to the clock divider.

The output formula is $\mathbf{F_{out} = F_{in}/2^{(N+1)}}$, where F_{in} is the input clock frequency, F_{out} is the clock divider output frequency and N is the 4-bit value in FSEL (FRQDIV[3:0]).

When writing 1 to DIVIDER_EN (FRQDIV[4]), the chained counter starts to count. When writing 0 to DIVIDER_EN (FRQDIV[4]), the chained counter continuously runs till divided clock reaches low state and stay in low state.

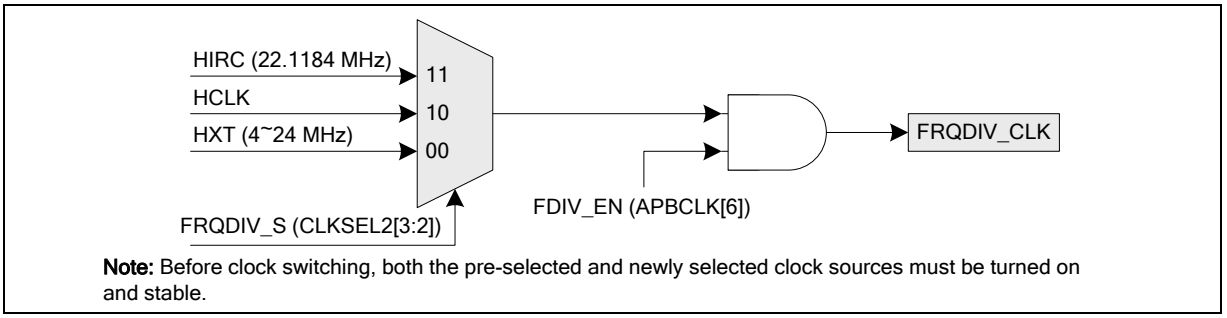


Figure 6-13 Clock Source of Frequency Divider

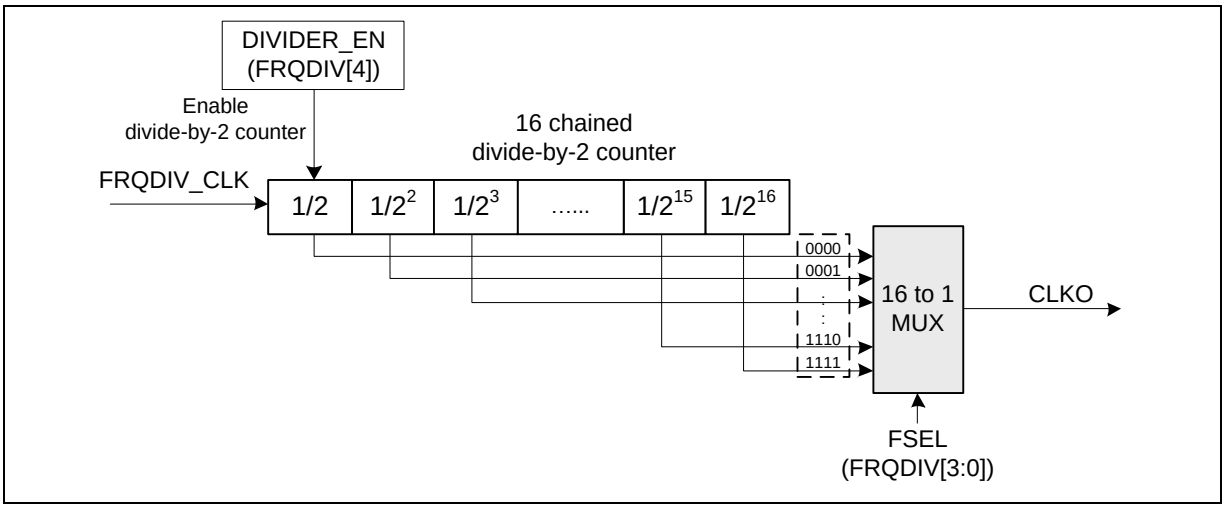


Figure 6-14 Block Diagram of Frequency Divider

6.4 Flash Memory Controller (FMC)

6.4.1 Overview

The NuMicro® NUC123 series is equipped with 68/36 Kbytes on-chip embedded flash for application program memory (APROM) and Data Flash, and 4 Kbytes for ISP loader program memory (LDROM) that could be programmed boot loader to update APROM and Data Flash through In-System-Programming (ISP) procedure. The ISP function enables user to update embedded flash when chip is soldered on PCB. After chip is powered on, Cortex®-M0 CPU fetches code from APROM or LDROM decided by boot select (CBS (Config0[7:6]). User can also select to enable or disable In-Application-Programming (IAP) function through boot select (CBS (Config0[7:6]). Also, the NUC123 provides Data Flash for user, to store some application dependent data before chip is powered off.

6.4.2 Features

- Runs up to 72 MHz and optional up to 50MHz with zero wait state for continuous address read access
- Supports 68/36 KB application program ROM (APROM)
- Supports 4 KB loader ROM (LDROM)
- Supports Data Flash with configurable memory size
- Supports 8 bytes User Configuration block to control system initiation
- Supports 512 bytes page erase for all embedded flash
- Supports In-System-Programming (ISP) / In-Application-Programming (IAP) to update embedded flash memory

6.5 General Purpose I/O (GPIO)

6.5.1 Overview

The NuMicro® NUC123 series has up to 47 General Purpose I/O pins shared with other function pins depending on the chip configuration. These 47 pins are arranged in 5 ports named GPIOA, GPIOB, GPIOC, GPIOD and GPIOF. GPIOA has 6 pins on PA[15:10]. GPIOB has 15 pins on PB[15:12] and PB[10:0]. GPIOC has 12 pins on PC[13:8] and PC[5:0]. GPIOD has 10 pins on PD[11:8] and PD[5:0]. GPIOF has 4 pins on PF[3:0]. Each one of the 47 pins is independent and has the corresponding register bits to control the pin mode function and data.

The I/O type of each of I/O pins can be configured by software individually as input, output, open-drain or quasi-bidirectional mode. After the chip is reset, the I/O mode of all pins are depending on CIOINI (Config0[10]) (NUC123xxxAEx Only). Each I/O pin has a very weakly individual pull-up resistor which is about 110 kΩ~300 kΩ for V_{DD} is from 5.0 V to 2.5 V.

6.5.2 Features

- Four I/O modes:
  - Quasi bi-direction
  - Push-Pull output
  - Open-Drain output
  - Input only with high impendence
- TTL/Schmitt trigger input selectable by GPx_TYPE[15:0] in GPx_MFP[31:16]
- I/O pin can be configured as interrupt source with edge/level setting
- Supports High Driver and High Sink I/O mode
- Configurable default I/O mode of all pins after reset by CIOINI (Config0[10]) setting (NUC123xxxAEx Only)
  - If CIOINI (Config[10]) is 0, all GPIO pins in input tri-state mode after chip reset
  - If CIOINI (Config[10]) is 1, all GPIO pins in Quasi-bidirectional mode after chip reset
- I/O pin internal pull-up resistor enabled only in Quasi-bidirectional I/O mode
- Enabling the pin interrupt function will also enable the wake-up function

6.6 PDMA Controller (PDMA)

6.6.1 Overview

The NuMicro® NUC123 contains a six-channel peripheral direct memory access (PDMA) controller and a cyclic redundancy check (CRC) generator.

The PDMA can transfer data to and from memory or transfer data to and from APB devices. For PDMA channel (PDMA CH0~CH5), there is one-word buffer as transfer buffer between the Peripherals APB devices and Memory. The CPU can recognize the completion of a PDMA operation by software polling or when it receives an internal PDMA interrupt. The PDMA controller can increase source or destination address or fixed them as well.

The PDMA controller contains a cyclic redundancy check (CRC) generator that can perform CRC calculation with programmable polynomial settings. The CRC engine supports CPU PIO mode and PDMA transfer mode.

6.6.2 Features

- Supports six PDMA channels and one CRC channel; each PDMA channel can support a unidirectional transfer
- AMBA AHB master/slave interface compatible, for data transfer and register read/write
- Hardware round robin priority scheme. PDMA channel 0 has the highest priority
- PDMA
  - Peripheral-to-memory, memory-to-peripheral, and memory-to-memory transfer
  - Supports word/half-word/byte transfer data width from/to peripheral
  - Supports address direction: increment, fixed
  - Supports software, SPI, UART, ADC, PWM and I^2S request
- Cyclic Redundancy Check (CRC)
  - Supports four common polynomials CRC-CCITT, CRC-8, CRC-16, and CRC-32
    - CRC-CCITT: $X^{16} + X^{12} + X^5 + 1$
    - CRC-8: $X^8 + X^2 + X + 1$
    - CRC-16: $X^{16} + X^{15} + X^2 + 1$
    - CRC-32: $X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$
  - Programmable seed value
  - Supports programmable order reverse setting for input data and CRC checksum
  - Supports programmable 1's complement setting for input data and CRC checksum.
  - Supports CPU PIO mode or PDMA transfer mode
  - Supports 8/16/32-bit of data width in CPU PIO mode
    - 8-bit write mode: 1-AHB clock cycle operation
    - 16-bit write mode: 2-AHB clock cycle operation
    - 32-bit write mode: 4-AHB clock cycle operation

- Supports byte alignment transfer length in CRC PDMA mode

6.7 Timer Controller (TMR)

6.7.1 Overview

The Timer controller includes four 32-bit timers, Timer0 ~ Timer3, allowing user to easily implement a timer control for applications. The timer can perform functions, such as frequency measurement, delay timing, clock generation, and event counting by external input pins, and interval measurement by external capture pins.

6.7.2 Features

- Four sets of 32-bit timers with 24-bit up counter and one 8-bit prescale counter
- Independent clock source for each timer
- Provides one-shot, periodic, toggle-output and continuous counting operation modes
- 24-bit up counter value is readable through TDR (TDR[23:0])
- Supports event counting function
- 24-bit capture value is readable through TCAP (TCAP[23:0])
- Supports external capture pin event for interval measurement
- Supports external capture pin event to reset 24-bit up counter
- Supports chip wake-up from Idle/Power-down mode if a timer interrupt signal is generated

6.8 PWM Generator and Capture Timer (PWM)

6.8.1 Overview

The NuMicro® NUC123 series has 1 set of PWM group supporting 1 set of PWM generators which can be configured as 4 independent PWM outputs, PWM0~PWM3, or as 2 complementary PWM pairs, (PWM0, PWM1), (PWM2, PWM3) with two programmable dead-zone generators. PWM output function can be alternated to capture function.

Each PWM generator has one 8-bit prescaler, one clock divider with 5 divided frequencies (1, 1/2, 1/4, 1/8, 1/16), two PWM Timers including two clock selectors, two 16-bit PWM down-counters for PWM period control, two 16-bit comparators for PWM duty control and one dead-zone generator. The PWM generators provide four independent PWM interrupt flags which are set by hardware when the corresponding PWM period down counter reaches zero.

Each PWM interrupt source with its corresponding enable bit can cause CPU to request PWM interrupt. The PWM generators can be configured as one-shot mode to produce only one PWM cycle signal or auto-reload mode to output PWM waveform continuously. PWM can be used to trigger ADC when operation in center-aligned mode.

6.8.2 Features

PWM function:

- Up to 1 PWM group (PWMA) to support 4 PWM channels or 2 PWM paired channels
- Supports 8-bit prescaler from 1 to 255
- Up to 16-bit resolution PWM timer
- PWM timer supports down and up-down operation type
- One-shot or Auto-reload mode PWM
- PWM Interrupt request synchronized with PWM period or duty
- Supports dead-zone generator with 8-bit resolution for 2 PWM paired channels
- Supports trigger ADC on center point in center-aligned mode

Capture function:

- Supports 4 Capture input channels shared with 4 PWM output channels
- Supports rising or falling capture condition
- Supports rising or falling capture interrupt
- Supports PDMA transfer function for each channel

6.9 Watchdog Timer (WDT)

6.9.1 Overview

The purpose of Watchdog Timer (WDT) is to perform a system reset when system runs into an unknown state. This prevents system from hanging for an infinite period of time. Besides, this Watchdog Timer supports the function to wake-up system from Idle/Power-down mode.

6.9.2 Features

- 18-bit free running up counter for WDT time-out interval
- Selectable time-out interval (2^4 ~ 2^{18}) and the time-out interval is 1.6 ms ~ 26.214 s if WDT_CLK = 10 kHz.
- System kept in reset state for a period of (1 / WDT_CLK) * 63
- Supports selectable WDT reset delay period, including 1026、130、18 or 3 WDT_CLK reset delay period
- Supports to force WDT enabled after chip powered on or reset by setting CWDTEN in Config0 register
- Supports WDT time-out wake-up function only if WDT clock source is selected as 10 kHz.

6.10 Window Watchdog Timer (WWDT)

6.10.1 Overview

The Window Watchdog Timer is used to perform a system reset within a specified window period to prevent software run to uncontrollable status by any unpredictable condition. The 6-bit down counter value will stop to update when chip is in Idle or Power-down mode.

6.10.2 Features

- 6-bit down counter value WWDTCVAL (WWDTCVR[5:0]) and 6-bit compare value WINCMP (WWDTCR[21:16]) to make the WWDT time-out window period flexible
- Supports 4-bit value PERIODSEL (WWDTCR[11:8]) to programmable maximum 11-bit prescale counter period of WWDT counter

6.11 UART Interface Controller (UART)

6.11.1 Overview

The NuMicro® NUC123 series provides two channels of Universal Asynchronous Receiver/ Transmitters (UART). UART Controller performs Normal Speed UART and supports flow control function. The UART Controller performs a serial-to-parallel conversion on data received from the peripheral and a parallel-to-serial conversion on data transmitted from the CPU. Each UART Controller channel supports six types of interrupts. The UART controller also supports IrDA SIR and RS-485.

6.11.2 Features

- Full duplex, asynchronous communications
- Separates receive / transmit 16/16 bytes entry FIFO for data payloads
- Supports hardware auto flow control/flow control
- Programmable receiver buffer trigger level
- Supports programmable baud-rate generator for each channel individually
- Supports nCTS wake-up function
- Supports 8-bit receiver buffer time-out detection function
- UART0/UART1 served by the DMA controller
- Programmable transmitting data delay time between the last stop and the next start bit by setting DLY (UA_TOR [15:8])
- Supports break error, frame error, parity error and receive/transmit buffer overflow detect function
- Fully programmable serial-interface characteristics
  - Programmable number of data bit, 5-, 6-, 7-, 8-bit character
  - Programmable parity bit, even, odd, no parity or stick parity bit generation and detection
  - Programmable stop bit, 1, 1.5, or 2 stop bit generation
- Supports IrDA SIR function mode
  - Supports for 3/16-bit duration for normal mode
- Supports RS-485 function mode.
  - Supports RS-485 9-bit mode
  - Supports hardware or software direct enable to program nRTS pin to control RS-485 transmission direction

6.12 PS/2 Device Controller (PS2D)

6.12.1 Overview

PS/2 device controller provides basic timing control for PS/2 communication. All communication between the device and the host is managed through the CLK and DATA pins. Unlike PS/2 keyboard or mouse device controller, the received/transmit code needs to be translated as meaningful code by firmware. The device controller generates the CLK signal after receiving a request to send, but host has ultimate control over communication. DATA sent from the host to the device is read on the rising edge and DATA sent from device to the host is change after rising edge. A 16 bytes FIFO is used to reduce CPU intervention. Software can select 1 to 16 bytes for a continuous transmission.

6.12.2 Features

- Host communication inhibit and request to send detection
- Reception frame error detection
- Programmable 1 to 16 bytes transmit buffer to reduce CPU intervention
- Double buffer for data reception
- S/W override bus

6.13 I²C Serial Interface Controller (Master/Slave) (I²C)

6.13.1 Overview

I²C is a two-wire, bi-directional serial bus that provides a simple and efficient method of data exchange between devices. The I²C standard is a true multi-master bus including collision detection and arbitration that prevents data corruption if two or more masters attempt to control the bus simultaneously.

There are two sets of I²C controllers which support Power-down wake-up function.

6.13.2 Features

- Supports up to two I²C ports
- Master/Slave mode
- Bidirectional data transfer between masters and slaves
- Multi-master bus (no central master)
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
- Serial clock synchronization allow devices with different bit rates to communicate via one serial bus
- Built-in 14-bit time-out counter requesting the I²C interrupt if the I²C bus hangs up and timer-out counter overflows.
- Programmable clocks allow for versatile rate control
- Supports 7-bit addressing mode
- Supports multiple address recognition (four slave address with mask option)
- Supports Power-down wake-up function

6.14 Serial Peripheral Interface (SPI)

6.14.1 Overview

The Serial Peripheral Interface (SPI) applies to synchronous serial data communication and allows full duplex transfer. Devices communicate in Master/Slave mode with 4-wire bi-direction interface. This NuMicro® NUC123 series contains up to three sets of SPI controllers performing a serial-to-parallel conversion on data received from a peripheral device, and a parallel-to-serial conversion on data transmitted to a peripheral device. Each set of SPI controller can be configured as a Master or a Slave device.

This controller supports variable serial clock function for special application and it also supports 2-bit Transfer mode. The controller also supports PDMA function to access the data buffer and also supports Dual I/O transfer mode.

6.14.2 Features

- Up to three sets of SPI controllers
- Supports Master or Slave mode operation
- Supports 2-bit Transfer mode
- Supports Dual I/O transfer mode
- Configurable bit length of a transfer word from 8 to 32-bit
- Provide separate 8-layer depth transmit and receive FIFO buffers
- Supports MSB first or LSB first transfer sequence
- Up to two slave select lines in Master mode
- Supports Byte Reorder function
- Supports configurable suspend interval in Master mode
- Variable output serial clock frequency in Master mode
- Supports PDMA transfer
- Supports 3-Wire, no slave select signal, bi-direction interface

6.15 I²S Controller (I²S)

6.15.1 Overview

The I²S controller consists of IIS protocol to interface with external audio CODEC. Two 8 word depth FIFO buffers for read path and write path respectively and is capable of handling 8/16/24/32 bits word sizes. PDMA controller handles the data movement between FIFO and memory.

6.15.2 Features

- Operated as either Master or Slave
- Capable of handling 8, 16, 24 and 32 bits word
- Supports monaural and stereo audio data
- Supports four data format:
  - I²S data format
  - MSB justified data format
  - PCM mode A
  - PCM mode B
- Provides two 8 word depth FIFO buffers, one for transmitting and the other for receiving
- Generates interrupt requests when buffer levels cross a programmable boundary
- Supports PDMA transfer

6.16 USB Device Controller (USB)

6.16.1 Overview

There is one set of USB 2.0 full-speed device controller and transceiver in this device. It is compliant with USB 2.0 full-speed device specification and supports Control/Bulk/Interrupt/ Isochronous transfer types.

In this device controller, there are two main interfaces: APB bus and USB bus which comes from the USB PHY transceiver. For the APB bus, the CPU can program control registers through it. There are 512 bytes internal SRAM as data buffer in this controller. For IN or OUT transfer, it is necessary to write data to SRAM or read data from SRAM through the APB interface or SIE. User needs to set the effective starting address of SRAM for each endpoint buffer through buffer segmentation register (BUFSEGx).

There are 8 endpoints in this controller. Each of the endpoint can be configured as IN or OUT endpoint. All the operations including Control, Bulk, Interrupt and Isochronous transfer are implemented in this block. The block of ENDPOINT CONTROL is also used to manage the data sequential synchronization, endpoint state control, current start address, transaction status, and data buffer status for each endpoint.

There are four different interrupt events in this controller. They are the wake-up event, device plug-in or plug-out event, USB events, such as IN ACK, OUT ACK, and BUS events, such as suspend and resume, etc. Any event will cause an interrupt, and user just needs to check the related event flags in interrupt event status register (USB_INTSTS) to acknowledge what kind of interrupt occurring, and then check the related USB Endpoint Status Register (USB_EPSTS) to acknowledge what kind of event occurring in this endpoint.

A software-disable function is also supported for this USB controller. It is used to simulate the disconnection of this device from the host. If user enables DRVSE0 bit (USB_DRVSE0), the USB controller will force the output of USB_D+ and USB_D- to level low and its function is disabled. After disable the DRVSE0 bit, host will enumerate this USB device again.

For more information on the Universal Serial Bus, please refer to *Universal Serial Bus Specification Revision 1.1.*

6.16.2 Features

- Compliant with USB 2.0 Full-Speed specification
- Provides 1 interrupt vector with 4 different interrupt events (WAKEUP, FLDET, USB and BUS)
- Supports Control/Bulk/Interrupt/Isochronous transfer types
- Supports suspend function when no bus activity existing for 3 ms
- Provides 8 endpoints for configurable Control/Bulk/Interrupt/Isochronous transfer types and maximum 512 bytes buffer size
- Provides remote wake-up capability

6.17 Analog-to-Digital Converter (ADC)

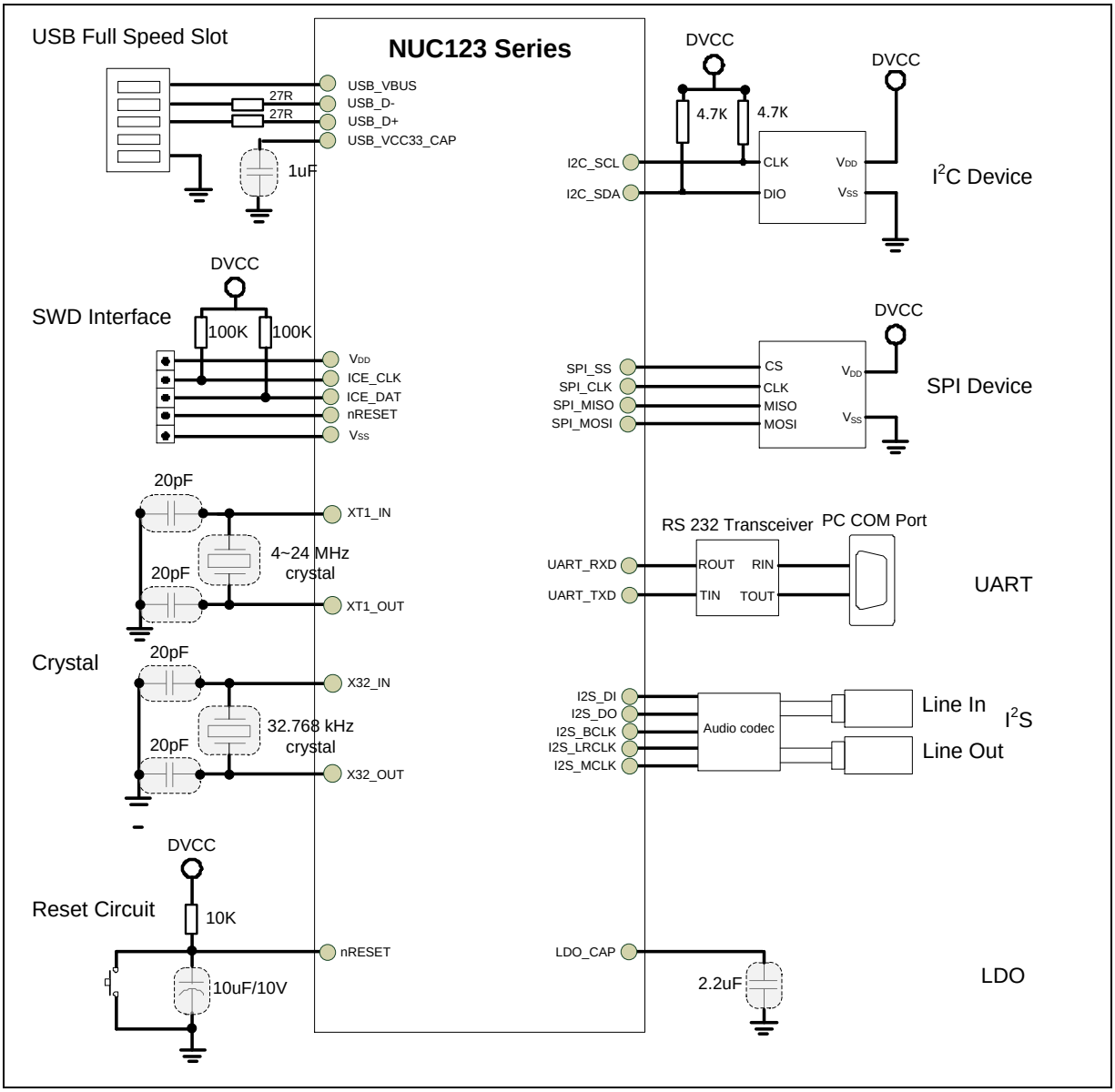
6.17.1 Overview

NuMicro® NUC123 Series contains one 10-bit successive approximation analog-to-digital converters (SAR A/D converter) with 8 input channels. The A/D converter supports three operation modes: single, single-cycle scan and continuous scan mode. The A/D converters can be started by software, PWM center-aligned trigger and external STADC pin.

6.17.2 Features

- Conversion range : 0 to AV_{DD}
- 10-bit resolution and 8-bit accuracy is guaranteed
- Up to 8 single-end analog input channels
- Maximum ADC clock frequency as 6 MHz (NUC123xxxANx Only)
- Maximum ADC clock frequency as 3 MHz (NUC123xxxAEx Only)
- Up to 166 kSPS (Samples Per Second) conversion rate (NUC123xxxANx Only)
- Up to 200 kSPS (Samples Per Second) conversion rate (NUC123xxxAEx Only)
- Three operating modes
  - Single mode: A/D conversion is performed one time on a specified channel
  - Single-cycle Scan mode: A/D conversion is performed one cycle on all specified channels with the sequence from the lowest numbered channel to the highest numbered channel
  - Continuous Scan mode: A/D converter continuously performs Single-cycle scan mode until software stops A/D conversion
- A/D conversion started by:
  - Software writes 1 to ADST bit
  - External pin STADC (PB.8)
  - PWM center-aligned trigger
- Supports 8 data registers to stored conversion result with valid and overrun indicators
- Supports 2 sets of digital comparators to monitor conversion result of specified channel and to generate an interrupt when conversion result matches comparison condition
- Channel 7 supports 2 input sources: external analog voltage and internal band-gap voltage
- Supports PDMA transfer

7 PERIPHERAL APPLICATION SCHEME



Note 1: It is recommended to use 100 kΩ pull-up resistor on both ICE_DAT and ICE_CLK pin.

Note 2: It is recommended to use 10 kΩ pull-up resistor and 10 μF capacitor on nRESET pin.

8 ELECTRICAL CHARACTERISTICS (NUC123XXXANX)

8.1 Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
$V_{DD} - V_{SS}$	DC Power Supply	-0.3	+7.0	V
V_{IN}	Input Voltage	V_{SS} - 0.3	V_{DD} + 0.3	V
$1/t_{CLCL}$	Oscillator Frequency	4	24	MHz
T_A	Operating Temperature	-40	+85	°C
T_{ST}	Storage Temperature	-55	+150	°C
I_{DD}	Maximum Current into V_{DD}	-	120	mA
I_{SS}	Maximum Current out of V_{SS}		120	mA
I_{IO}	Maximum Current sunk by a I/O pin		35	mA
	Maximum Current sourced by a I/O pin		35	mA
	Maximum Current sunk by total I/O pins		100	mA
	Maximum Current sourced by total I/O pins		100	mA

Note: Exposure to conditions beyond those listed under absolute maximum ratings may adversely affect the lift and reliability of the device.

8.2 DC Electrical Characteristics

(V_{DD} -V_{SS} = 5.5 V, TA = 25°C)

PARAMETER	SYM	SPECIFICATIONS				TEST CONDITIONS
		MIN	TYP	MAX	UNIT	
Operation voltage	V_{DD}	2.5		5.5	V	V_{DD} = 2.5V ~ 5.5V up to 72 MHz
V_{DD} rise rate to ensure internal operation correctly	V_{RISE}	0.05			V/ms	
Power ground	V_{SS} AV_{SS}	-0.3			V	
LDO output voltage	V_{LDO}	1.62	1.8	1.98	V	V_{DD} > 2.5V
Analog operating voltage	AV_{DD}	0	V_{DD}		V	When system uses analog function, please refer to chapter 7.4 for corresponding analog operating voltage
Operating current Normal Run mode at 72 MHz	I_{DD1}		36		mA	V_{DD} = 5.5V at 72 MHz, All IP and PLL Enabled, XTAL = 12 MHz
	I_{DD2}		21		mA	V_{DD} = 5.5V at 72 MHz, All IP Disabled and PLL Enabled, XTAL = 12 MHz
	I_{DD3}		35		mA	V_{DD} = 3V at 72 MHz, All IP and PLL enabled, XTAL = 12 MHz
	I_{DD4}		20		mA	V_{DD} = 3V at 72 MHz, All IP Disabled and PLL Enabled, XTAL = 12 MHz
Operating current Normal Run mode at 12 MHz	I_{DD5}		7		mA	V_{DD} = 5.5V at 12 MHz, All IP Enabled and PLL Disabled, XTAL = 12 MHz
	I_{DD6}		4		mA	V_{DD} = 5.5V at 12 MHz, All IP and PLL Disabled, XTAL = 12 MHz
	I_{DD7}		6		mA	V_{DD} = 3V at 12 MHz, All IP Enabled and PLL Disabled, XTAL = 12 MHz
	I_{DD8}		3		mA	V_{DD} = 3V at 12 MHz, All IP and PLL Disabled, XTAL = 12 MHz
Operating current Normal Run mode	I_{DD9}		4		mA	V_{DD} = 5V at 4 MHz, All IP Enabled and PLL Disabled, XTAL = 4 MHz

PARAMETER	SYM	SPECIFICATIONS				TEST CONDITIONS
		MIN	TYP	MAX	UNIT	
at 4 MHz	I_{DD10}		3		mA	V_{DD} = 5V at 4 MHz, All IP and PLL Disabled, XTAL = 4 MHz
	I_{DD11}		4		mA	V_{DD} = 3V at 4 MHz, All IP Enabled and PLL Disabled, XTAL = 4 MHz
	I_{DD12}		2		mA	V_{DD} = 3V at 4 MHz, All IP and PLL Disabled, XTAL = 4 MHz
Operating current Idle mode at 72 MHz	I_{IDLE1}		29		mA	V_{DD} = 5.5V at 72 MHz, All IP and PLL Enabled, XTAL = 12 MHz
	I_{IDLE2}		14		mA	V_{DD} = 5.5V at 72 MHz, All IP Disabled and PLL Enabled, XTAL = 12 MHz
	I_{IDLE3}		28		mA	V_{DD} = 3V at 72 MHz, All IP and PLL Enabled, XTAL = 12 MHz
	I_{IDLE4}		13		mA	V_{DD} = 3V at 72 MHz, All IP Disabled and PLL Enabled, XTAL=12 MHz
Operating current Idle mode at 12 MHz	I_{IDLE5}		6		mA	V_{DD} = 5.5V at 12 MHz, All IP Enabled and PLL Disabled, XTAL = 12 MHz
	I_{IDLE6}		3		mA	V_{DD} = 5.5V at 12 MHz, All IP and PLL Disabled, XTAL = 12 MHz
	I_{IDLE7}		5		mA	V_{DD} = 3V at 12 MHz, All IP Enabled and PLL Disabled, XTAL = 12 MHz
	I_{IDLE8}		2		mA	V_{DD} = 3 V at 12 MHz, All IP and PLL Disabled, XTAL = 12 MHz
Operating current Idle mode at 4 MHz	I_{IDLE9}		3		mA	V_{DD} = 5V at 4 MHz, All IP Enabled and PLL Disabled, XTAL = 4 MHz
	I_{IDLE10}		2		mA	V_{DD} = 5V at 4 MHz, All IP and PLL Disabled, XTAL = 4 MHz
	I_{IDLE11}		2		mA	V_{DD} = 3V at 4 MHz, All IP Enabled and PLL Disabled, XTAL = 4 MHz
	I_{IDLE12}		1		mA	V_{DD} = 3V at 4 MHz, All IP and PLL Disabled, XTAL = 4 MHz

PARAMETER	SYM	SPECIFICATIONS				TEST CONDITIONS
		MIN	TYP	MAX	UNIT	
Operating current Idle mode at 10 kHz	I_{IDLE5}		131		μA	V_{DD} = 5.5V at 10 kHz, All IP Enabled and PLL Disabled, LIRC 10 kHz Enabled
	I_{IDLE6}		129		μA	V_{DD} = 5.5V at 10 kHz, All IP and PLL Disabled, LIRC 10 kHz Enabled
	I_{IDLE7}		125		μA	V_{DD} = 3V at 10 kHz, All IP Enabled and PLL Disabled, LIRC 10 kHz Enabled
	I_{IDLE8}		124		μA	V_{DD} = 3 V at 10 kHz, All IP and PLL Disabled, LIRC 10 kHz Enabled
Standby current Power-down mode	I_{PWD1}		12		μA	V_{DD} = 5.5V, No load when BOV function Disabled
	I_{PWD2}		9		μA	V_{DD} = 3.3V, No load when BOV function Disabled
Input Current PA, PB, PC, PD, PE, PF (Quasi-bidirectional mode)	I_{IN1}		-64		μA	V_{DD} = 5.5V, V_{IN} = 0V or V_{IN} = V_{DD}
Input Current at /RESET[1]	I_{IN2}	-55	-45	-30	μA	V_{DD} = 3.3V, V_{IN} = 0.45V
Input Leakage Current PA, PB, PC, PD, PE, PF	I_{LK}	-2	-	+2	μA	V_{DD} = 5.5V, 0 < V_{IN} < V_{DD}
Logic 1 to 0 Transition Current PA~PF (Quasi-bidirectional mode)	I_{TL} [3]	-650	-	-200	μA	V_{DD} = 5.5V, V_{IN} < 2.0V
Input Low Voltage PA, PB, PC, PD, PE, PF (TTL input)	V_{IL1}	-0.3	-	0.8	V	V_{DD} = 4.5V
		-0.3	-	0.6		V_{DD} = 2.5V
Input High Voltage PA, PB, PC, PD, PE, PF (TTL input)	V_{IH1}	2.0	-	V_{DD} +0.2	V	V_{DD} = 5.5V
		1.5	-	V_{DD} +0.2		V_{DD} = 3.0V
Input Low Voltage PA, PB, PC, PD, PE, PF (Schmitt input)	V_{IL2}	-0.5	-	0.35 V_{DD}	V	
Input High Voltage PA, PB, PC, PD, PE, PF (Schmitt input)	V_{IH2}	0.65 V_{DD}	-	V_{DD}+0.5	V	
Hysteresis voltage of PA~PE (Schmitt input)	V_{HY}		0.2 V_{DD}		V	
Input Low Voltage XT1[*2]	V_{IL3}	0	-	0.8	V	V_{DD} = 4.5V
		0	-	0.4		V_{DD} = 3.0V
Input High Voltage XT1[*2]	V_{IH3}	3.5	-	V_{DD} +0.2	V	V_{DD} = 5.5V
		2.4	-	V_{DD} +0.2		V_{DD} = 3.0V
Negative going threshold (Schmitt input), /RESET	V_{ILS}	-0.5	-	0.2 V_{DD}	V	
Positive going threshold (Schmitt input), /RESET	V_{IHS}	0.6 V_{DD}	-	V_{DD}+0.5	V	

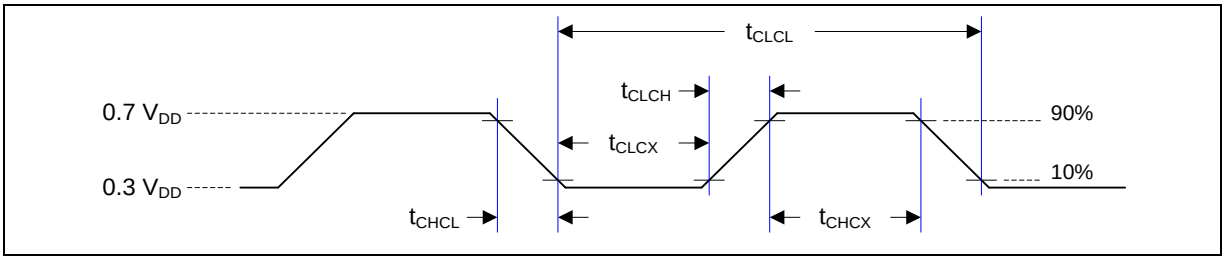
PARAMETER	SYM	SPECIFICATIONS				TEST CONDITIONS
		MIN	TYP	MAX	UNIT	
Source Current PA, PB, PC, PD, PE, PF (Quasi-bidirectional Mode)	I_{SR11}	-300	-370	-450	μA	V_{DD} = 4.5V, V_S = 2.4V
	I_{SR12}	-50	-70	-90	μA	V_{DD} = 2.7V, V_S = 2.2V
	I_{SR12}	-40	-60	-80	μA	V_{DD} = 2.5V, V_S = 2.0V
Source Current PA, PB, PC, PD, PE, PF (Push-pull Mode)	I_{SR21}	-20	-24	-28	mA	V_{DD} = 4.5V, V_S = 2.4V
	I_{SR22}	-4	-6	-8	mA	V_{DD} = 2.7V, V_S = 2.2V
	I_{SR22}	-3	-5	-7	mA	V_{DD} = 2.5V, V_S = 2.0V
Sink Current PA, PB, PC, PD, PE, PF (Quasi-bidirectional and Push-pull Mode)	I_{SK1}	10	16	20	mA	V_{DD} = 4.5V, V_S = 0.45V
	I_{SK1}	7	10	13	mA	V_{DD} = 2.7V, V_S = 0.45V
	I_{SK1}	6	9	12	mA	V_{DD} = 2.5V, V_S = 0.45V
Brown-out voltage with BOV_VL [1:0] =00b	$V_{BO2.2}$	2.1	2.2	2.3	V	
Brown-out voltage with BOV_VL [1:0] =01b	$V_{BO2.7}$	2.6	2.7	2.8	V	
Brown-out voltage with BOV_VL [1:0] =10b	$V_{BO3.8}$	3.7	3.8	3.9	V	
Brown-out voltage with BOV_VL [1:0] =11b	$V_{BO4.5}$	4.4	4.5	4.6	V	
Hysteresis range of BOD voltage	V_{BH}	30	-	150	mV	V_{DD} = 2.5V - 5.5V

Notes:

1. nRESET pin is a Schmitt trigger input.
2. Crystal Input is a CMOS input.
3. Pins of PA, PB, PC, PD and PE can source a transition current when they are being externally driven from 1 to 0. In the condition of V_{DD}=5.5 V, 5he transition current reaches its maximum value when V_{IN} approximates to 2V.

8.3 AC Electrical Characteristics

8.3.1 External 4~24 MHz High Speed Oscillator



Note: Duty cycle is 50%.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
t_{CHCX}	Clock High Time		10	-	-	ns
t_{CLCX}	Clock Low Time		10	-	-	ns
t_{CLCH}	Clock Rise Time		2	-	15	ns
t_{CHCL}	Clock Fall Time		2	-	15	ns

8.3.2 External 4~24 MHz High Speed Crystal

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Input clock frequency	External crystal	4	12	24	MHz
Temperature	-	-40	-	85	°C
V_{DD}	-	2.5	5	5.5	V

8.3.2.1 Typical Crystal Application Circuits

CRYSTAL	C1	C2	R
4 MHz ~ 24 MHz	10~20 pF	10~20 pF	without

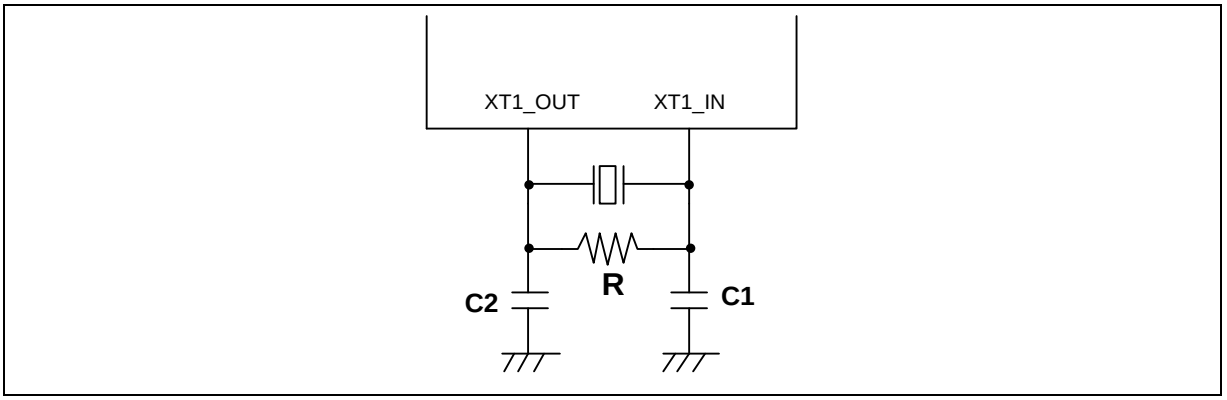


Figure 8-1 Typical Crystal Application Circuit

8.3.3 Internal 22.1184 MHz High Speed Oscillator

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Supply voltage[1]	-	2.5	-	5.5	V
Center Frequency	-	-	22.1184	-	MHz
Calibrated Internal Oscillator Frequency	+25°C; V_{DD} =5 V	-1	-	+1	%
	-40°C~+85°C; V_{DD} =2.5 V~5.5 V	-3	-	+3	%
Operation Current	V_{DD} =5 V	-	500	-	μA

8.3.4 Internal 10 kHz Low Speed Oscillator

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Supply voltage[1]	-	2.5	-	5.5	V
Center Frequency	-	-	10	-	kHz
Calibrated Internal Oscillator Frequency	+25°C; V_{DD} =5 V	-30	-	+30	%
	-40°C~+85°C; V_{DD}=2.5 V~5.5 V	-50	-	+50	%

Note: Internal operation voltage comes from LDO.

8.4 Analog Characteristics

8.4.1 10-bit SARADC Specifications

PARAMETER	SYM	SPECIFICATIONS				TEST CONDITIONS
		MIN	TYP	MAX	UNIT	
Operating Voltage	AV_{DD}	2.7		5.5	V	$AV_{DD} = V_{DD}$
Operating Current	I_{ADC}			1.5	mA	$AV_{DD} = V_{DD} = 5V$, $F_{SPS} = 150k$
Resolution	R_{ADC}			10	bit	
Reference Voltage	V_{REF}		AV_{DD}		V	V_{REF} Connected to AV_{DD} in Chip
ADC input Voltage	V_{IN}	0		AV_{DD}	V	
Sampling Rate	F_{SPS}	150k			Hz	V_{DD} = 5V, ADC Clock = 6 MHz Free Running Conversion
Integral Non-linearity Error (INL)	INL			±1	LSB	
Differential Non-linearity Error (DNL)	DNL			±1	LSB	
Gain Error	E_G			±2	LSB	
Offset Error	E_{OFFSET}		3		LSB	
Absolute Error	E_{ABS}		4		LSB	
ADC Clock Frequency	F_{ADC}	100k		6M	Hz	V_{DD} = 5V
Clock Cycle	AD_{CYC}	36			Cycle	

8.4.2 LDO and Power Management Specifications

PARAMETER	MIN	TYP	MAX	UNIT	NOTE
Input Voltage	2.5	5	5.5	V	V_{DD} input voltage
Output Voltage	1.62	1.8	1.98	V	V_{DD} > 2.5V
Temperature	-40	25	85	°C	
Cbp	-	1	-	µF	Resr = 1Ω

Notes:

1. It is recommended that a 10 µF or higher capacitor and a 100nF bypass capacitor are connected between V_{DD} and the closest V_{SS} pin of the device.

2. To ensure power stability, a 1 µF (Cbp) or higher capacitor must be connected between LDO pin and the closest VSS pin of the device.

8.4.3 Low Voltage Reset Specifications

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Operation voltage	-	1.7	-	5.5	V
Quiescent current	V_{DD} = 5.5 V	-	-	5	μA
Temperature	-	-40	25	85	°C
Threshold voltage	Temperature = 25°C	1.7	2.0	2.3	V
	Temperature = -40°C	-	2.4	-	V
	Temperature = 85°C	-	1.6	-	V
Hysteresis	-	0	0	0	V

8.4.4 Brown-out Detector Specifications

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Operation voltage	-	2.5	-	5.5	V
Quiescent current	AV_{DD} = 5.5 V	-	-	125	μA
Temperature	-	-40	25	85	°C
Brown-out voltage	BOV_VL[1:0] = 11	4.4	4.5	4.6	V
	BOV_VL [1:0] = 10	3.7	3.8	3.9	V
	BOV_VL [1:0] = 01	2.6	2.7	2.8	V
	BOV_VL [1:0] = 00	2.1	2.2	2.3	V
Hysteresis	-	30	-	150	mV

8.4.5 Power-On Reset (5V) Specifications

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Temperature	-	-40	25	85	°C
Reset voltage	V+	-	2	-	V
Quiescent current	Vin>reset voltage	-	1	-	nA

8.4.6 USB PHY Specifications

8.4.6.1 USB DC Electrical Characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	Input high (driven)		2.0			V
V_{IL}	Input low				0.8	V
V_{DI}	Differential input sensitivity	|PADP-PADM|	0.2			V
V_{CM}	Differential common-mode range	Includes V_{DI} range	0.8		2.5	V
V_{SE}	Single-ended receiver threshold		0.8		2.0	V
	Receiver hysteresis			200		mV
V_{OL}	Output low (driven)		0		0.3	V
V_{OH}	Output high (driven)		2.8		3.6	V
V_{CRS}	Output signal cross voltage		1.3		2.0	V
R_{PU}	Pull-up resistor		1.425		1.575	kΩ
R_{PD}	Pull-down resistor		14.25		15.75	kΩ
V_{TRM}	Termination Voltage for upstream port pull up (RPU)		3.0		3.6	V
Z_{DRV}	Driver output resistance	Steady state drive*		10		Ω
C_{IN}	Transceiver capacitance	Pin to GND			20	pF

Note: Driver output resistance doesn't include series resistor resistance.

8.4.6.2 USB Full-Speed Driver Electrical Characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
T_{FR}	Rising time	C_L = 50p	4		20	ns
T_{FF}	Falling time	C_L = 50p	4		20	ns
T_{FRFF}	Rising and falling time matching	$T_{FRFF} = T_{FR}/T_{FF}$	90		111.11	%

8.4.6.3 USB Power Dissipation

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
I_{VBUS}	VBUS current (steady state)	Standby		50		μA

8.4.6.4 USB LDO Specification

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{BUS}	VBUS Pin Input Voltage		4.0	5.0	5.5	V
V_{DD33}	LDO Output Voltage		3.0	3.3	3.6	V
C_{bp}	External Bypass Capacitor			1.0	-	μF

8.5 Flash DC Electrical Characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	Supply voltage		1.62	1.8	1.98	V[1]
T_{RET}	Data Retention	Temp=85 °C	10			year
T_{ERASE}	Page Erase Time			20		ms
T_{MER}	Mass Erase Time			40		ms
T_{PROG}	Program Time			40		μs
I_{DD1}	Read Current				0.25	mA
I_{DD2}	Program/Erase Current				7	mA
I_{PD}	Power Down Current			1	20	μA

Note: V_{DD} is source from chip LDO output voltage.

8.6 SPI Dynamic Characteristics

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
SPI Master mode (V_{DD} = 4.5V ~ 5.5V, 30 pF loading Capacitor)					
t_{DS}	Data setup time	TBD	TBD	-	ns
t_{DH}	Data hold time	TBD	-	-	ns
t_V	Data output valid time	-	TBD	TBD	ns
SPI Master mode (V_{DD} = 3.0V ~ 3.6V, 30 pF loading Capacitor)					
t_{DS}	Data setup time	TBD	TBD	-	ns
t_{DH}	Data hold time	TBD	-	-	ns
t_V	Data output valid time	-	TBD	TBD	ns
SPI Slave mode (V_{DD} = 4.5V ~ 5.5V, 30 pF loading Capacitor)					
t_{DS}	Data setup time	TBD	-	-	ns
t_{DH}	Data hold time	TBD	-	-	ns
t_V	Data output valid time	-	TBD	TBD	ns
SPI Slave mode (V_{DD} = 3.0V ~ 3.6V, 30 pF loading Capacitor)					
t_{DS}	Data setup time	TBD	-	-	ns
t_{DH}	Data hold time	TBD	-	-	ns
t_V	Data output valid time	-	TBD	TBD	ns

TBD: To be defined.

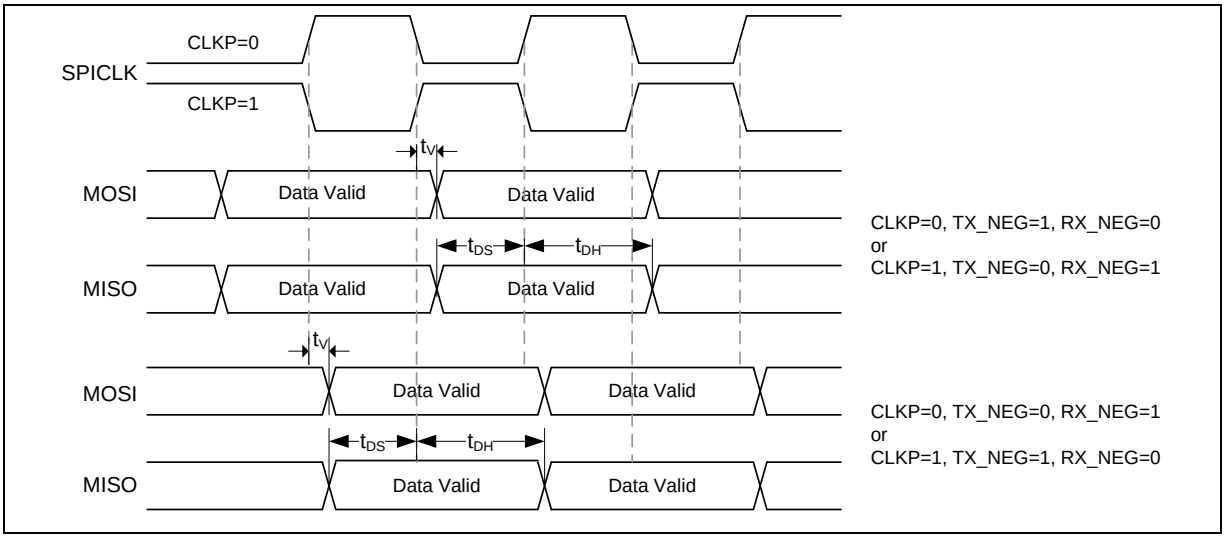


Figure 8-2 SPI Master Dynamic Characteristics Timing

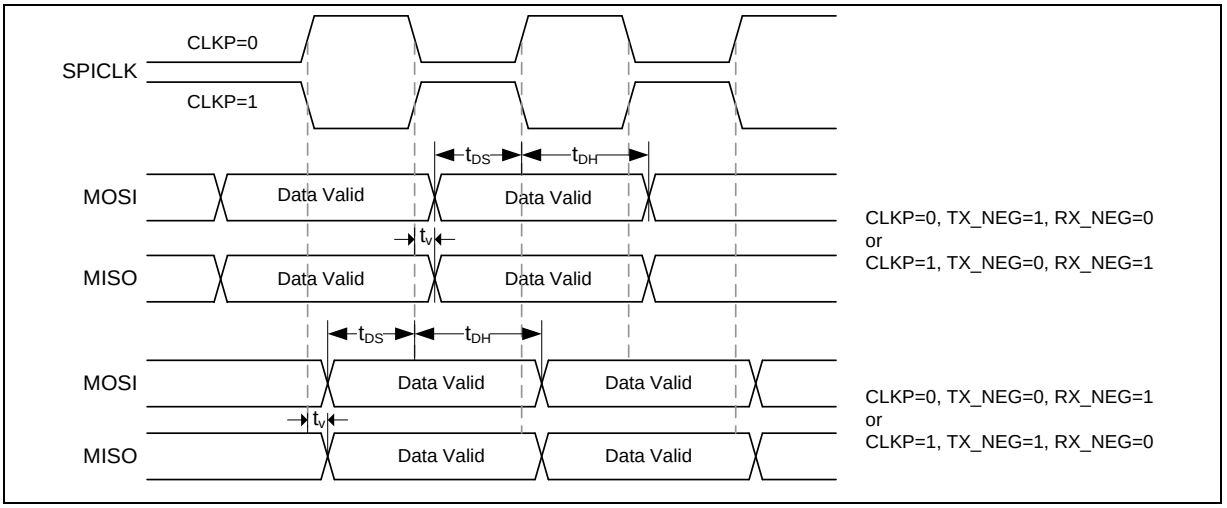


Figure 8-3 SPI Slave Dynamic Characteristics Timing

9 ELECTRICAL CHARACTERISTICS (NUC123XXXAEX)

9.1 Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
$V_{DD} - V_{SS}$	DC Power Supply	-0.3	+7.0	V
V_{IN}	Input Voltage	V_{SS} - 0.3	V_{DD} + 0.3	V
$1/t_{CLCL}$	Oscillator Frequency	4	24	MHz
T_A	Operating Temperature	-40	+105	°C
T_{ST}	Storage Temperature	-55	+150	°C
I_{DD}	Maximum Current into V_{DD}	-	120	mA
I_{SS}	Maximum Current out of V_{SS}		120	mA
I_{IO}	Maximum Current sunk by a I/O pin		35	mA
	Maximum Current sourced by a I/O pin		35	mA
	Maximum Current sunk by total I/O pins		100	mA
	Maximum Current sourced by total I/O pins		100	mA

Note: Exposure to conditions beyond those listed under absolute maximum ratings may adversely affect the lift and reliability of the device.

9.2 DC Electrical Characteristics

(V_{DD}-V_{SS}=2.5 ~ 5.5 V, T_A = 25°C)

PARAMETER	SYM	SPECIFICATIONS				TEST CONDITIONS
		MIN	TYP	MAX	UNIT	
Operation voltage	V_{DD}	2.5		5.5	V	V_{DD} = 2.5V ~ 5.5V up to 72 MHz
V_{DD} rise rate to ensure internal operation correctly	V_{RISE}	0.05			V/ms	
Power ground	V_{SS} AV_{SS}	-0.3			V	
LDO output voltage	V_{LDO}	1.62	1.8	1.98	V	V_{DD} > 2.5V
Analog operating voltage	AV_{DD}	0	V_{DD}		V	
Operating current Normal Run mode at 72 MHz	I_{DD1}		39		mA	V_{DD} = 5.5V at 72 MHz, All IP and PLL Enabled, XTAL = 12 MHz
	I_{DD2}		24		mA	V_{DD} = 5.5V at 72 MHz, All IP Disabled and PLL Enabled, XTAL = 12 MHz
	I_{DD3}		37		mA	V_{DD} = 3V at 72 MHz, All IP and PLL enabled, XTAL = 12 MHz
	I_{DD4}		23		mA	V_{DD} = 3V at 72 MHz, All IP Disabled and PLL Enabled, XTAL = 12 MHz
Operating current Normal Run mode at 12 MHz	I_{DD5}		10		mA	V_{DD} = 5.5V at 12 MHz, All IP Enabled and PLL Disabled, XTAL = 12 MHz
	I_{DD6}		7		mA	V_{DD} = 5.5V at 12 MHz, All IP and PLL Disabled, XTAL = 12 MHz
	I_{DD7}		8		mA	V_{DD} = 3V at 12 MHz, All IP Enabled and PLL Disabled, XTAL = 12 MHz
	I_{DD8}		6		mA	V_{DD} = 3V at 12 MHz, All IP and PLL Disabled, XTAL = 12 MHz
Operating current Normal Run mode	I_{DD9}		6		mA	V_{DD} = 5V at 4 MHz, All IP Enabled and PLL Disabled, XTAL = 4 MHz

PARAMETER	SYM	SPECIFICATIONS				TEST CONDITIONS
		MIN	TYP	MAX	UNIT	
at 4 MHz	I_{DD10}		5		mA	V_{DD} = 5V at 4 MHz, All IP and PLL Disabled, XTAL = 4 MHz
	I_{DD11}		4		mA	V_{DD} = 3V at 4 MHz, All IP Enabled and PLL Disabled, XTAL = 4 MHz
	I_{DD12}		3		mA	V_{DD} = 3V at 4 MHz, All IP and PLL Disabled, XTAL = 4 MHz
Operating current Idle mode at 72 MHz	I_{IDLE1}		28		mA	V_{DD} = 5.5V at 72 MHz, All IP and PLL Enabled, XTAL = 12 MHz
	I_{IDLE2}		12		mA	V_{DD} = 5.5V at 72 MHz, All IP Disabled and PLL Enabled, XTAL = 12 MHz
	I_{IDLE3}		25		mA	V_{DD} = 3V at 72 MHz, All IP and PLL Enabled, XTAL = 12 MHz
	I_{IDLE4}		10		mA	V_{DD} = 3V at 72 MHz, All IP Disabled and PLL Enabled, XTAL=12 MHz
Operating current Idle mode at 12 MHz	I_{IDLE5}		6		mA	V_{DD} = 5.5V at 12 MHz, All IP Enabled and PLL Disabled, XTAL = 12 MHz
	I_{IDLE6}		3		mA	V_{DD} = 5.5V at 12 MHz, All IP and PLL Disabled, XTAL = 12 MHz
	I_{IDLE7}		5		mA	V_{DD} = 3V at 12 MHz, All IP Enabled and PLL Disabled, XTAL = 12 MHz
	I_{IDLE8}		2		mA	V_{DD} = 3 V at 12 MHz, All IP and PLL Disabled, XTAL = 12 MHz
Operating current Idle mode at 4 MHz	I_{IDLE9}		5		mA	V_{DD} = 5V at 4 MHz, All IP Enabled and PLL Disabled, XTAL = 4 MHz
	I_{IDLE10}		4		mA	V_{DD} = 5V at 4 MHz, All IP and PLL Disabled, XTAL = 4 MHz
	I_{IDLE11}		3		mA	V_{DD} = 3V at 4 MHz, All IP Enabled and PLL Disabled, XTAL = 4 MHz
	I_{IDLE12}		2		mA	V_{DD} = 3V at 4 MHz, All IP and PLL Disabled, XTAL = 4 MHz

PARAMETER	SYM	SPECIFICATIONS				TEST CONDITIONS
		MIN	TYP	MAX	UNIT	
Operating current Idle mode at 10 kHz	I_{IDLE5}		110		μA	V_{DD} = 5.5V at 10 kHz, All IP Enabled and PLL Disabled, LIRC 10 kHz Enabled
	I_{IDLE6}		110		μA	V_{DD} = 5.5V at 10 kHz, All IP and PLL Disabled, LIRC 10 kHz Enabled
	I_{IDLE7}		100		μA	V_{DD} = 3V at 10 kHz, All IP Enabled and PLL Disabled, LIRC 10 kHz Enabled
	I_{IDLE8}		100		μA	V_{DD} = 3 V at 10 kHz, All IP and PLL Disabled, LIRC 10 kHz Enabled
Standby current Power-down mode	I_{PWD1}		15		μA	V_{DD} = 5.5V, No load when BOV function Disabled
	I_{PWD2}		13		μA	V_{DD} = 3.3V, No load when BOV function Disabled
Input Current PA, PB, PC, PD, PE, PF (Quasi-bidirectional mode)	I_{IN1}		-64		μA	V_{DD} = 5.5V, V_{IN} = 0V
Input Current at /RESET[1]	I_{IN2}	-55	-45	-30	μA	V_{DD} = 3.3V, V_{IN} = 0.45V
Input Leakage Current PA, PB, PC, PD, PE, PF	I_{LK}	-2	-	+2	μA	V_{DD} = 5.5V, 0 < V_{IN} < V_{DD}
Logic 1 to 0 Transition Current PA~PF (Quasi-bidirectional mode)	I_{TL} [3]	-650	-	-200	μA	V_{DD} = 5.5V, V_{IN} < 2.0V
Input Low Voltage PA, PB, PC, PD, PE, PF (TTL input)	V_{IL1}	-0.3	-	0.8	V	V_{DD} = 4.5V
		-0.3	-	0.6		V_{DD} = 2.5V
Input High Voltage PA, PB, PC, PD, PE, PF (TTL input)	V_{IH1}	2.0	-	V_{DD} +0.2	V	V_{DD} = 5.5V
		1.5	-	V_{DD} +0.2		V_{DD} = 3.0V
Input Low Voltage PA, PB, PC, PD, PE, PF (Schmitt input)	V_{IL2}	-0.5	-	0.35 V_{DD}	V	
Input High Voltage PA, PB, PC, PD, PE, PF (Schmitt input)	V_{IH2}	0.65 V_{DD}	-	V_{DD}+0.5	V	
Hysteresis voltage of PA~PE (Schmitt input)	V_{HY}		0.2 V_{DD}		V	
Input Low Voltage XT1[*2]	V_{IL3}	0	-	0.8	V	V_{DD} = 4.5V
		0	-	0.4		V_{DD} = 3.0V
Input High Voltage XT1[*2]	V_{IH3}	3.9	-	V_{DD} +0.2	V	V_{DD} = 5.5V
		2.4	-	V_{DD} +0.2		V_{DD} = 3.0V
Negative going threshold (Schmitt input), /RESET	V_{ILS}	-0.5	-	0.2 V_{DD}	V	
Positive going threshold (Schmitt input), /RESET	V_{IHS}	0.6 V_{DD}	-	V_{DD}+0.5	V	

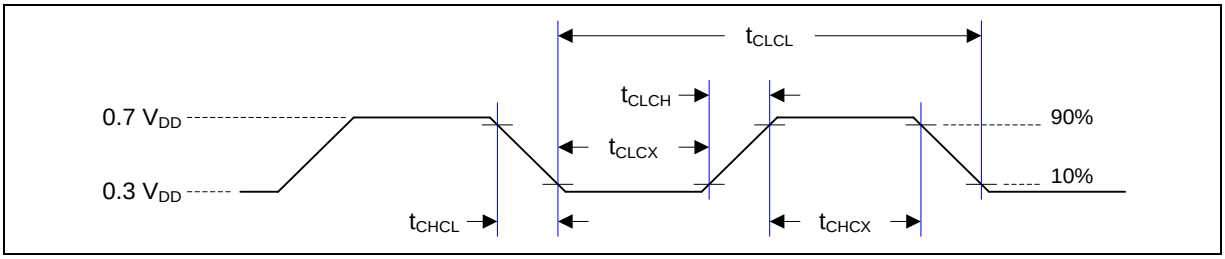
PARAMETER	SYM	SPECIFICATIONS				TEST CONDITIONS
		MIN	TYP	MAX	UNIT	
Source Current PA, PB, PC, PD, PE, PF (Quasi-bidirectional Mode)	I_{SR11}	-300	-370	-450	μA	V_{DD} = 4.5V, V_S = 2.4V
	I_{SR12}	-50	-70	-90	μA	V_{DD} = 2.7V, V_S = 2.2V
	I_{SR12}	-40	-60	-80	μA	V_{DD} = 2.5V, V_S = 2.0V
Source Current PA, PB, PC, PD, PE, PF (Push-pull Mode)	I_{SR21}	-24	-28	-32	mA	V_{DD} = 4.5V, V_S = 2.4V
	I_{SR22}	-4	-6	-8	mA	V_{DD} = 2.7V, V_S = 2.2V
	I_{SR22}	-3	-5	-7	mA	V_{DD} = 2.5V, V_S = 2.0V
Sink Current PA, PB, PC, PD, PE, PF (Quasi-bidirectional and Push-pull Mode)	I_{SK1}	10	16	20	mA	V_{DD} = 4.5V, V_S = 0.45V
	I_{SK1}	7	10	13	mA	V_{DD} = 2.7V, V_S = 0.45V
	I_{SK1}	6	9	12	mA	V_{DD} = 2.5V, V_S = 0.45V
Brown-out voltage with BOV_VL [1:0] =00b	$V_{BO2.2}$	2.1	2.2	2.3	V	
Brown-out voltage with BOV_VL [1:0] =01b	$V_{BO2.7}$	2.6	2.7	2.8	V	
Brown-out voltage with BOV_VL [1:0] =10b	$V_{BO3.8}$	3.5	3.7	3.9	V	
Brown-out voltage with BOV_VL [1:0] =11b	$V_{BO4.5}$	4.2	4.4	4.6	V	
Hysteresis range of BOD voltage	V_{BH}	30	-	150	mV	V_{DD} = 2.5V - 5.5V

Notes:

1. nRESET pin is a Schmitt trigger input.
2. Crystal Input is a CMOS input.
3. Pins of PA, PB, PC, PD and PE can source a transition current when they are being externally driven from 1 to 0. In the condition of V_{DD}=5.5 V, 5he transition current reaches its maximum value when V_{IN} approximates to 2V.

9.3 AC Electrical Characteristics

9.3.1 External 4~24 MHz High Speed Oscillator



Note: Duty cycle is 50%.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
t_{CHCX}	Clock High Time		10	-	-	ns
t_{CLCX}	Clock Low Time		10	-	-	ns
t_{CLCH}	Clock Rise Time		2	-	15	ns
t_{CHCL}	Clock Fall Time		2	-	15	ns

9.3.2 External 4~24 MHz High Speed Crystal

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Input clock frequency	External crystal	4	-	24	MHz
Temperature	-	-40	-	105	°C
V_{DD}	-	2.5	-	5.5	V

9.3.2.1 Typical Crystal Application Circuits

CRYSTAL	C1	C2	R
4 MHz ~ 24 MHz	10~20 pF	10~20 pF	without

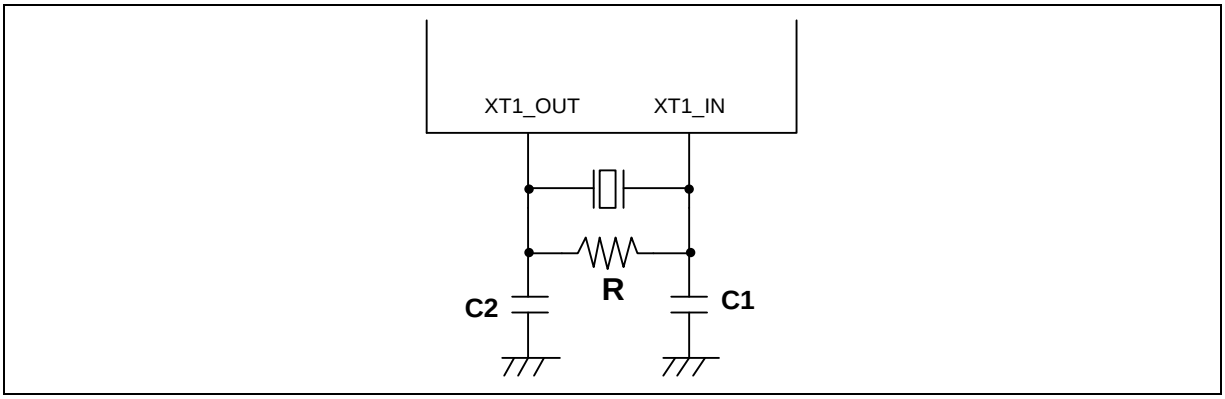


Figure 9-1 Typical Crystal Application Circuit

9.3.3 Internal 22.1184 MHz High Speed Oscillator

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Supply voltage[1]	-	2.5	-	5.5	V
Center Frequency	-	-	22.1184	-	MHz
Calibrated Internal Oscillator Frequency	+25°C; V_{DD} =5 V	-1	-	+1	%
	-40°C~+105°C; V_{DD}=2.5 V~5.5 V	-3	-	+3	%
Operation Current	V_{DD} =5 V	-	500	-	μA

9.3.4 Internal 10 kHz Low Speed Oscillator

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Supply voltage[1]	-	2.5	-	5.5	V
Center Frequency	-	-	10	-	kHz
Calibrated Internal Oscillator Frequency	+25°C; V_{DD} =5 V	-30	-	+30	%
	-40°C~+105°C; V_{DD}=2.5 V~5.5 V	-50	-	+50	%

Note: Internal operation voltage comes from LDO.

9.4 Analog Characteristics

9.4.1 10-bit SARADC Specifications

PARAMETER	Sym.	Specification				TEST CONDITIONS
		Min.	TYP.	Max.	Unit	
Operating voltage	AV_{DD}	2.7		5.5	V	$AV_{DD} = V_{DD}$
Operating current	I_{ADC}			1.5	mA	$AV_{DD} = V_{DD} = 5V$, $F_{SPS} = 200k$
Resolution	R_{ADC}			10	bit	
Reference voltage	V_{REF}		AV_{DD}		V	V_{REF} connected to AV_{DD} in chip
ADC input voltage	V_{IN}	0		AV_{DD}	V	
Sampling rate	F_{SPS}	200k			Hz	V_{DD} = 5V, ADC clock = 3 MHz Free running conversion
Integral non-linearity error (INL)	INL			±1	LSB	
Differential non-linearity (DNL)	DNL			±1	LSB	
Gain error	E_G			±2	LSB	
Offset error	E_{OFFSET}		3		LSB	
Absolute error	E_{ABS}		4		LSB	
ADC clock frequency	F_{ADC}	100k		3M	Hz	V_{DD} = 5V
Clock cycle	AD_{CYC}	16			Cycle	

9.4.2 LDO and Power Management Specifications

PARAMETER	MIN	TYP	MAX	UNIT	NOTE
Input Voltage	2.5	5	5.5	V	V_{DD} input voltage
Output Voltage	1.62	1.8	1.98	V	V_{DD} > 2.5V
Temperature	-40	25	105	°C	
Cbp	-	1	-	µF	Resr = 1Ω

Notes:

1. It is recommended that a 10µF or higher capacitor and a 100nF bypass capacitor are connected between V_{DD} and the closest V_{SS} pin of the device.

2. To ensure power stability, a 1µF (Cbp) or higher capacitor must be connected between LDO pin and the closest V_{SS} pin of the device.

9.4.3 Low Voltage Reset Specifications

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Operation voltage	-	1.7	-	5.5	V
Quiescent current	V_{DD} = 5.5 V	-	-	5	μA
Temperature	-	-40	25	105	°C
Threshold voltage	Temperature = 25°C	1.7	2.0	2.3	V
	Temperature = -40°C	-	1.8	-	V
	Temperature = 85°C	-	2.2	-	V
Hysteresis	-	0	0	0	V

9.4.4 Brown-out Detector Specifications

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Operation voltage	-	2.5	-	5.5	V
Quiescent current	AV_{DD} = 5.5 V	-	-	125	μA
Temperature	-	-40	25	105	°C
Brown-out voltage	BOV_VL[1:0] = 11	4.2	4.4	4.6	V
	BOV_VL [1:0] = 10	3.5	3.7	3.9	V
	BOV_VL [1:0] = 01	2.6	2.7	2.8	V
	BOV_VL [1:0] = 00	2.1	2.2	2.3	V
Hysteresis	-	30	-	150	mV

9.4.5 Power-On Reset (5V) Specifications

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Temperature	-	-40	25	105	°C
Reset voltage	V+	-	2	-	V
Quiescent current	Vin>reset voltage	-	1	-	nA

9.4.6 USB PHY Specifications

9.4.6.1 USB DC Electrical Characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	Input high (driven)		2.0			V
V_{IL}	Input low				0.8	V
V_{DI}	Differential input sensitivity	|PADP-PADM|	0.2			V
V_{CM}	Differential common-mode range	Includes V_{DI} range	0.8		2.5	V
V_{SE}	Single-ended receiver threshold		0.8		2.0	V
	Receiver hysteresis			200		mV
V_{OL}	Output low (driven)		0		0.3	V
V_{OH}	Output high (driven)		2.8		3.6	V
V_{CRS}	Output signal cross voltage		1.3		2.0	V
R_{PU}	Pull-up resistor		1.425		1.575	kΩ
R_{PD}	Pull-down resistor		14.25		15.75	kΩ
V_{TRM}	Termination Voltage for upstream port pull up (RPU)		3.0		3.6	V
Z_{DRV}	Driver output resistance	Steady state drive*		10		Ω
C_{IN}	Transceiver capacitance	Pin to GND			20	pF

Note: Driver output resistance doesn't include series resistor resistance.

9.4.6.2 USB Full-Speed Driver Electrical Characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
T_{FR}	Rising time	C_L = 50p	4		20	ns
T_{FF}	Falling time	C_L = 50p	4		20	ns
T_{FRFF}	Rising and falling time matching	$T_{FRFF} = T_{FR}/T_{FF}$	90		111.11	%

9.4.6.3 USB Power Dissipation

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
I_{VBUS}	VBUS current (steady state)	Standby		50		μA

9.4.6.4 USB LDO Specification

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{BUS}	VBUS Pin Input Voltage		4.0	5.0	5.5	V
V_{DD33}	LDO Output Voltage		3.0	3.3	3.6	V
C_{bp}	External Bypass Capacitor			1.0	-	μF

9.5 Flash DC Electrical Characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	Supply Voltage		1.62	1.8	1.98	V[1]
N_{ENDUR}	Endurance		20000			cycles[2]
T_{RET}	Data Retention	At 25°C	100			year
T_{ERASE}	Page Erase Time			20		ms
T_{MER}	Mass Erase Time			40		ms
T_{PROG}	Program Time			35		μs
I_{DD1}	Read Current		-	TBD		mA/MHz
I_{DD2}	Program/Erase Current				7	mA
I_{PD}	Power Down Current		-	1	20	μA

Note1: V_{DD} is source from chip LDO output voltage.

Note2: Number of program/erase cycles.

Note3: This table is guaranteed by design, not test in production.

9.6 SPI Dynamic Characteristics

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
SPI Master mode (V_{DD} = 4.5V ~ 5.5V, 30pF loading Capacitor)					
t_{DS}	Data setup time	4	2	-	ns
t_{DH}	Data hold time	0	-	-	ns
t_V	Data output valid time	-	7	11	ns
SPI Master mode (V_{DD} = 3.0V ~ 3.6V, 30pF loading Capacitor)					
t_{DS}	Data setup time	5	3	-	ns
t_{DH}	Data hold time	0	-	-	ns
t_V	Data output valid time	-	13	18	ns
SPI Slave mode (V_{DD} = 4.5V ~ 5.5V, 30pF loading Capacitor)					
t_{DS}	Data setup time	0	-	-	ns
t_{DH}	Data hold time	2*PCLK+4	-	-	ns
t_V	Data output valid time	-	2*PCLK+11	2*PCLK+19	ns
SPI Slave mode (V_{DD} = 3.0V ~ 3.6V, 30pF loading Capacitor)					
t_{DS}	Data setup time	0	-	-	ns
t_{DH}	Data hold time	2*PCLK+6	-	-	ns
t_V	Data output valid time	-	2*PCLK+19	2*PCLK+25	ns

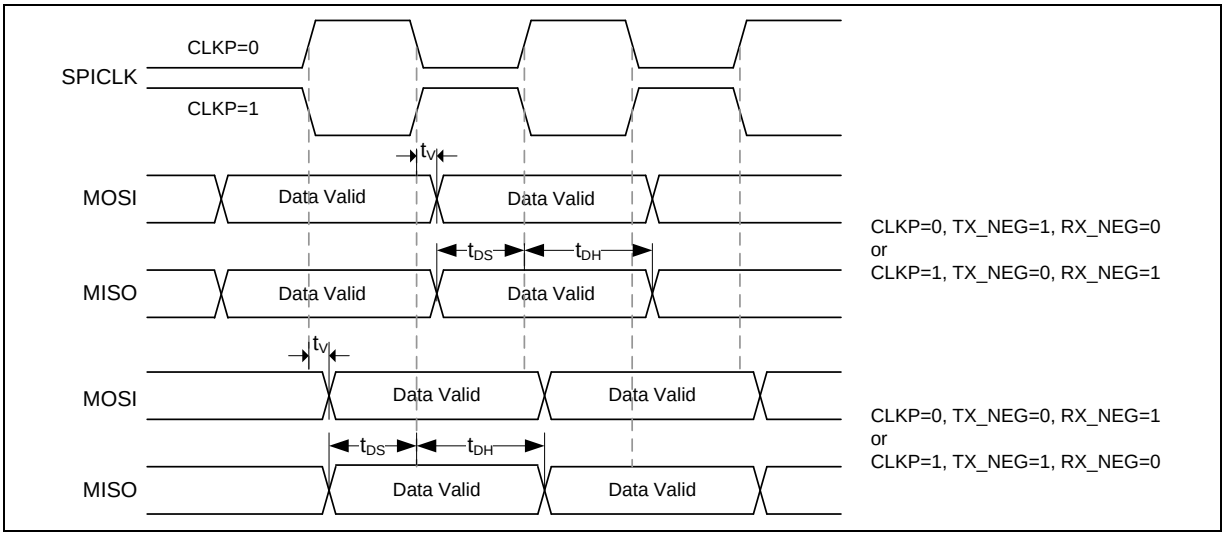


Figure 9-2 SPI Master Dynamic Characteristics timing

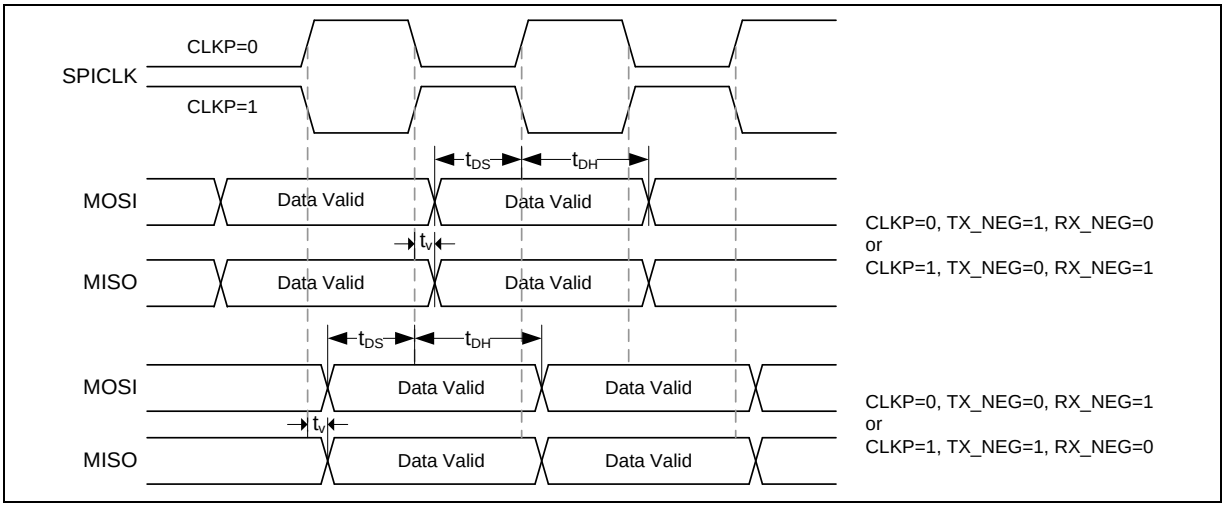
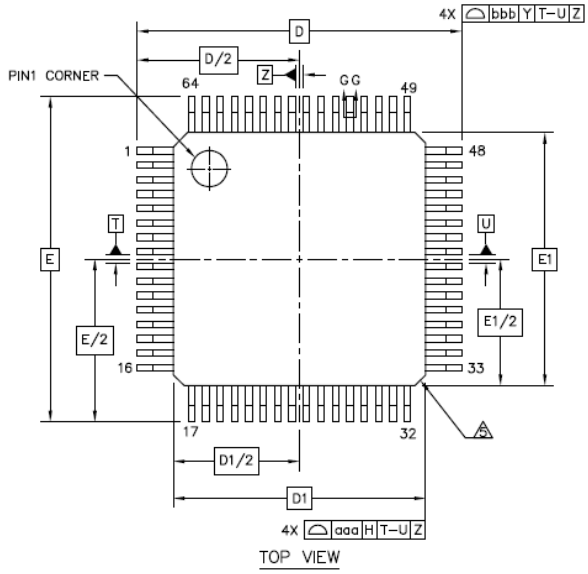


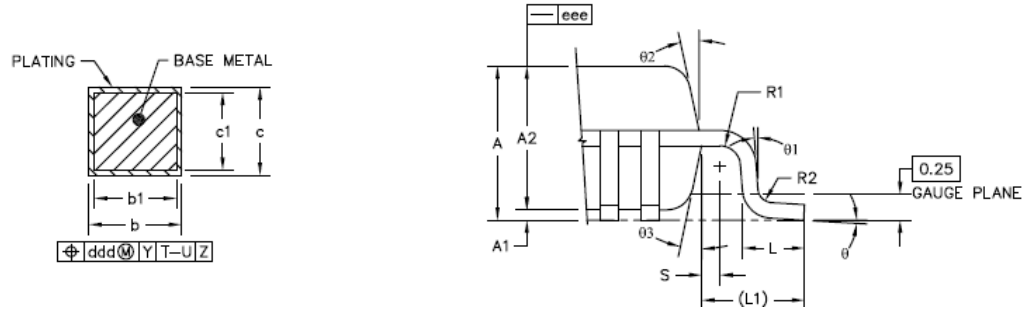
Figure 9-3 SPI Slave Dynamic Characteristics Timing

10 PACKAGE DIMENSIONS

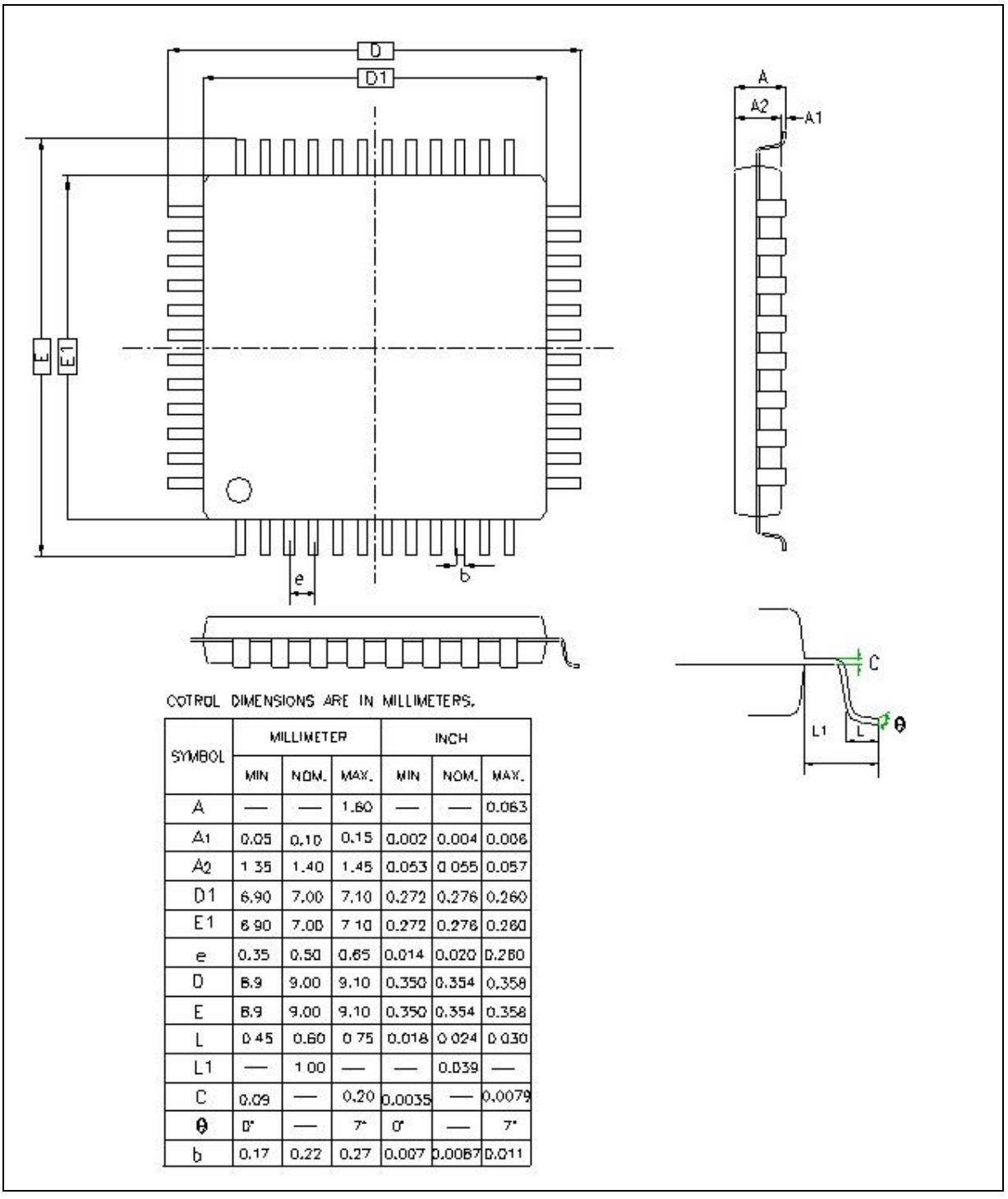
10.1 64L LQFP (7x7x1.4 mm footprint 2.0 mm)



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	---	---	1.6
STAND OFF		A1	0.05	---	0.15
MOLD THICKNESS		A2	1.35	1.4	1.45
LEAD WIDTH(PLATING)		b	0.13	0.18	0.23
LEAD WIDTH		b1	0.13	0.16	0.19
L/F THICKNESS(PLATING)		c	0.09	---	0.2
L/F THICKNESS		c1	0.09	---	0.16
BODY SIZE	X	D	9 BSC		
	Y	E	9 BSC		
	X	D1	7 BSC		
	Y	E1	7 BSC		
LEAD PITCH		e	0.4 BSC		
		L	0.45	0.6	0.75
FOOTPRINT		L1	1 REF		
		θ	0°	3.5°	7°
		θ1	0°	---	---
		θ2	11°	12°	13°
		θ3	11°	12°	13°
		R1	0.08	---	---
		R2	0.08	---	0.2
		S	0.2	---	---
PACKAGE EDGE TOLERANCE		aaa	0.2		
LEAD EDGE TOLERANCE		bbb	0.2		
COPLANARITY		ccc	0.08		
LEAD OFFSET		ddd	0.07		
MOLD FLATNESS		eee	0.05		



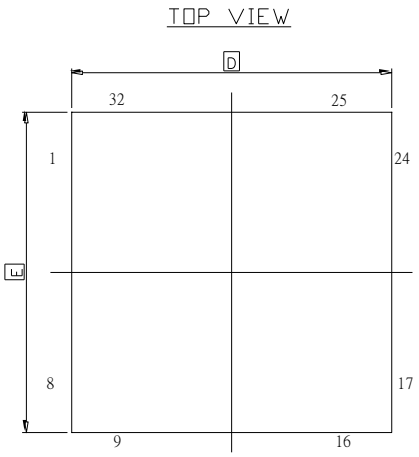
10.2 48L LQFP (7x7x1.4 mm footprint 2.0 mm)

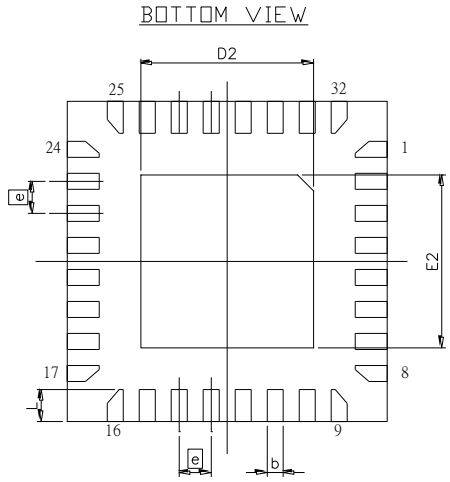


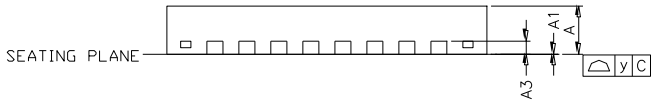
CONTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN	NOM.	MAX.	MIN	NOM.	MAX.
A	—	—	1.60	—	—	0.063
A1	0.05	0.10	0.15	0.002	0.004	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
D1	6.90	7.00	7.10	0.272	0.276	0.280
E1	6.90	7.00	7.10	0.272	0.276	0.280
e	0.35	0.50	0.65	0.014	0.020	0.280
D	8.9	9.00	9.10	0.350	0.354	0.358
E	8.9	9.00	9.10	0.350	0.354	0.358
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	—	1.00	—	—	0.039	—
C	0.09	—	0.20	0.0035	—	0.0079
θ	0°	—	7°	0°	—	7°
b	0.17	0.22	0.27	0.007	0.0087	0.011

10.3 33L QFN (5x5x0.8 mm)







SYMBOL	DIMENSION (MM)			DIMENSION (INCH)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.0275	0.0295	0.0315
A1	0	0.02	0.05	0	0.001	0.002
A3	0.20 REF			0.008 REF		
b	0.18	0.25	0.30	0.007	0.010	0.012
D	5.00 BSC			0.197 BSC		
E	5.00 BSC			0.197 BSC		
e	0.50 BSC			0.0197 BSC		
L	0.30	0.40	0.50	0.012	0.016	0.020
y	0.10			0.0039		
D2	3.20	3.40	3.60	0.124	0.138	0.142
E2	3.20	3.40	3.60	0.124	0.138	0.142

11 REVISION HISTORY

Date	Revision	Description
2012.04.01	1.00	Initial version.
2015.05.29	2.00	1. Merged NUC123xxxANx & NUC123xxxAEx into this document.
2015.11.04	2.01	1. Removed ADC function pins of NUC123 QFN33 package type in section 4.3.1.3, 4.3.2.3 and 4.4.1.
2016.01.12	2.02	1. Revised section 9.2 Source Current PA, PB, PC, PD, PE, PF (Push-pull Mode).
2016.07.06	2.03	1. Updated ADC function pins of NUC123 QFN33 package type in section 4.3.1.3, 4.3.2.3 and 4.4.1.
2017.05.03	2.04	1. Updated Typical Crystal Application Circuit for External 4~24 MHz High Speed Crystal in section 8.3.2.1.
2020.05.08	2.05	1. Added peripheral application scheme in chapter 7. 2. Added notes about the hardware reference design for ICE_DAT, ICE_CLK and nRESET pins in section 4.4 and chapter 7.

Important Notice

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