PD- 93904A

International
IOR Rectifier

SMPS MOSFET

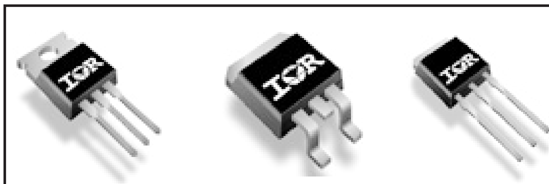
IRFB23N20D
IRFS23N20D
IRFSL23N20D

HEXFET® Power MOSFET

Applications
- High frequency DC-DC converters

V_{DSS}	$R_{DS(on)}$ max	I_D
200V	**0.10Ω**	**24A**

Benefits
- Low Gate-to-Drain Charge to Reduce Switching Losses
- Fully Characterized Capacitance Including Effective C_{OSS} to Simplify Design, (See App. Note AN1001)
- Fully Characterized Avalanche Voltage and Current



TO-220AB IRFB23N20D — D^2Pak IRFS23N20D — TO-262 IRFSL23N20D

Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V	24	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V	17	
I_{DM}	Pulsed Drain Current ①	96	
P_D @T_A = 25°C	Power Dissipation ⑦	3.8	W
P_D @T_C = 25°C	Power Dissipation	170	
	Linear Derating Factor	1.1	W/°C
V_{GS}	Gate-to-Source Voltage	± 30	V
dv/dt	Peak Diode Recovery dv/dt ③	3.3	V/ns
T_J	Operating Junction and	-55 to + 175	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting torqe, 6-32 or M3 screw⑥	10 lbf•in (1.1N•m)	

Typical SMPS Topologies

- Telecom 48V input Forward Converter

Notes ① through ⑤ are on page 11

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Static @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	200	–––	–––	V	V_{GS} = 0V, I_D = 250µA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	–––	0.26	–––	V/°C	Reference to 25°C, I_D = 1mA ⑥
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	–––	–––	0.10	Ω	V_{GS} = 10V, I_D = 14A ④
$V_{GS(th)}$	Gate Threshold Voltage	3.0	–––	5.5	V	V_{DS} = V_{GS}, I_D = 250µA
I_{DSS}	Drain-to-Source Leakage Current	–––	–––	25	µA	V_{DS} = 200V, V_{GS} = 0V
		–––	–––	250		V_{DS} = 160V, V_{GS} = 0V, T_J = 150°C
I_{GSS}	Gate-to-Source Forward Leakage	–––	–––	100	nA	V_{GS} = 30V
	Gate-to-Source Reverse Leakage	–––	–––	-100		V_{GS} = -30V

Dynamic @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
g_{fs}	Forward Transconductance	13	–––	–––	S	V_{DS} = 50V, I_D = 14A
Q_g	Total Gate Charge	–––	57	86	nC	I_D = 14A
Q_{gs}	Gate-to-Source Charge	–––	14	21		V_{DS} = 160V
Q_{gd}	Gate-to-Drain ("Miller") Charge	–––	27	40		V_{GS} = 10V, ④⑥
$t_{d(on)}$	Turn-On Delay Time	–––	14	–––	ns	V_{DD} = 100V
t_r	Rise Time	–––	32	–––		I_D = 14A
$t_{d(off)}$	Turn-Off Delay Time	–––	26	–––		R_G = 4.6Ω
t_f	Fall Time	–––	16	–––		V_{GS} = 10V ④
C_{iss}	Input Capacitance	–––	1960	–––	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	–––	300	–––		V_{DS} = 25V
C_{rss}	Reverse Transfer Capacitance	–––	65	–––		f = 1.0MHz⑥
C_{oss}	Output Capacitance	–––	2200	–––		V_{GS} = 0V, V_{DS} = 1.0V, f = 1.0MHz
C_{oss}	Output Capacitance	–––	120	–––		V_{GS} = 0V, V_{DS} = 160V, f = 1.0MHz
C_{oss} eff.	Effective Output Capacitance	–––	220	–––		V_{GS} = 0V, V_{DS} = 0V to 160V ⑤

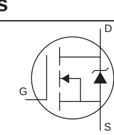
Avalanche Characteristics

	Parameter	Typ.	Max.	Units
E_{AS}	Single Pulse Avalanche Energy②⑥	–––	250	mJ
I_{AR}	Avalanche Current①	–––	14	A
E_{AR}	Repetitive Avalanche Energy①	–––	17	mJ

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	–––	0.90	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface ⑥	0.50	–––	
$R_{\theta JA}$	Junction-to-Ambient⑥	–––	62	
$R_{\theta JA}$	Junction-to-Ambient⑦	–––	40	

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	–––	–––	24	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①⑥	–––	–––	96		
V_{SD}	Diode Forward Voltage	–––	–––	1.3	V	T_J = 25°C, I_S = 14A, V_{GS} = 0V ④
t_{rr}	Reverse Recovery Time	–––	200	300	ns	T_J = 25°C, I_F = 14A
Q_{rr}	Reverse RecoveryCharge	–––	1300	1940	nC	di/dt = 100A/µs ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

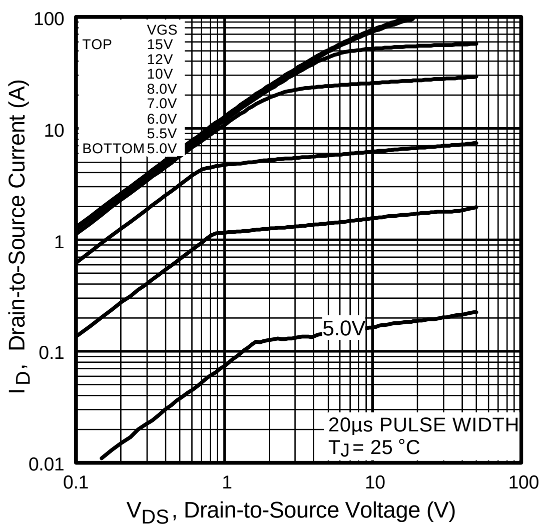


Fig 1. Typical Output Characteristics

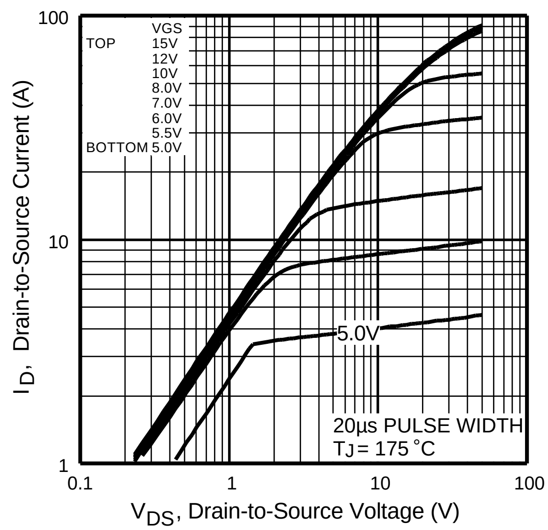


Fig 2. Typical Output Characteristics

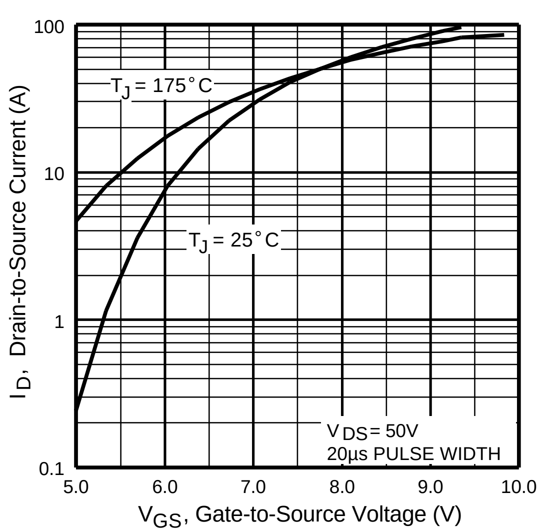


Fig 3. Typical Transfer Characteristics

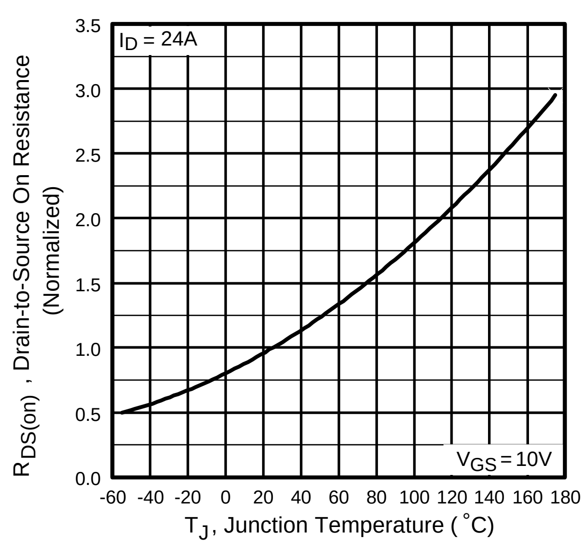


Fig 4. Normalized On-Resistance Vs. Temperature

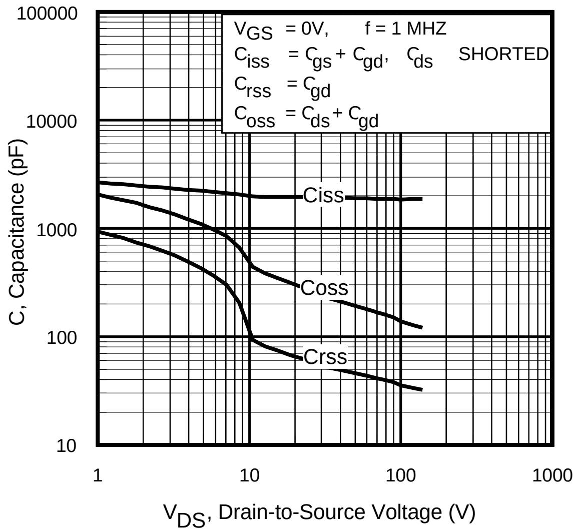


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

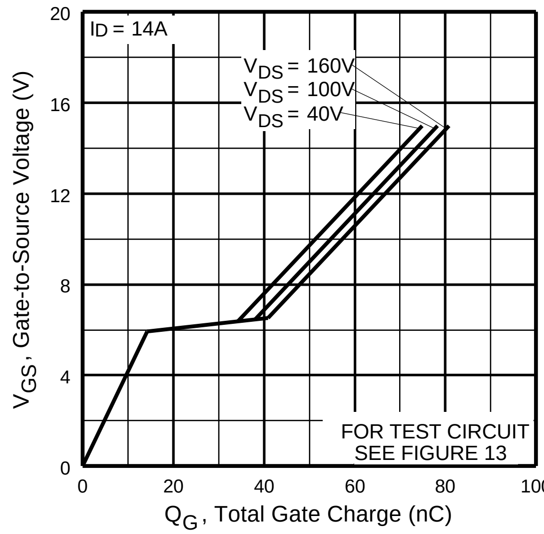


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

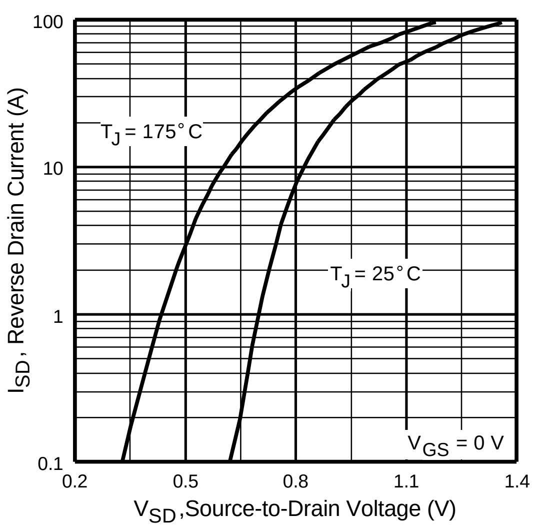


Fig 7. Typical Source-Drain Diode Forward Voltage

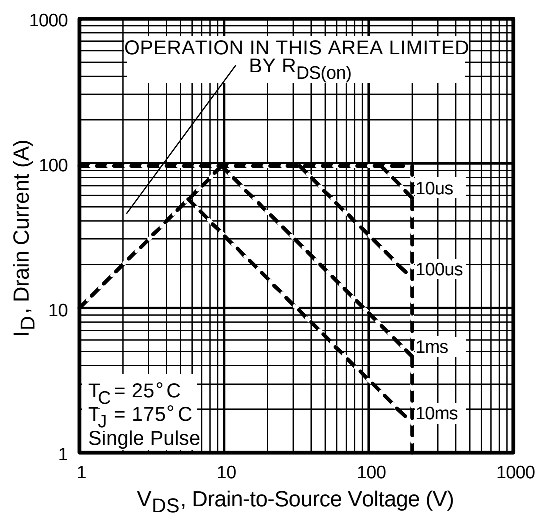


Fig 8. Maximum Safe Operating Area

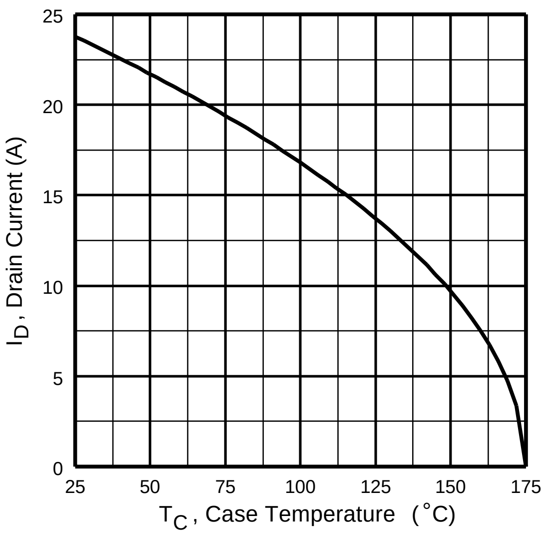


Fig 9. Maximum Drain Current Vs. Case Temperature

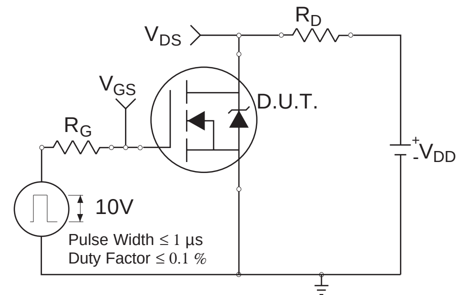


Fig 10a. Switching Time Test Circuit

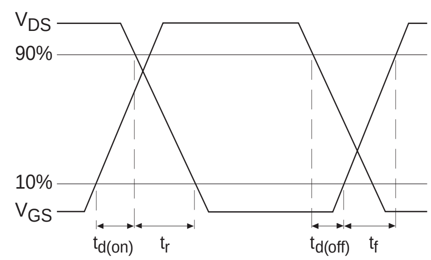


Fig 10b. Switching Time Waveforms

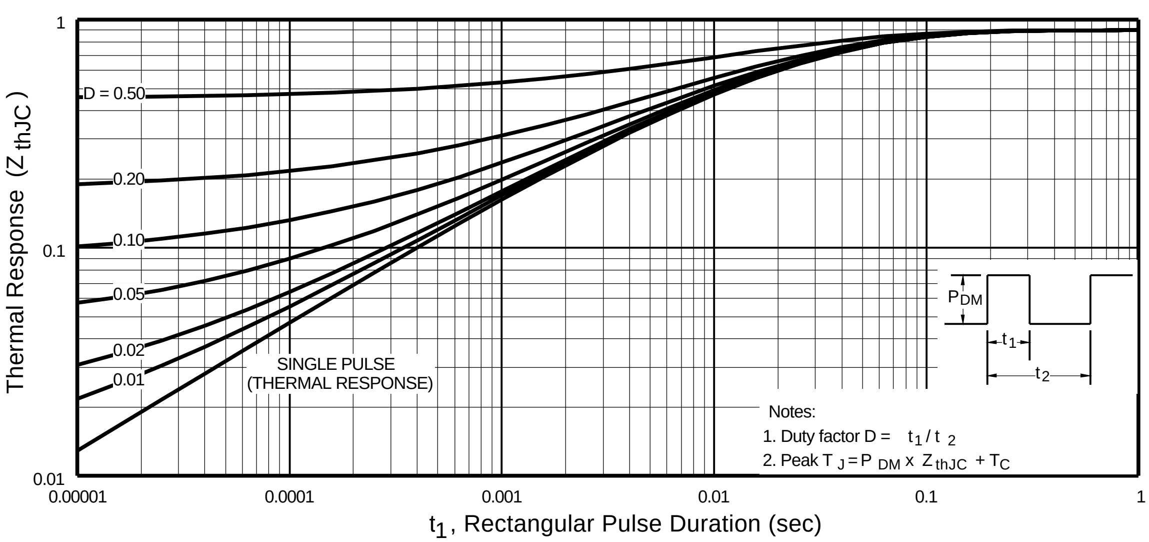


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

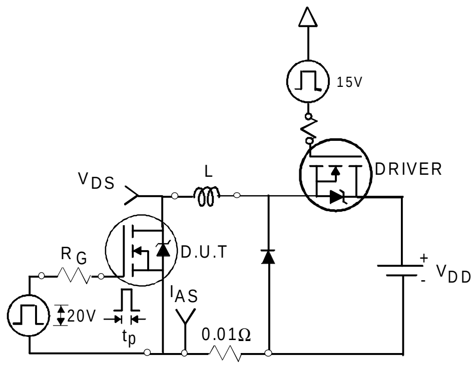


Fig 12a. Unclamped Inductive Test Circuit

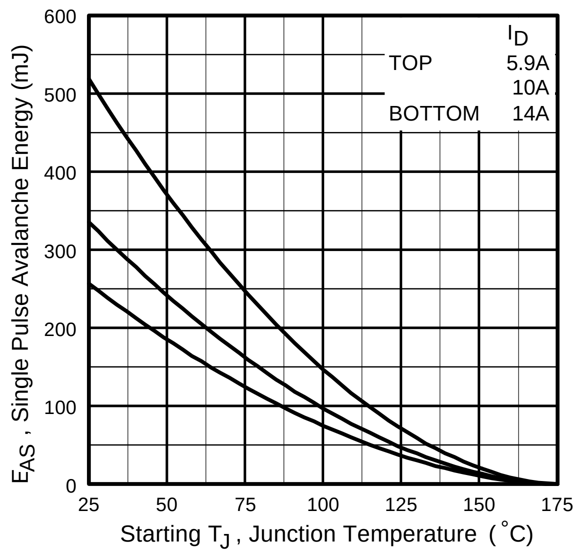


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

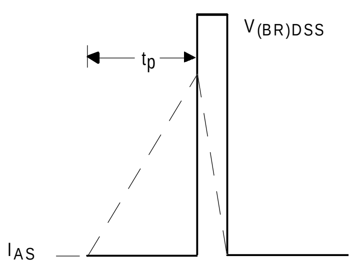


Fig 12b. Unclamped Inductive Waveforms

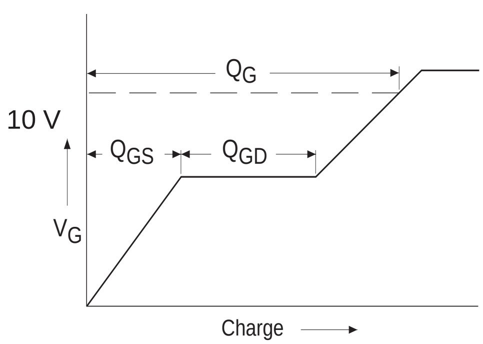


Fig 13a. Basic Gate Charge Waveform

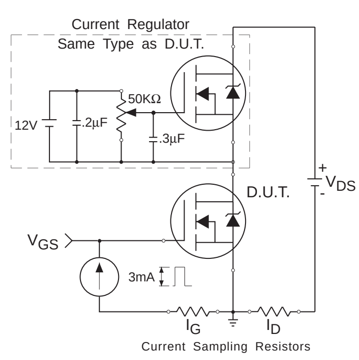
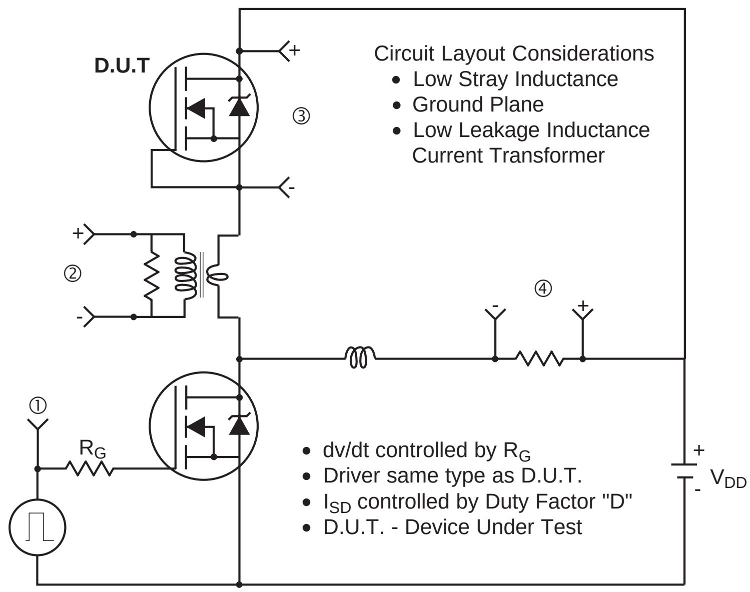
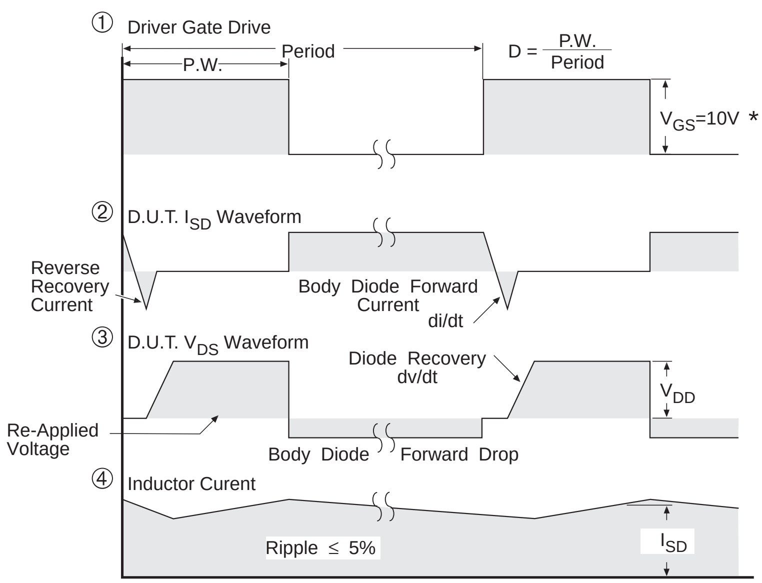


Fig 13b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit



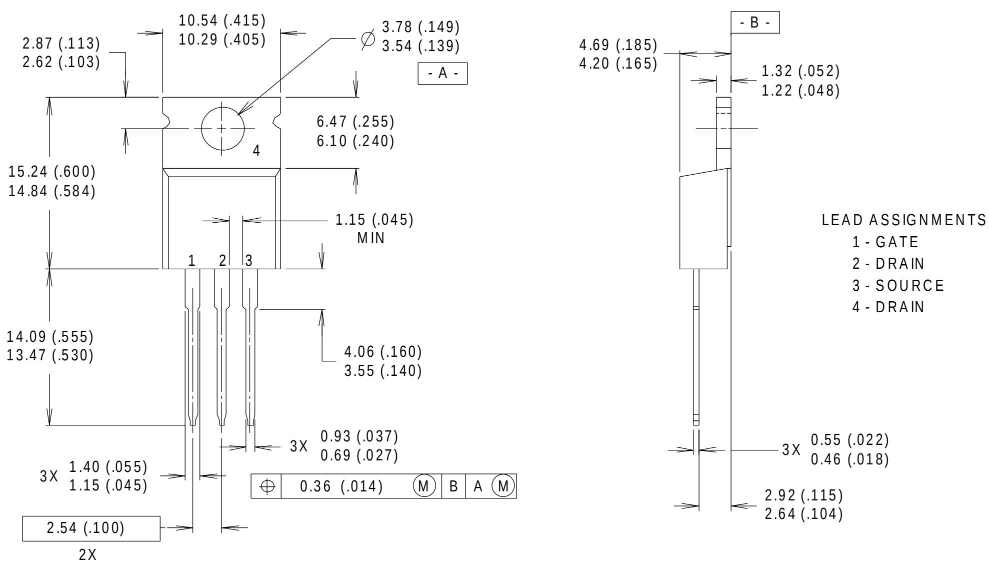


* V_{GS} = 5V for Logic Level Devices

Fig 14. For N-Channel HEXFET® Power MOSFETs

TO-220AB Package Outline

Dimensions are shown in millimeters (inches)



NOTES:

1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.

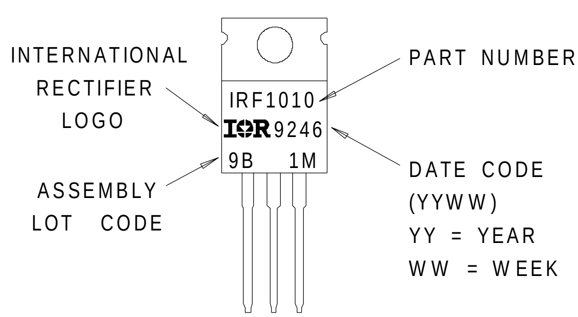
2 CONTROLLING DIMENSION : INCH

3 OUTLINE CONFORMS TO JEDEC OUTLINE TO-220AB.

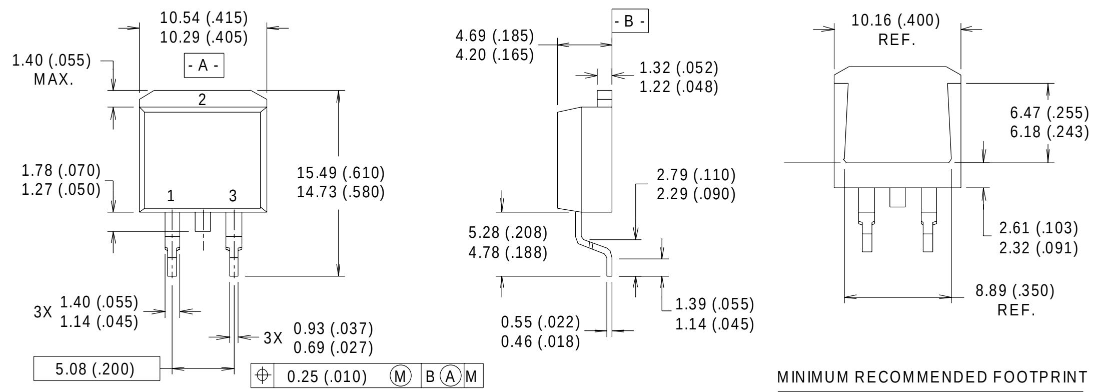
4 HEATSINK & LEAD MEASUREMENTS DO NOT INCLUDE BURRS.

TO-220AB Part Marking Information

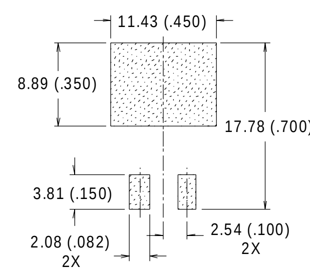
EXAMPLE : THIS IS AN IRF1010
WITH ASSEMBLY
LOT CODE 9B1M



D²Pak Package Outline



MINIMUM RECOMMENDED FOOTPRINT

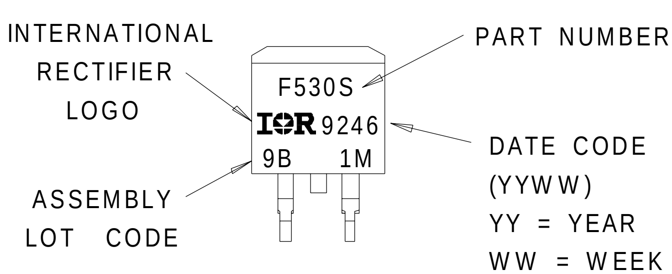


NOTES:

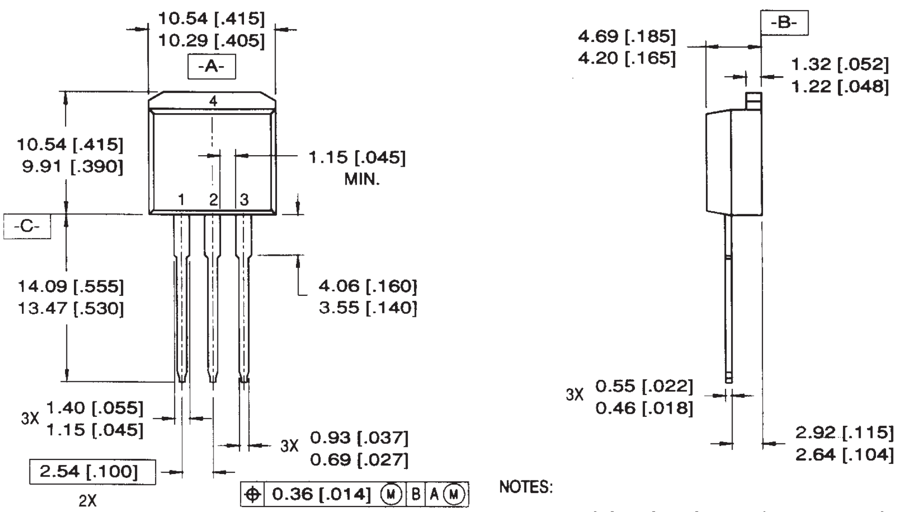
1. DIMENSIONS AFTER SOLDER DIP.
2. DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
3. CONTROLLING DIMENSION : INCH.
4. HEATSINK & LEAD DIMENSIONS DO NOT INCLUDE BURRS.

LEAD ASSIGNMENTS
1 - GATE
2 - DRAIN
3 - SOURCE

D²Pak Part Marking Information



TO-262 Package Outline



LEAD ASSIGNMENTS

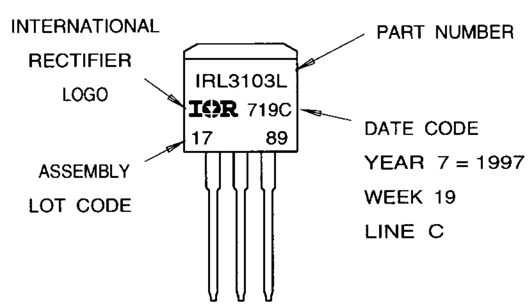
1 = GATE
2 = DRAIN
3 = SOURCE
4 = DRAIN

NOTES:

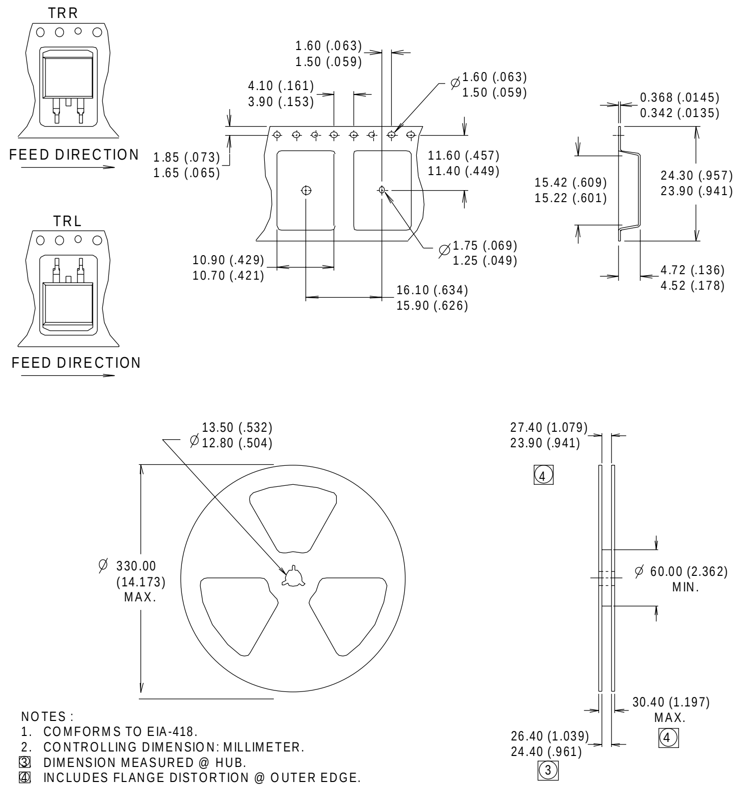
1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. HEATSINK & LEAD DIMENSIONS DO NOT INCLUDE BURRS.

TO-262 Part Marking Information

EXAMPLE: THIS IS AN IRL3103L
LOT CODE 1789
ASSEMBLED ON WW 19, 1997
IN THE ASSEMBLY LINE "C"



D^2Pak Tape & Reel Information



Notes:

① Repetitive rating; pulse width limited by max. junction temperature.

② Starting $T_J = 25°C$, $L = 2.6mH$ $R_G = 25\Omega$, $I_{AS} = 14A$.

③ $I_{SD} \leq 14A$, $di/dt \leq 130A/\mu s$, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq 175°C$

④ Pulse width ≤ 300µs; duty cycle ≤ 2%.

⑤ C_{oss} eff. is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}

⑥ This is only applied to TO-220AB package

⑦ This is applied to D^2Pak, when mounted on 1" square PCB (FR-4 or G-10 Material).
For recommended footprint and soldering techniques refer to application note #AN-994.

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IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
IR EUROPEAN REGIONAL CENTER: 439/445 Godstone Rd, Whyteleafe, Surrey CR3 OBL, UK Tel: ++ 44 (0)20 8645 8000
IR CANADA: 15 Lincoln Court, Brampton, Ontario L6T3Z2, Tel: (905) 453 2200
IR GERMANY: Saalburgstrasse 157, 61350 Bad Homburg Tel: ++ 49 (0) 6172 96590
IR ITALY: Via Liguria 49, 10071 Borgaro, Torino Tel: ++ 39 011 451 0111
IR JAPAN: K&H Bldg., 2F, 30-4 Nishi-Ikebukuro 3-Chome, Toshima-Ku, Tokyo 171 Tel: 81 (0)3 3983 0086
IR SOUTHEAST ASIA: 1 Kim Seng Promenade, Great World City West Tower, 13-11, Singapore 237994 Tel: ++ 65 (0)838 4630
IR TAIWAN:16 Fl. Suite D. 207, Sec. 2, Tun Haw South Road, Taipei, 10673 Tel: 886-(0)2 2377 9936

Data and specifications subject to change without notice. 4/00

Note: For the most current drawings please refer to the IR website at:
http://www.irf.com/package/