PRODUCT/PROCESS CHANGE NOTIFICATION

PCN IPG-IPC/14/8797
Dated 14 Nov 2014

ST7580 : METAL MASK CHANGE

Table 1. Change Implementation Schedule

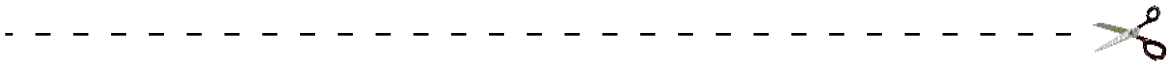
Forecasted implementation date for change	07-Nov-2014
Forecasted availability date of samples for customer	30-Nov-2014
Forecasted date for **STMicroelectronics** change Qualification Plan results availability	07-Nov-2014
Estimated date of changed product first shipment	13-Feb-2015

Table 2. Change Identification

Product Identification (Product Family/Commercial Product)	ST7580 and ST7580TR
Type of change	Product design change
Reason for change	To improve yield and device stability
Description of the change	Metal Fix (from CA to CB version)
Change Product Identification	By a new Finished Goods code
Manufacturing Location(s)	

Table 3. List of Attachments

Customer Part numbers list	
Qualification Plan results	



Customer Acknowledgement of Receipt	**PCN IPG-IPC/14/8797**
Please sign and return to STMicroelectronics Sales Office	**Dated 14 Nov 2014**

☐ Qualification Plan Denied	Name:
☐ Qualification Plan Approved	Title:
	Company:
☐ Change Denied	Date:
☐ Change Approved	Signature:

Remark

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DOCUMENT APPROVAL

Name	Function
Moscatelli, Alessandro	Marketing Manager
Arrigo, Domenico Massimo	Product Manager
Moretti, Paolo	Q.A. Manager

ATTACHMENT TO PCN IPG-IPC/14/8797

WHAT*:*
We have upgraded product line UAC3CA from CA to CB revision.
The impacted commercial products are: ST7580 and ST7580TR

WHY*:*
To improve the yield and the device stability.

HOW*:*
Through a metal mask modification.

WHEN*:*
The metal mask change has already been evaluated (see attached Reliability Report) and is effective immediately.

Samples will be available end of November.

Reliability Report

General Information	
Product Line	*UAC3*
Product Description	*Power Line Modem*
Product division	*I&PC*
Package	*VFQFPN48 7x7*
Silicon process technology	*BCD8 1v8*

Locations	
Wafer fab location	*AGRATE R2*
Assembly plant location	*CALAMBA - Phil*
Reliability assessment	*Pass*

DOCUMENT HISTORY

Version	Date	Pages	Author	Comment
1.0	5-May-14	15	P. Coerezza	Original document

Issued by

Paolo Coerezza

Reviewed by

Giuseppe Capodici

Approved by

Alceo Paratore

Table of Contents

1 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
AEC-Q100	: Stress test qualification for integrated circuits
8161393	: General Specification For Product Development

2 RELIABILITY EVALUATION OVERVIEW

2.1 Objectives

This report contains the reliability evaluation of UAC3 device diffused in AGRATE R2 and assembled in VFQFPN48 7x7 in CALAMBA.

According to Reliability Qualification Plan, below is the list of the trials performed:

Die Oriented Tests

- High Temperature Operating Life
- Temperature Humidity Bias
- Early Life Failure Rate

Package Oriented Tests

- Preconditioning
- Temperature Cycling
- Autoclave
- High Temperature Storage Life
- Temperature Humidity Bias

Electrical Characterization

- ESD resistance test
- LATCH-UP resistance test

2.2 Conclusion

Taking in account the results of the trials performed **the UAC3 diffused in AGRATE R2 and assembled in VFQFPN48 7x7 in CALAMBA can be qualified from reliability viewpoint.**

3 DEVICE CHARACTERISTICS

3.1 Device description

3.1.1 Generalities

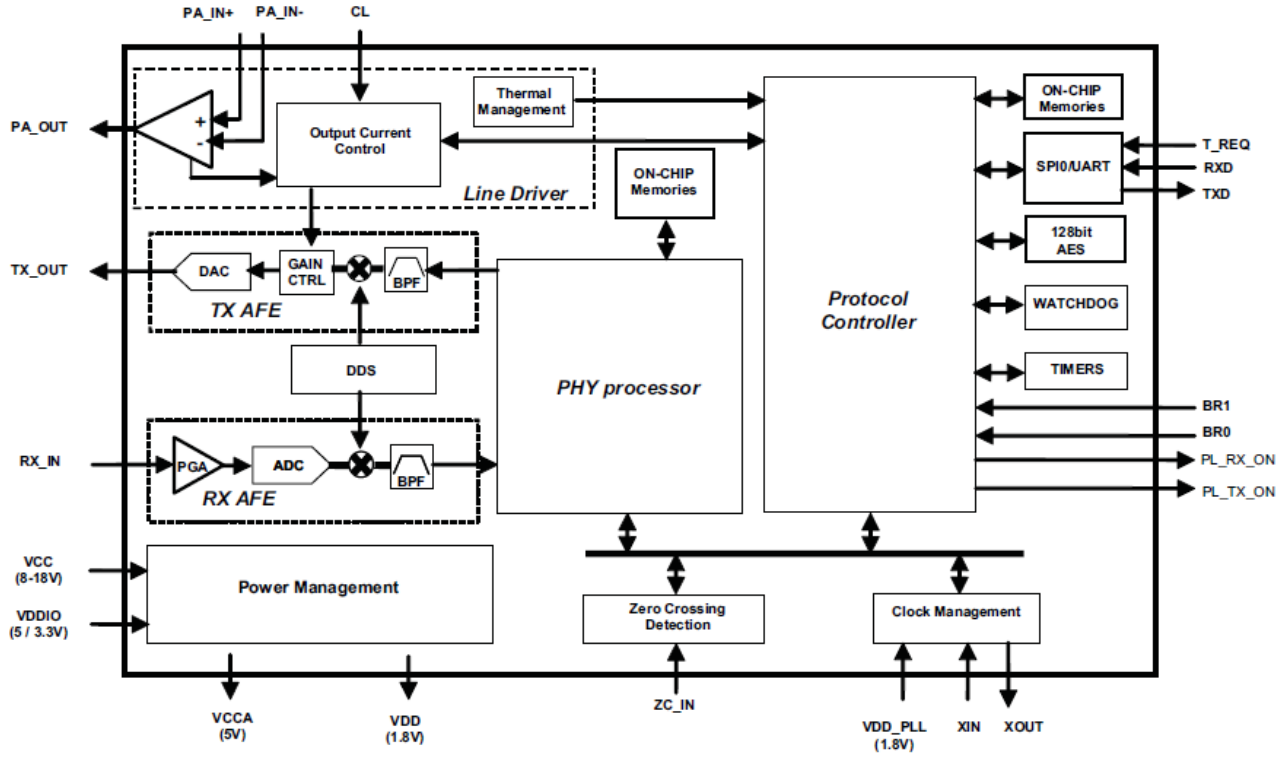
The UAC3 is a flexible power line networking system-on-chip combining a high performing PHY processor core and a protocol controller with a fully integrated analog front end (AFE) and line driver for a scalable future-proof, cost effective, single chip, narrow-band power line communication solution.

3.1.2 Pin connection

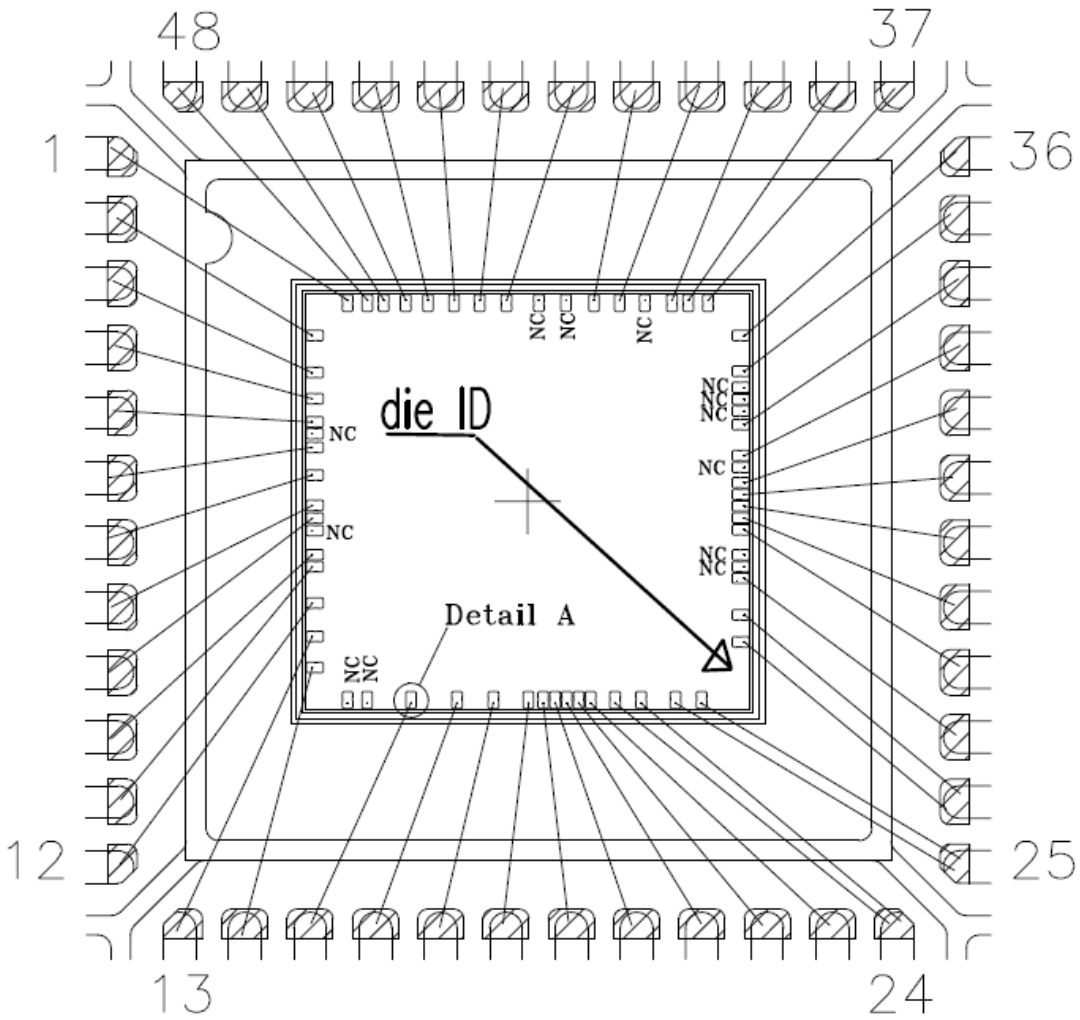
Pin	Name
1	TXD
2	RXD
3	VDDIO
4	TRSTN
5	TMS
6	GND
7	TCK
8	TDO
9	TDI
10	RESETN
11	VDD
12	XIN
13	XOUT
14	GND
15	VSSA
16	VDD_PLL
17	VCCA
18	ZC_IN
19	RX_IN
20	TX_OUT
21	PA_IN+
22	PA_IN-
23	CL
24	VCC
25	VSS
26	PA_OUT

Pin	Name
27	VDD_REG_1V8
28	VDDIO
29	NC
30	NC
31	RESERVED0
32	NC
33	GND
34	VDDIO
35	VSSA
36	CL_SEL
37	PL_RX_ON
38	T_REQ
39	BR1
40	BR0
41	PL_TX_ON
42	RESERVED1
43	RESERVED2
44	RESERVED3
45	GND
46	VDD
47	RESERVED4
48	RESERVED5
-	Exposed pad

3.1.3 Block diagram

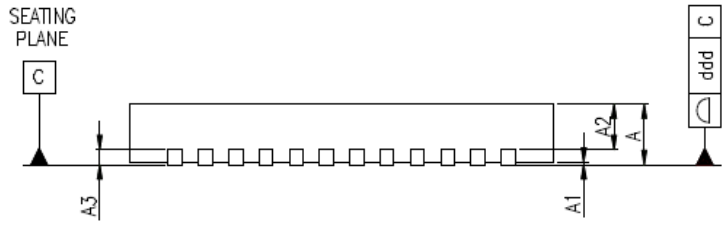


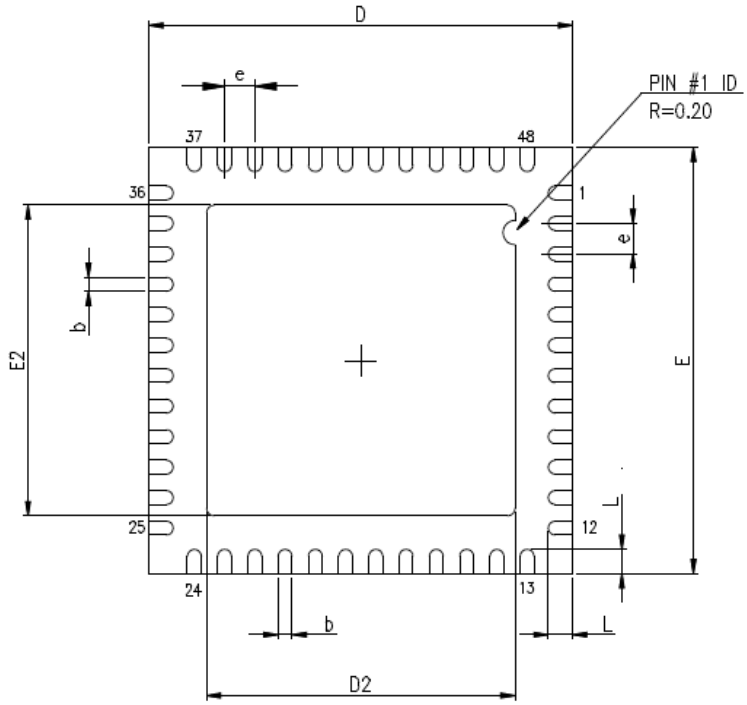
3.1.4 Bonding diagram



3.1.5 Package outline/Mechanical data

Dim.	(mm)		
	Min.	Typ.	Max.
A	0.80	0.90	1.00
A1		0.02	0.05
A2		0.65	1.00
A3		0.25	
b	0.18	0.23	0.30
D	6.85	7.00	7.15
D2	4.95	5.10	5.25
E	6.85	7.00	7.15
E2	4.95	5.10	5.25
e	0.45	0.50	0.55
L	0.30	0.40	0.50
ddd		0.08	





3.2 Traceability

Wafer fab information	
Wafer fab manufacturing location	*AGRATE R2*
Wafer diameter	*8 inches*
Wafer thickness	*280 µm*
Silicon process technology	*BCD8 1v8*
Die finishing back side	*Cr/NiV/Au*
Die size	*3539 x 3339 µm*
Bond pad metallization layers	*AlCu*
Passivation	*Polymide*
Metal levels	*4*

Assembly Information	
Assembly plant location	*CALAMBA*
Package description	*VFQFPN48 7x7*
Molding compound	*CEL9220HF13*
Wires bonding materials/diameters	*Au*
Die attach material	*Ablestik QMI 519*
Lead solder material	*NiPdAu*

4 TESTS RESULTS SUMMARY

4.1 LOTs information

Lot ID #	Silicon Rev.	Package	Assy Plant	Diff. Plant	Comments
UAC3	CBA	VFQFPN48 7x7	CALAMBA – Phil	AGRATE R2	
UAC3	CAA	TQFP64 10x10	MUAR - Malaysia	AGRATE R2	
UAB3	ABA	VFQFPN48 7x7	MUAR - Malaysia	AGRATE R2	

4.2 Test plan and results summary

Die Oriented Tests							
Test	**Method**	**Conditions**	**Failure/SS**			**Duration**	**Note**
			UAC3 CBA	UAC3 CAA	UAB3 ABA		
HTOL	High Temperature Operating Life						
	PC before	**Tj=150°C** **Vcc=18V, DVdd=5.5V, *Iout=1A rms, 3A Peak*** ***BIST+SCAN+Functionals tests***	**0/77** (1)	-	**0/40** (2)	(1) 500h (2) 1000h	
ELFR	Early Life Failure Rate						
		Tj=150°C **Vcc=18V, DVdd=5.5V, *Iout=1A rms, 3A Peak*** ***BIST+SCAN+Functional tests***	**-**	-	**0/2400** (3)	**24H**	**(3) BAA rev.**

Package Oriented Tests							
Test	**Method**	**Conditions**	**Failure/SS**			**Duration**	**Note**
			UAC3 CBA	UAC3 CAA	UAB3 ABA		
PC	Pre-Conditioning: Moisture sensitivity level 3						
		192h 30°C/60% - 3 reflow PBT 260°C	**0/77**	**0/154**	**0/100**	**-**	
THB	Temperature Humidity Bias						
	PC before	**Ta=85°C/85%RH** **Vcc=20V, Vdd=2V, DVdd=5.5V**	**-**	**-**	**0/40**	**1000h**	
AC	Autoclave						
	PC before	**121°C 2atm**	**-**	**0/77**	**0/40 + 0/77 (3)**	**168h**	**(3) BAA rev**
TC	Temperature Cycling						
	PC before	**Temp. range:** 1000 cycles @ -50/+150 °C	**-**	**0/77**	**-**		
		500 cycles @ -65/+150 °C		**-**	**0/40 + 0/77(3)**		**(3) BAA rev.**
HTSL	High Temperature Storage						
	No bias	**Tamb=150°C**	**-**	**0/77**	**0/40**	**1000h**	

Electrical Characterization Tests							
Test	**Method**	**Conditions**	**Failure/SS**			**Duration**	**Note**
			UAC3 CBA	UAC3 CAA	UAB3 ABA		
ESD	Electro Static Discharge						
	Human Body Model	**+/- 2kV**	**-**	-	**0/3**		
	Machine Model	**+/- 200V**	**-**	-	**0/3**		
	Charge Device Model	**+/- 500V; +/- 750V on corner pins**	**-**	**0/3**	**-**		
		+/- 1.5kV	**-**	**-**	**0/3**		
LU	Latch-Up						
	Over-voltage and Current Injection	**Tamb=85°C** **Jedec78 – Level B**	**-**	-	**0/3**	**-**	

Note:
The UAC3 device is a metal option of the UAB3 device and all positive reliability results obtained on UAB3 can be extended by similarity to the UAC3 device.

5 TESTS DESCRIPTION & DETAILED RESULTS

5.1 Die oriented tests

5.1.1 High Temperature Operating Life

This test is performed like application conditions in order to check electromigration phenomena, gate oxide weakness and other design/manufacturing defects put in evidence by internal power dissipation.

The flow chart is the following:

- Initial testing @ Ta=25°C
- Check at 168 and 500hrs @ Ta=25°C
- Final Testing (1000hrs) @ Ta=25°C

5.1.2 Early Life Failure Rate

This test is to evaluate the defects inducing failure in early life.
The device is stressed in biased conditions at the max junction temperature.

The flow chart is the following:

- Initial testing @ Ta=25°C,
- Final Testing (24 hr.) @ Ta=25°C

5.2 Package oriented tests

5.2.1 Pre-Conditioning

The device is submitted to a typical temperature profile used for surface mounting, after a controlled moisture absorption.
The scope is to verify that the surface mounting stress does not impact on the subsequent reliability performance. The typical failure modes are "popcorn" effect and delamination.

5.2.2 High Temperature Storage

The device is stored in unbiased condition at the max. temperature allowed by the package materials, sometimes higher than the max. operative temperature.
The scope is to investigate the failure mechanisms activated by high temperature, typically wire-bonds solder joint ageing, data retention faults, metal stress-voiding.

5.2.3 Thermal Cycles

The purpose of this test is to evaluate the thermo mechanical behavior under moderate thermal gradient stress.
Test flow chart is the following:

- Initial testing @ Ta=25°C
- Readout @ 500 cycles
- Final Testing @ 1000 cycles @ Ta=25°C

TEST CONDITIONS:

- Ta= -50°C to +150°C(air)
- 15 min. at temperature extremes
- 1 min. transfer time

5.2.4 Autoclave

The purpose of this test is to point out critical water entry path with consequent corrosion phenomena related to chemical contamination and package hermeticity.
Test flow chart is the following:

- Initial testing @ Ta=25°C
- Final Testing (168hrs) @ Ta=25°C

TEST CONDITIONS:

- P=2.08 atm
- Ta=121°C
- test time= 168hrs

5.2.5 Temperature Humidity Bias

The test is addressed to put in evidence problems of the die-package compatibility related to phenomena activated in wet conditions such as electro-chemical corrosion.
The device is stressed in static configuration approaching some field status like power down. Temperature, Humidity and Bias are applied to the device in the following environmental conditions => Ta=85°C / RH=85%.
Input pins to Low / High Voltage (alternate) to maximize voltage contrast.
Test Duration 1000 h.

The flow chart is the following:

- Initial testing @ Ta=25°C
- Check @ 168 and 500hrs
- Final Testing (1000hrs) @ Ta=25°C

5.3 Electrical Characterization Tests

5.3.1 Latch-up

This test is intended to verify the presence of bulk parasitic effects inducing latch-up.
The device is submitted to a direct current forced/sinked into the input/output pins. Removing the direct current no change in the supply current must be observed.

Stress applied:

condition	NEG. INJECTION	POS. INJECTION	OVERVOLTAGE
IN low: 0V	-100mA	Inom+100mA	Vdd,Vdd_pll,Vdd_reg1v8=3V DVdd,Vcca,DVdd_flash=7.5V Vdd_12=18V Vcc=27V
IN high: 9.9V	-100mA	Inom+100mA	Vdd,Vdd_pll,Vdd_reg1v8=3V DVdd,Vcca,DVdd_flash=7.5V Vdd_12=18V Vcc=27V

Setup Configuration:
Pin RESETN tied LOW and tested only during LOW conditions

5.3.2 E.S.D.

This test is performed to verify adequate pin protection to electrostatic discharges.
The flow chart is the following:

- Initial testing @ Ta=25°C
- ESD discharging @ Ta=25°C
- Final Testing @ Ta=25°C

TEST CONDITIONS:

- **Human Body Model** — ANSI/ESDA/JEDEC STANDARD JES001
CDF-AEC-Q100-002
- **Machine Model** — JEDEC STANDARD EIA/JESD-A115
CDF-AEC-Q100-003
- **Charge Device Model** — ANSI/ESD STM 5.3.1 ESDA – JEDEC JESD22-C101
CDF-AEC-Q100-011

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