PCN Number:	20171204001	PCN Date:	December 06, 2017
Title:	Datasheet for TUSB544 ☐		
Customer Contact:	PCN Manager	Dept:	Quality Services

Change Type:					
☐	Assembly Site	☐	Design	☐	Wafer Bump Site
☐	Assembly Process	☒	Data Sheet	☐	Wafer Bump Material
☐	Assembly Materials	☐	Part number change	☐	Wafer Bump Process
☐	Mechanical Specification	☐	Test Site	☐	Wafer Fab Site
☐	Packing/Shipping/Labeling	☐	Test Process	☐	Wafer Fab Materials
				☐	Wafer Fab Process

Notification Details

Description of Change:

Texas Instruments Incorporated is announcing an information only notification.
The product datasheet(s) is being updated as summarized below.
The following change history provides further details.

TEXAS INSTRUMENTS

TUSB544

SLLSEZ0D – APRIL 2017 – REVISED OCTOBER 2017

Changes from Revision C (October 2017) to Revision D **Page**

- Changed text of the second paragraph in the *DESCRIPTION* From: "..cable and board trace loss due to inter symbol interference (ISI)" To: "..inter symbol interference (ISI) due to cable and board trace loss." 1
- Changed Pin 2 and Pin 35 text From: "When I2C_EN !=0,.." To: "In I2C mode,.." in the *Pin Functions* 4
- Changed Pin 14 text From: "..levels for the GPIO configuration.." To: "..levels for the 2-level GPIO configuration.." in the *Pin Functions* 5
- Changed Pin 17 in the text From: 0 = GPIO Mode (I^2C disabled) To: 0 = GPIO Mode AUX Snoop enabled (I^2C disabled) in the *Pin Functions* 5
- Changed Pins 21, 22, and 23 From: "When I2C_EN !=0,.." To: "In GPIO mode,.." in the *Pin Functions* 5
- Removed "When I2C_EN = 0" from pin 32. 5
- In pin 32, changed 2ms to $t_{CTL1\_DEBOUNCE}$ 5
- From: DEQ1 sets the high-frequency equalizer gain for downstream facing URX1, URX2, UTX1, UTX2 receivers. To: DEQ1 sets the high-frequency equalizer gain for downstream facing DRX1, DRX2, DTX1, DTX2 receivers 6
- Deleted the MAX value of 10 ms from $t_{CTL1\_DEBOUNCE}$ in the *Switching Characteristics* 10
- Added test Condition " DP lanes will be disabled if low for greater than min value" for $t_{CTL1\_DEBOUNCE}$ in the *Switching Characteristics* 10
- Changed text From: "There is an internal 30 kΩ pull-up and a 94kΩ pull-down." To: "There are internal pull-up and a pull-down resisters." in *4-Level Inputs* 18
- Changed text From: "..when I2C_EN = "0"." To: "..when I2C_EN = "0" or "F"." in the first paragraph of *Device Configuration in GPIO Mode* 19
- Changed Table 4 21
- Changed text From: "..when I2C_EN is not equal to "0"." To: "..when I2C_EN is equal to "1". " in *Device Configuration in I2C Mode* 28
- Changed text From: "When I2C_EN is '0',.." To: :In I2C mode,.." in *DisplayPort Mode* 29
- Changed text From: "When I2C_EN is '0',.." To: :In GPIO mode,.." in *Custom Alternate Mode* 29
- Deleted the *Cable Mode* section and all "cable mode" from datasheet. 29

- Changed Table 12 35
- Changed Bit 5-2 Type From: R/WU To: R/W in Table 15 36
- Changed Bit 7-0 Type From: R/WU To: R/W in Figure 25 and Table 16 37
- Changed Bit 7-0 Type From: R/WU To: R/W in Figure 26 and Table 17 37
- Changed Bit 6-0 Type From: RU To: RH in Figure 27 and Table 18 38
- Changed Figure 29 and Table 20 40
- Changed Bit 7-0 Type From: R/WU To: R/W in Figure 30 and Table 21 40
- Changed Bit 3-0 Type From: R/WU To: R/W in Figure 31 and Table 22 41
- Changed bit 7 From: R/WU To: RH in Figure 32 and Table 23 41
- USB3.1_# register default changed to 4h from 0h. 41
- Changed USB3.1_4 register default to 23h from 00h. 42
- Changed SBU1, and SBU2 pin labels on the Sink side of Figure 40 48
- Changed SBU1, and SBU2 pin labels on the Sink side of Figure 41 49
- Changed SBU1, and SBU2 pin labels on the Sink side of Figure 42 49
- Changed SBU1, and SBU2 pin labels on the Sink side of Figure 48 52
- Changed SBU1, and SBU2 pin labels on the Sink side of Figure 49 53
- Changed SBU1, and SBU2 pin labels on the Sink side of Figure 50 53

The datasheet number will be changing.

Device Family	Change From:	Change To:
TUSB544□□	SLLSEZ0C	SLLSEZ0D

These changes may be reviewed at the datasheet links provided.

http://www.ti.com/product/TUSB544

Reason for Change:

To accurately reflect device characteristics.

Anticipated impact on Fit, Form, Function, Quality or Reliability (positive / negative):

No anticipated impact. This is a specification change announcement only. There are no changes to the actual device.

Changes to product identification resulting from this PCN:

None.

Product Affected:

TUSB544IRNQR	TUSB544IRNQT	TUSB544RNQR	TUSB544RNQT

For questions regarding this notice, e-mails can be sent to the regional contacts shown below or your local Field Sales Representative.

Location	E-Mail
USA	PCNAmericasContact@list.ti.com
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