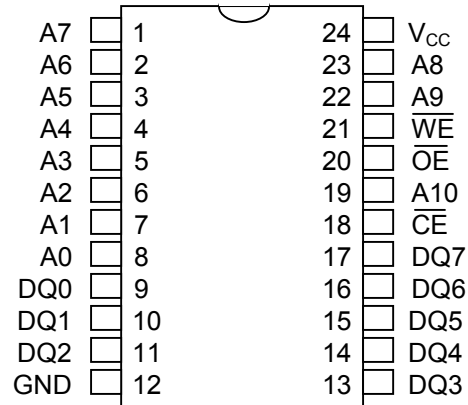


### FEATURES

- Low-power CMOS design
- Standby current
  - 50nA max at  $t_A = +25^\circ\text{C}$   $V_{CC} = 3.0\text{V}$
  - 100nA max at  $t_A = +25^\circ\text{C}$   $V_{CC} = 5.5\text{V}$
  - 1 $\mu\text{A}$  max at  $t_A = +60^\circ\text{C}$   $V_{CC} = 5.5\text{V}$
- Full operation for  $V_{CC} = 5.5\text{V}$  to 2.7V
- Data retention voltage = 5.5V to 2.0V
- Fast 5V access time
  - DS2016-100      100ns
- Reduced-speed 3V access time
  - DS2016-100      250ns
- Operating temperature range of  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$
- Full static operation
- TTL compatible inputs and outputs over voltage range of 5.5V to 2.7V
- Available in 24-pin DIP and 24-pin SO packages
- Suitable for both battery operated and battery backup applications

### PIN ASSIGNMENT



DS2016 24-Pin DIP (600mil)  
DS2016R 24-Pin SO (300mil)

### PIN DESCRIPTION

- A0 to A10      - Address Inputs
- DQ0 to DQ7    - Data Input/Output
- $\overline{\text{CE}}$             - Chip Enable Input
- $\overline{\text{WE}}$             - Write Enable Input
- $\overline{\text{OE}}$             - Output Enable Input
- V<sub>CC</sub>             - Power Supply Input 2.7V - 5.5V
- GND             - Ground

### DESCRIPTION

The DS2016 2k x 8 3V/5V Operation Static RAM is a 16,384-bit, low-power, fully static random access memory organized as 2048 words by 8 bits using CMOS technology. The device operates from a single power supply with a voltage input between 2.7V and 5.5V. The chip enable input ( $\overline{\text{CE}}$ ) is used for device selection and can be used in order to achieve the minimum standby current mode, which facilitates both battery operated and battery backup applications. The device provides access times as fast as 100ns when operated from a 5V power supply input and also provides relatively good performance of 250ns access while operating from a 3V input. The device maintains TTL-level inputs and outputs over the input voltage range of 2.7V to 5.5V. The DS2016 is most suitable for low-power applications where battery operation or battery backup for nonvolatility is required. The DS2016 is a JEDEC-standard 2k x 8 SRAM and is pin-compatible with ROM and EPROM of similar density.

**OPERATION MODE**

MODE	$\overline{\text{CE}}$	$\overline{\text{OE}}$	$\overline{\text{WE}}$	A0-A10	DQ-DQ7	POWER
READ	L	L	H	STABLE	DATA OUT	$I_{\text{CCO}}$
WRITE	L	X	L	STABLE	DATA IN	$I_{\text{CCO}}$
DESELECT	L	H	H	X	HIGH-Z	$I_{\text{CCO}}$
STANDBY	H	X	X	X	HIGH-Z	$I_{\text{CCS}}$

**ABSOLUTE MAXIMUM RATINGS**

SYMBOL	PARAMETER	RATING
$V_{\text{CC}}$	Power Supply Voltage	-0.3V to +7.0V
$V_{\text{IN}}, V_{\text{IO}}$	Input, Input/Output Voltage	-0.3 to $V_{\text{CC}} + 0.3\text{V}$
$T_{\text{STG}}$	Storage Temperature	-55°C to +125°C
$T_{\text{OPR}}$	Operating Temperature	-40°C to +85°C
$T_{\text{SOLDER}}$	Soldering Temperature/Time	IPC/JEDEC J-STD-020

**CAPACITANCE**

+25°C)

 $(T_{\text{A}} =$ 

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	$C_{\text{IN}}$		5	10	pF	
Input/Output Capacitance	$C_{\text{IO}}$		5	12	pF	

**+5-VOLT OPERATION****RECOMMENDED DC OPERATING CONDITIONS** $(T_{\text{A}} = -40^{\circ}\text{C to } +85^{\circ}\text{C})$ 

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Power Supply Voltage	$V_{\text{CC}}$	4.5	5.0	5.5	V	
Input High Voltage	$V_{\text{IH}}$	2.0		$V_{\text{CC}} + 0.3$	V	
Input Low Voltage	$V_{\text{IL}}$	-0.3		0.8	V	
Data Retention Voltage	$V_{\text{DR}}$	2.0		5.5	V	

**DC CHARACTERISTICS** $(T_{\text{A}} = -40^{\circ}\text{C to } +85^{\circ}\text{C}; V_{\text{CC}} = 5\text{V} \pm 10\%)$ 

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Leakage Current	$I_{\text{IL}}$	$0\text{V} \leq V_{\text{IN}} \leq V_{\text{CC}}$			$\pm 0.1$	$\mu\text{A}$
I/O Leakage Current	$I_{\text{LO}}$	$\overline{\text{CE}} = V_{\text{IH}}, 0\text{V} \leq V_{\text{IO}} \leq V_{\text{CC}}$			$\pm 0.5$	$\mu\text{A}$
Output High Current	$I_{\text{OH}}$	$V_{\text{OH}} = 2.4\text{V}$	-1.0			mA
Output Low Current	$I_{\text{OL}}$	$V_{\text{OL}} = 0.4\text{V}$	4.0			mA
Standby Current	$I_{\text{CCS1}}$	$\overline{\text{CE}} = 2.0\text{V}$			0.3	mA
Standby Current	$I_{\text{CCS2}}$	$\overline{\text{CE}} \geq V_{\text{CC}} - 0.5\text{V}, t_{\text{A}} = +60^{\circ}\text{C}$			1	$\mu\text{A}$
Standby Current	$I_{\text{CCS2}}$	$\overline{\text{CE}} \geq V_{\text{CC}} - 0.5\text{V}, t_{\text{A}} = +25^{\circ}\text{C}$			100	nA
Operating Current	$I_{\text{CCO}}$	$\overline{\text{CE}} = 0.8\text{V}, 200\text{ns cycle}$			55	mA

**AC CHARACTERISTICS READ CYCLE** ( $T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ;  $V_{CC} = 5\text{V} \pm 10\%$ )

PARAMETER	SYMBOL	DS2016-100			UNITS	NOTES
		MIN	TYP	MAX		
Read Cycle Time	$t_{RC}$	100			ns	
Access Time	$t_{ACC}$			100	ns	
$\overline{OE}$ to Output Valid	$t_{OE}$			50	ns	
$\overline{CE}$ to Output Valid	$t_{CO}$			100	ns	
$\overline{CE}$ or $\overline{OE}$ to Output Active	$t_{COE}$	5			ns	
Output High-Z from Deselection	$t_{OD}$	5		35	ns	
Output Hold from Address Change	$t_{OH}$	5			ns	

**AC CHARACTERISTICS WRITE CYCLE** ( $T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ;  $V_{CC} = 5\text{V} \pm 10\%$ )

PARAMETER	SYMBOL	DS2016-100			UNITS	NOTES
		MIN	TYP	MAX		
Write Cycle Time	$t_{WC}$	100			ns	
Write Pulse Width	$t_{WP}$	75			ns	
Address Setup Time	$t_{AW}$	0			ns	
Write Recovery Time	$t_{WR}$	10			ns	
Output High-Z from $\overline{WE}$	$t_{ODW}$			35	ns	
Output Active from $\overline{WE}$	$t_{OEWE}$	5			ns	
Data Setup Time	$t_{DS}$	40			ns	
Data Hold Time	$t_{DH}$	0			ns	

**DATA RETENTION CHARACTERISTICS** ( $T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ )

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Data Retention Supply Voltage	$V_{DR}$	$\overline{CE} \geq V_{CC} - 0.5\text{V}$	2.0		5.5	V
Data Retention Current at 5.5V	$I_{CCR1}$	$\overline{CE} \geq V_{CC} - 0.5\text{V}$		0.1*	1	$\mu\text{A}$
Data Retention Current at 2.0V	$I_{CCR2}$	$\overline{CE} \geq V_{CC} - 0.5\text{V}$		50*	750	nA
Chip Deselect to Data Retention	$t_{CDR}$		0			$\mu\text{s}$
Recovery Time	$t_R$		2			ms

\* Typical values are at  $+25^{\circ}\text{C}$

**+3-VOLT OPERATION****RECOMMENDED DC OPERATING CONDITIONS** ( $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ )

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Power Supply Voltage	$V_{CC}$	2.7	3.0	3.5	V	
Input High Voltage	$V_{IH}$	2.0		$V_{CC} + 0.3$	V	
Input Low Voltage	$V_{IL}$	-0.3		0.6	V	
Data Retention Voltage	$V_{DR}$	2.0		3.5	V	

**DC CHARACTERISTICS** ( $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ ;  $V_{CC} = 2.7\text{V}$  to  $3.5\text{V}$ )

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Leakage Current	$I_{IL}$	$0\text{V} \leq V_{IN} \leq V_{CC}$			$\pm 0.1$	$\mu\text{A}$
I/O Leakage Current	$I_{LO}$	$\overline{CE} = V_{IH}, 0\text{V} \leq V_{IO} \leq V_{CC}$			$\pm 0.5$	$\mu\text{A}$
Output High Current	$I_{OH}$	$V_{OH} = 2.2\text{V}$	-0.5			mA
Output Low Current	$I_{OL}$	$V_{OL} = 0.4\text{V}$	4.0			mA
Standby Current	$I_{CCS1}$	$\overline{CE} = 2.0\text{V}$			0.1	mA
Standby Current	$I_{CCS2}$	$\overline{CE} \geq V_{CC} - 0.3\text{V}, T_A = +60^\circ\text{C}$			500	nA
Standby Current	$I_{CCS2}$	$\overline{CE} \geq V_{CC} - 0.3\text{V}, T_A = +25^\circ\text{C}$			50	nA
Operating Current	$I_{CCO}$	$\overline{CE} = 0.6\text{V}$ min cycle			25	mA

**AC CHARACTERISTICS READ CYCLE**( $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ ;  $V_{CC} = 2.7\text{V}$  to  $3.5\text{V}$ )

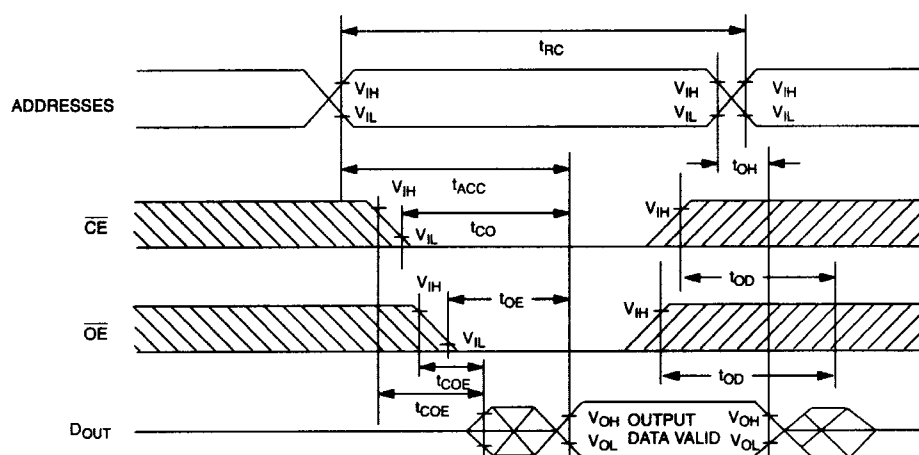
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Read Cycle Time	$t_{RC}$	250			ns	
Access Time	$t_{ACC}$			250	ns	
$\overline{OE}$ to Output Valid	$t_{OE}$			120	ns	
$\overline{CE}$ to Output Valid	$t_{CO}$			250	ns	
$\overline{CE}$ or $\overline{OE}$ to Output Active	$t_{COE}$	15			ns	
Output High-Z from Deselection	$t_{OD}$	5		100	ns	
Output Hold from Address Change	$t_{OH}$	15			ns	

**AC CHARACTERISTICS WRITE CYCLE** $(T_A = -40^{\circ}\text{C to } +85^{\circ}\text{C}; V_{CC} = 2.7\text{V to } 3.5\text{V})$ 

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Write Cycle Time	$t_{WC}$	250			ns	
Write Pulse Width	$t_{WP}$	190			ns	
Address Setup Time	$t_{AW}$	0			ns	
Write Recovery Time	$t_{WR}$	25			ns	
Output High-Z from $\overline{WE}$	$t_{ODW}$			90	ns	
Output Active from $\overline{WE}$	$t_{OEW}$	5			ns	
Data Setup Time	$t_{DS}$	100			ns	
Data Hold Time	$t_{DH}$	0			ns	

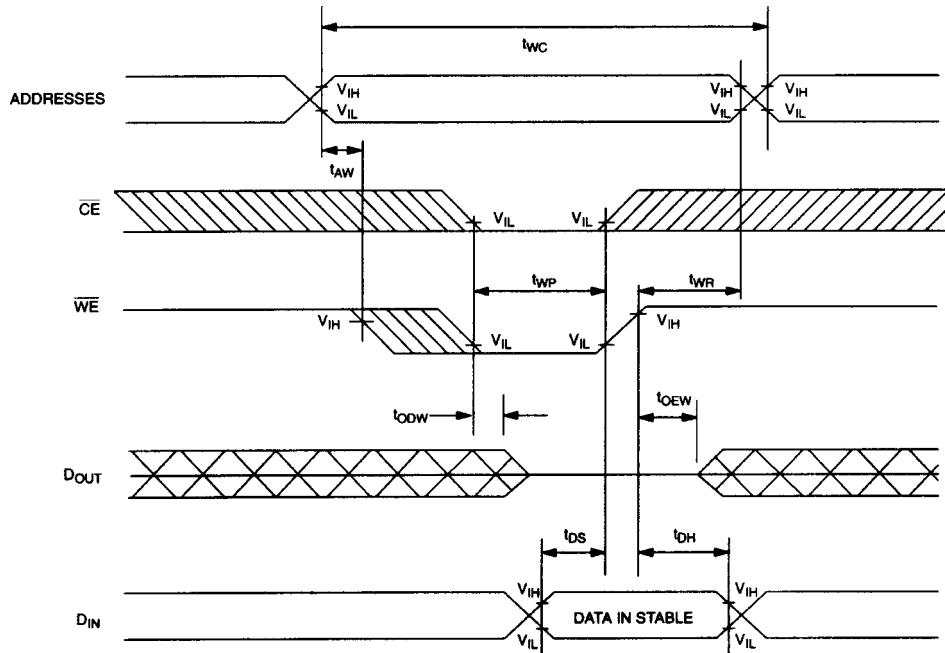
**DATA RETENTION CHARACTERISTICS** $(T_A = -40^{\circ}\text{C to } +85^{\circ}\text{C})$ 

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Data Retention Supply Voltage	$V_{DR}$	$\overline{CE} \geq V_{CC} - 0.3\text{V}$	2.0		3.5	V
Data Retention Current at 3.5V	$I_{CCR1}$	$\overline{CE} \geq V_{CC} - 0.3\text{V}$		50*	1000	nA
Data Retention Current at 2.0V	$I_{CCR2}$	$\overline{CE} \geq V_{CC} - 0.3\text{V}$		50*	750	nA
Chip Deselect to Data Retention	$t_{CDR}$		0			$\mu\text{s}$
Recovery Time	$t_R$		2			ms

\* Typical values are at  $+25^{\circ}\text{C}$ **TIMING DIAGRAM: READ CYCLE**

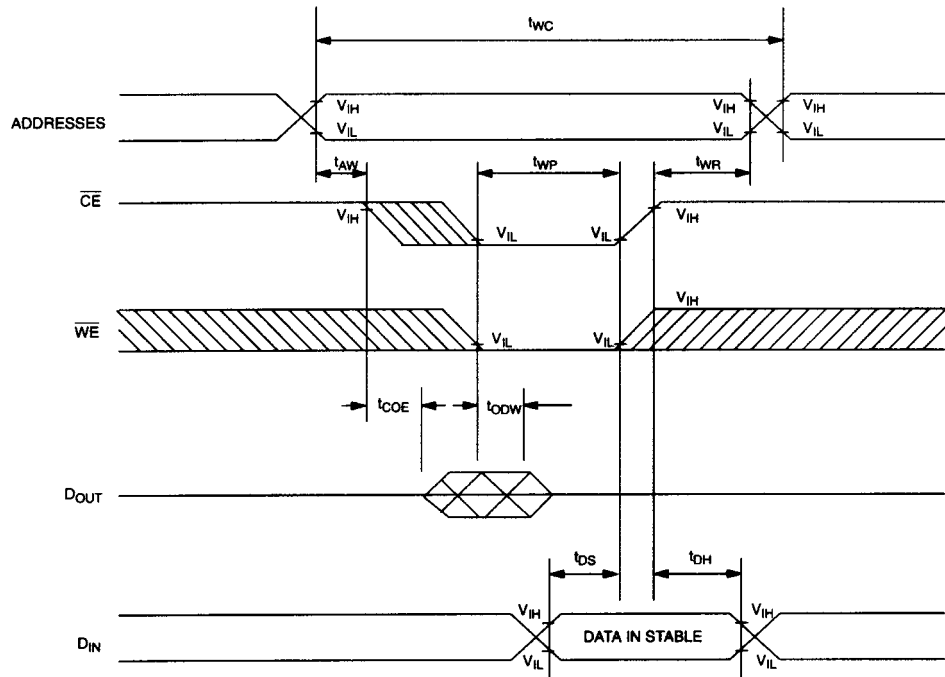
SEE NOTE 1

### TIMING DIAGRAM: WRITE CYCLE 1

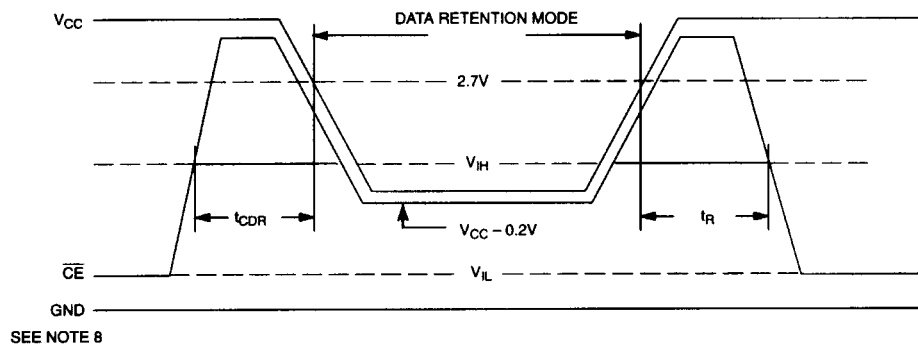


SEE NOTES 2, 3, 4, 5, 6, AND 7

### TIMING DIAGRAM: WRITE CYCLE 2



SEE NOTES 2, 3, 4, 5, 6, AND 7

**TIMING DIAGRAM: DATA RETENTION - POWER-UP, POWER-DOWN** Figure 1

SEE NOTE 8

SEE NOTE 8

**NOTES:**

- 1)  $\overline{WE}$  is high for read cycles.
- 2)  $\overline{OE} = V_{IH}$  or  $V_{IL}$ . If  $\overline{OE} = V_{IH}$  during write cycle, the output buffers remain in a high impedance state.
- 3)  $t_{WP}$  is specified as the logical AND of  $\overline{CE}$  and  $\overline{WE}$ .  $t_{WP}$  is measured from the latter of  $\overline{CE}$  or  $\overline{WE}$  going low to the earlier of  $\overline{CE}$  or  $\overline{WE}$  going high.
- 4)  $t_{DH}$  and  $t_{DS}$  are measured from the earlier of  $\overline{CE}$  or  $\overline{WE}$  going high.
- 5) If the  $\overline{CE}$  low transition occurs simultaneously with or later than the  $\overline{WE}$  low transition, the output buffers remain in a high impedance state.
- 6) If the  $\overline{CE}$  high transition occurs prior to or simultaneously with the  $\overline{WE}$  high transition, the output buffers remain in a high impedance state.
- 7) If  $\overline{WE}$  is low or the  $\overline{WE}$  low transition occurs prior to or simultaneously with the  $\overline{CE}$  low transition, the output buffers remain in a high impedance state.
- 8) If the  $V_{IH}$  level of CE is 2.0V during the period that  $V_{CC}$  voltage is going down from 4.5V to 2.7V,  $I_{CCS1}$  current flows.
- 9) The DS2016 maintains full operation from 5.5V to 2.7V. The electrical characteristics tables show two tested and guaranteed points of operation. For operation between 4.5V and 3.5V, use the composite worst case characteristics from both 5V and 3V operation for design purposes.

**DC TEST CONDITIONS**

Outputs Open

All voltages are referenced to ground.

**AC TEST CONDITIONS**

Output Load: 100pF + 1TTL Gate

Input Pulse Levels: 0V - 3.0V

Timing Measurement Reference Levels

Input: 1.5V

Output: 1.5V

Input Pulse Rise and Fall Times: 5ns

---

**PACKAGE INFORMATION**

For the latest package outline information, go to [www.maxim-ic.com/DallasPackInfo](http://www.maxim-ic.com/DallasPackInfo).