PCN Number:	20191103004	PCN Date:	Dec. 4, 2019
Title:	Datasheet for LMX2594		
Customer Contact:	PCN Manager	Dept:	Quality Services

Change Type:

☐	Assembly Site	☐	Design	☐	Wafer Bump Site
☐	Assembly Process	☒	Data Sheet	☐	Wafer Bump Material
☐	Assembly Materials	☐	Part number change	☐	Wafer Bump Process
☐	Mechanical Specification	☐	Test Site	☐	Wafer Fab Site
☐	Packing/Shipping/Labeling	☐	Test Process	☐	Wafer Fab Materials
				☐	Wafer Fab Process

Notification Details

Description of Change:

Texas Instruments Incorporated is announcing an information only notification.
The product datasheet(s) is being updated as summarized below.
The following change history provides further details.

TEXAS INSTRUMENTS

LMX2594

SNAS696C – MARCH 2017 – REVISED APRIL 2019

Changes from Revision B (March 2018) to Revision C **Page**

- Deleted the recommended bypass capacitor values for Vcc pins 7, 11, 15, 21, 26 and 37, as these capacitor values are not mandatory and the power supply filtering design is up to the user 7
- Changed all the 'FRAC_ORDER' to 'MASH_ORDER' to avoid confusion 9
- Changed the names of timing specs to align with timing diagram: changed t_{CE} to t_{ES}, t_{CS} to t_{DCS}, t_{CH} to t_{CDH}, and t_{CES} to t_{ECS} 11
- Changed the names of timing specs to align with timing diagram: changed t_{ES} to t_{CE}, t_{CES} to t_{ECS}, added t_{DCS} and t_{CDH}, and changed t_{CS} to t_{CR} 12
- Changed the serial data input timing diagram and corrected the typo for 'SCK' 12
- Deleted the note 'The CSB transition from high to low must occur when SCK is low' from the serial data input timing diagram, because SPI mode 4 (CPOL = 1, CPHA = 1) is also supported, and SCK is held high when idle in mode 4 12
- Added note for the serial data input timing diagram to explain the t_{CE} requirement for mode 4 (CPOL = 1, CPHA = 1) of SPI, because the diagram only indicated SPI mode 1 (CPOL = 0, CPHA = 0) 12
- Changed the serial data readback timing diagram 13
- Changed the note about MUXout clocking out and emphasized the effect of t_{CR} on the readback data available time 13
- Changed the f_{OUT} test conditions in the *Closed-Loop Phase Noise at 3.5 GHz* graph from: 14 GHz / 2 = 3.5 GHz to: to 14 GHz / 4 = 3.5 GHz 15
- Added *Normalized Output Power Across OUTA_PWR With Resistor Pullup* graph 15
- Changed "Vtune" to "Indirect Vtune" when LD_TYPE = 1 21
- Changed description for LD_TYPE. 21
- Added description of Indirect Vtune. 22
- Added description for the 'no assist' mode, mphasized the effect of VCO_SEL, VCO_DACISET_STRT and VCO_CAPCTRL_STRT under 'no assist' mode, and added recommended values for these registers 23
- Added description for the 'full assist' mode to allow the user to set VCO amplitude and capcode using linear interpolation under certain conditions 23
- Changed *OUTx_PWR Recommendations for Resistor Pullup* table 25
- Added description for category 3 of SYNC feature stating that FCAL_EN needs to be 1. 29
- Changed description of MASH_SEED 29

Revision History (continued)

- Added 10-ms wait time before re-programming register R0 in recommended initial power-up sequence 40
- Added the *General Programming Requirements* section based on frequently asked questions 40
- Changed register R4 in the register map to: exposed ACAL_CMP_DLY 41
- Changed the register R20[14] value from 0 to 1 in the full register map to match the R20 register description 41
- Changed the default value of R25 to align with register map of LMX2595. This change has no impact on the LMX2594 . 42
- Changed the R0[14] register field name in the register map from VCO_PHASE_SYNC_EN to VCO_PHASE_SYNC. to align with the rest of the data sheet 46
- Added recommended value for register CAL_CLK_DIV when lock time is not of concern..... 46
- Changed the typo for register 'VCO_DACISET' in the register map. Bit 0 of this register was not included in the map. The full register map and register description were correct 48
- Added description to the R4[15:8]: ACAL_CMP_DLY register..... 48
- Deleted the bit description '0: disabled; 1: enabled' for register 'PLL_N' 49
- Added description to the R60[15:0] LD_DLY register 51
- Changed the R31[14] register name from CHDIV_DIV2 to SEG1_EN to align with the naming in the TICS Pro GUI 53
- Changed the R105[1:0] field name from RAMP_NEXT_TRIG to RAMP1_NEXT_TRIG 58
- Added the *Bias Levels of Pins* table..... 64

The datasheet number will be changing.

Device Family	Change From:	Change To:
LMX2594	SNAS696B	SNAS696C

These changes may be reviewed at the datasheet links provided.

http://www.ti.com/product/LMX2594

Reason for Change:

To accurately reflect device characteristics.

Anticipated impact on Fit, Form, Function, Quality or Reliability (positive / negative):

No anticipated impact. This is a specification change announcement only. There are no changes to the actual device.

Changes to product identification resulting from this PCN:

None.

Product Affected:

LMX2594RHAR	LMX2594RHAT		

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