AN-1525
APPLICATION NOTE

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High Precision, Digital-to-Analog Conversion Using the 16-Bit AD5541/AD5542 Voltage Output DAC, ADR421 Reference, and the AD8628 Auto-Zero Op Amp

CIRCUIT FUNCTION AND BENEFITS

The circuit shown in Figure 1 provides precision data conversion using the AD5542 voltage output digital-to-analog converter (DAC) together with the ADR421 voltage reference and the AD8628 auto-zero operational amplifier (op amp) as the reference buffer. The AD8628 reference buffer provide benefits previously found only in expensive, auto-zeroing or chopper stabilized amplifiers. Using Analog Devices, Inc., circuit topology, these zero drift amplifiers combine low cost with high accuracy and low noise. No external capacitor is required, and the digital switching noise associated with most chopper-stabilized amplifiers is greatly reduced, making the AD8628 an ideal choice for reference buffering.

This circuit provides precision, low power, voltage output, digital-to-analog conversion. The AD5542 can be operated in buffered or unbuffered mode. The application and its requirements on settling time, input impedance, and noise determine which mode of operation is best. The selection of the output buffer amplifier can be tailored to suit dc precision or fast settling time. An output buffer is required where the DAC is required to drive a load less than 60 kΩ. The output impedance of the DAC is constant and code independent, however, to minimize gain errors, the input impedance of the output amplifier must be as high as possible. The output amplifier must have a 3 dB bandwidth of 1 MHz or greater. The output amplifier adds another time constant to the system, increasing the settling time of the final output.

A higher 3 dB amplifier bandwidth results in a faster effective settling time of the combined DAC and amplifier. All devices in the circuit can be powered from a single 5 V supply. The input voltage range of the ADR421 reference is 4.5 V to 18 V.

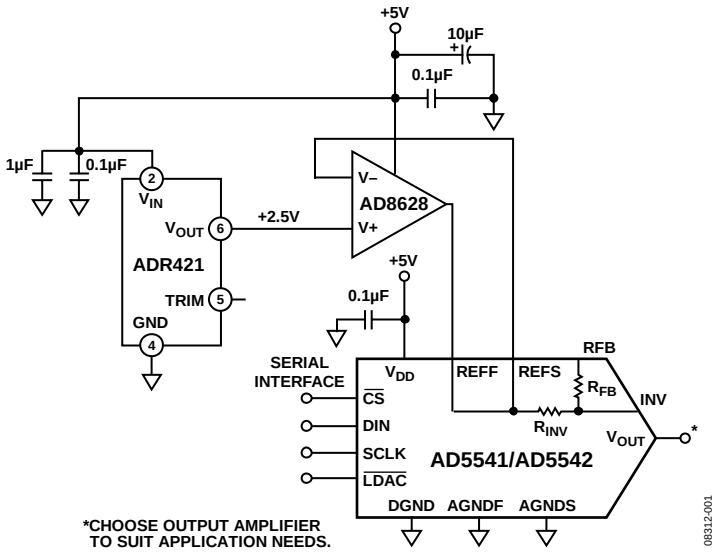

Figure 1. Precision DAC Configuration (Simplified Schematic)

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REVISION HISTORY

1/2018—Rev. 0 to Rev. A

Document Title Changed from CN0079 to AN-1525 ..... Universal
Change to Figure 1 1
Changes to Circuit Description Section, Figure 2, and Figure 3 3
Changes to Common Variations Section 5

8/2009—Revision 0: Initial Version

CIRCUIT DESCRIPTION

This circuit uses the AD5542 voltage output DAC, providing 16-bit, fully accurate performance. The DAC architecture of the AD5541/AD5542 is a segmented, rail-to-rail voltage mode DAC. With this type of configuration, the output impedance is independent of digital code, whereas the input impedance seen by the reference is heavily code dependent. For this reason, the reference buffer choice is important to account for the code dependent reference current, which can lead to linearity errors if the DAC reference is not adequately buffered. The op amp offset voltage, offset error temperature coefficient, and noise are important criteria when selecting a reference buffer with precision voltage output DACs. Offset errors in the reference circuit cause gain errors on the DAC output. This circuit uses the AD8628 zero drift, single-supply, rail-to-rail, input/output op amp. The AD8628 has an offset voltage of 1 μV (typical) drift of less than 0.005 μV/°C, and noise of 0.5 μV p-p (0.1 Hz to 10 Hz), and is suited for applications where error sources need to be minimized. The output voltage (V_{OUT}) is dependent on the reference voltage (V_{REF}), as shown in the following equation:

$$V_{OUT} = V_{REF} \times D/2^N$$

where:
D is the decimal data-word loaded to the DAC register.
N is the resolution of the DAC.

For a reference of 2.5 V, the equation is simplified to the following:

$$V_{OUT} = 2.5\ V \times D/65{,}536$$

Therefore, V_{OUT} is 1.25 V for the midscale code and 2.5 V for the full-scale code.

The LSB size is 2.5 V/65,536, or 38.1 μV.

There is a common misconception that auto-zero amplifiers are not to be trusted because of intermodulation terms and unwanted harmonics filtering through to the output due to the internal switching action. Previous auto-zero amplifiers used auto-zeroing or chopper stabilization techniques. Traditional auto-zeroing results in low noise energy at the auto-zeroing frequency at the expense of higher low frequency noise, due to aliasing of wide-band noise into the auto-zeroed frequency band. Chopping results in less low frequency noise at the expense of larger noise energy at the chopping frequency. The AD8628 family uses both auto-zeroing and chopping in a patented ping-pong arrangement to obtain lower low frequency noise together with lower energy at the chopping and auto-zeroing frequencies, maximizing the signal-to-noise ratio (SNR) for the majority of applications without the need for additional filtering. The relatively high internal chopping frequency of 15 kHz simplifies filter requirements for a wide, useful, noise free bandwidth in instrumentation and process control applications.

Measured results show that high accuracy, low noise performance with minimum high frequency intermodulation distortions transferred to the output is achievable using the AD8628 as a reference buffer in a high accuracy, high performance system.

Integral nonlinearity (INL) error is the deviation in LSBs of the actual DAC transfer function from an idealized transfer function. Differential nonlinearity (DNL) error is the difference between an actual step size and the ideal value of 1 LSB. The circuit in Figure 1 provides 16-bit resolution with ±1 LSB INL error and ±1 LSB DNL error. Figure 2 and Figure 3 show the INL and DNL performance of the circuit.

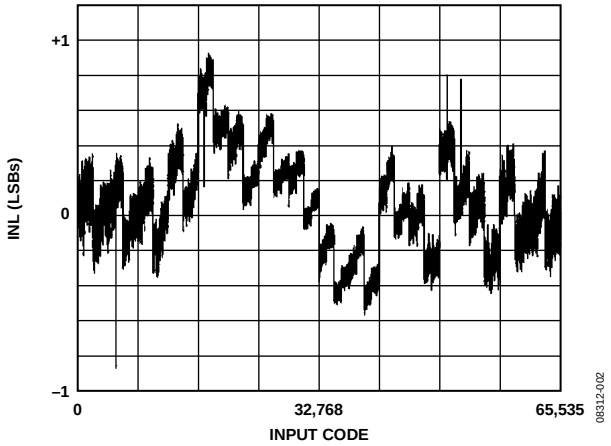

Figure 2. INL Error vs. Input Code

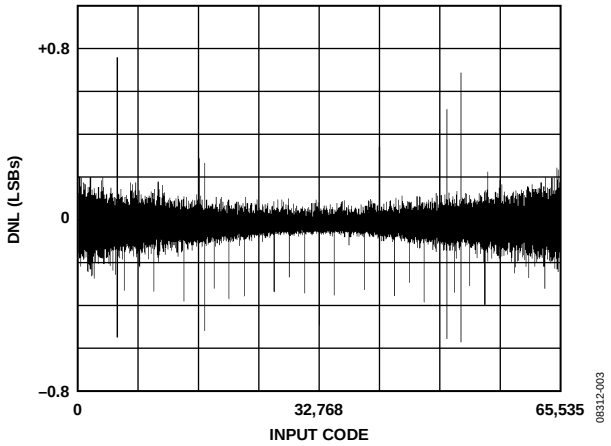

Figure 3. DNL Error vs. Input Code

The offset error and gain error are 10 μV and 170 μV, respectively. The gain error of ±5 LSBs and the zero code error of ±1 LSB are within the specified 38 μV (with a 2.5 V reference) at ambient temperature.

Figure 4 shows a 0.1 Hz to 10 Hz noise plot for the circuit. The output of the DAC, V_{OUT}, is connected to the input of a 0.1 Hz to 10 Hz bandwidth filter, followed by an amplifier with a gain of 10,000. The voltage noise is captured on a scope. A low peak-to-peak voltage of 57 mV is observed (5.7 µV with respect to the DAC output).

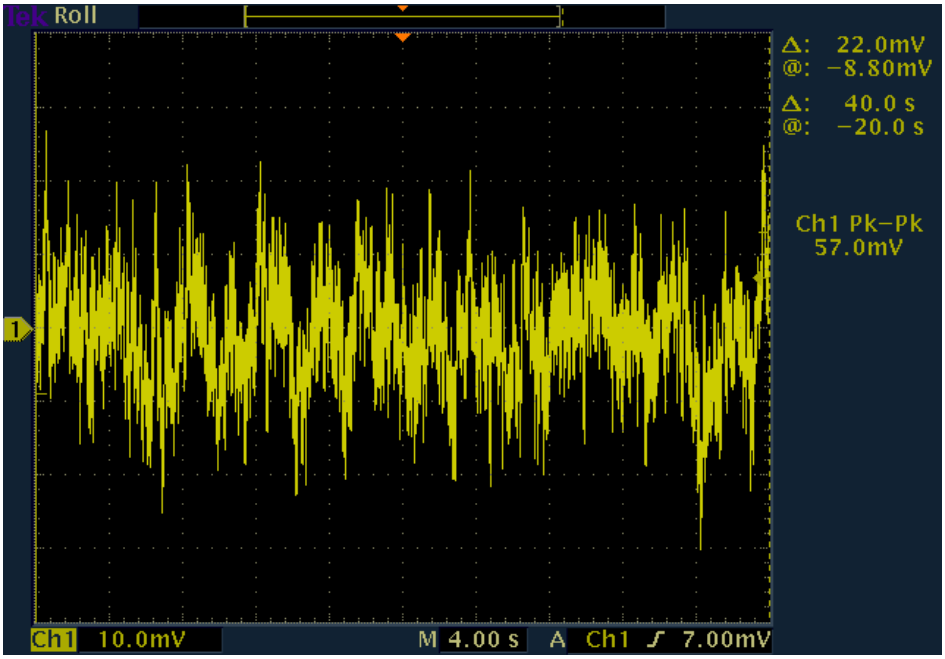

Figure 4. 0.1 Hz to 10 Hz Output Noise Plot; Full-Scale Code Loaded Into DAC (1/f Noise = 57 mV/10,000 = 5.7 µV)

Figure 5 shows the DAC output using the spectrum analyzer sweeping from 100 Hz to 100 kHz. No significant intermodulation distortion (IMD) terms were observed, showing that auto-zero amplifiers such as the AD8628 are ideal choices for reference buffers.

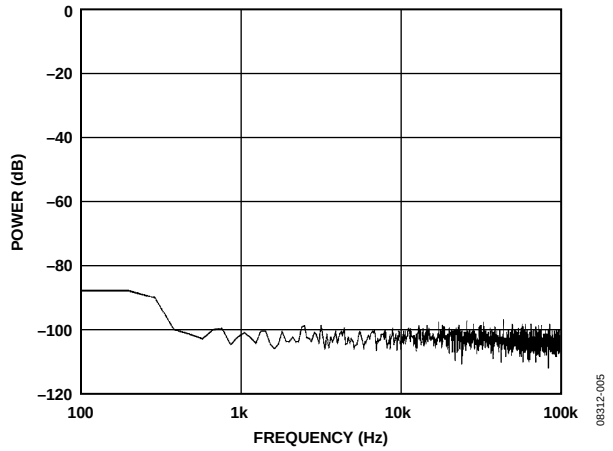

Figure 5. DAC Output Spectral Density Plot (dB Referenced to Full-Scale)

In any circuit where accuracy is important, it is helpful to carefully consider the power supply and ground return layout on the board. It is recommended that the printed circuit board (PCB) containing the circuit has separate analog and digital sections. If the circuit is used in a system where other devices require an AGND-to-DGND connection, make the connections at one ground point only, as close as possible to the AD5542. Bypass the power supply to the AD5542 with 10 µF and 0.1 µF capacitors. The capacitors must be as physically close as possible to the device, with the 0.1 µF capacitor ideally right up against the device. The 10 µF capacitors are tantalum beads. It is important that the 0.1 µF capacitors have low effective series resistance (ESR) and low effective series inductance (ESL), which is typical of common ceramic types of capacitors. These 0.1 µF capacitors provide a low impedance path to ground for high frequencies caused by transient currents due to internal logic switching. The power supply line must have as large a trace as possible to provide a low impedance path and reduce glitch effects on the supply line. Shield clocks and other fast switching digital signals from other parts of the board by digital ground.

The circuit must be constructed on a multilayer PCB with a large area ground plane. Use proper layout, grounding, and decoupling techniques to achieve optimum performance (see Tutorial MT-031, *Grounding Data Converters and Solving the Mystery of "AGND" and "DGND"* and Tutorial MT-101, *Decoupling Techniques*).

COMMON VARIATIONS

The AD8538 is another excellent auto-zero op amp candidate to be used for buffering the reference in this circuit. It provides a low offset voltage and ultralow bias current. The 2.500 V (typical) output ADR421 can be replaced by either the ADR423 or the ADR425, which are low noise references available from the same reference family as the ADR421, and provide 3 V and 5 V, respectively. The ADR441 and the ADR431 ultralow noise references are suitable substitutes that provide 2.5 V (typical). The size of the reference input voltage is restricted by the rail-to-rail output voltage capability of the operational amplifier selected.

There is no output buffer used in this circuit, because output buffer performance can be optimized for speed or dc precision, depending on the system bandwidth and application need. The AD8605 or the AD8655 are also suitable output buffer options.

REFERENCES

Kester, Walt. 2005. Chapter 3 and Chapter 7. *The Data Conversion Handbook.* Analog Devices.

MT-015 Tutorial, *Basic DAC Architectures II: Binary DACs,* Analog Devices.

MT-016 Tutorial, *Basic DAC Architectures III: Segmented DACs,* Analog Devices.

MT-031 Tutorial, *Grounding Data Converters and Solving the Mystery of "AGND" and "DGND",* Analog Devices.

MT-035 Tutorial, *Op Amp Inputs, Outputs, Single-Supply, and Rail-to-Rail Issues*, Analog Devices.

MT-055 Tutorial, *Chopper Stabilized (Auto-Zero) Precision Op Amps*, Analog Devices.

MT-101 Tutorial, *Decoupling Techniques*, Analog Devices.

Voltage Reference Wizard Selection Tool.

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