| **PCN Number:** | 20170613006 | **PCN Date:** | June 21, 2017 |
|---|---|---|---|
| **Title:** | TPS65381QDAPRQ1 new die revision | | |
| **Customer Contact:** | PCN Manager | **Dept:** | Quality Services |
| **Proposed 1st Ship Date:** | Dec. 21, 2017 | **Estimated Sample Availability:** | Date provided at sample request |

**Change Type:**

| | | | | | |
|---|---|---|---|---|---|
| ☐ | Assembly Site | ☒ | Design | ☐ | Wafer Bump Site |
| ☐ | Assembly Process | ☐ | Data Sheet | ☐ | Wafer Bump Material |
| ☐ | Assembly Materials | ☐ | Part number change | ☐ | Wafer Bump Process |
| ☐ | Mechanical Specification | ☐ | Test Site | ☐ | Wafer Fab Site |
| ☐ | Packing/Shipping/Labeling | ☐ | Test Process | ☐ | Wafer Fab Materials |
| | | | | ☐ | Wafer Fab Process |

## PCN Details

**Description of Change:**

Texas Instruments Incorporated is announcing the qualification of a new metal level only design revision to device TPS65381QDAPRQ1.

The release of new design revision addresses the following fixes:
- Timing violation to fix Scan (digital change only)
- Vgs issue on two spare FETs (no impact on parametric, only to eliminate reliability concerns)

**Reason for Change:**

To correct known design issues to enable scan at production test and eliminate reliability concerns related to Vgs issue.

**Anticipated impact on Fit, Form, Function, Quality or Reliability (positive / negative):**

None

**Changes to product identification resulting from this PCN:**

None

**Product Affected:**

TPS65381QDAPRQ1

# Automotive New Product Qualification Summary
# (As per AEC-Q100H and JEDEC Guidelines)

## TPS65381AQDAPRQ1
## Approved March 20, 2017

### Product Attributes

| Attributes | Qual Device: TPS65381AQDAPRQ1 | Product QBS Reference: TPS65381QDAPRQ1 | Product/Process/Package QBS Reference: TPS65300QPWPRQ1 |
|---|---|---|---|
| **Automotive Grade Level** | Grade 1 | Grade 1 | Grade 1 |
| **Operating Temp Range** | -40°C to +125°C | -40°C to +125°C | -40°C to +125°C |
| **Product Function** | Power Management | Power Management | Power Management |
| **Wafer Fab Supplier** | DMOS5 | DMOS5 | DMOS5 |
| **Die Revision** | C2 | A0 | A0 |
| **Assembly Site** | Taiwan | Taiwan | Taiwan |
| **Package Designator** | DAP | DAP | PWP |
| **Ball/Lead Count** | 32 | 32 | 24 |

- QBS: Qual By Similarity
- Qual device is stressed for MSL3

**Qualification Results**
**Data Displayed as: Number of lots / Total sample size / Total failed**

| Type | # | Test Spec | Min Lot Qty | SS/Lot | Test Name / Condition | Duration | Qual Device: TPS65381AQDAPRQ1 | Product QBS Reference: TPS65381QDAPRQ1 | Product/Process/Package QBS Reference: TPS65300QPWPRQ1 |
|---|---|---|---|---|---|---|---|---|---|
| Test Group A – Accelerated Environment Stress Tests | | | | | | | | | |
| PC | A1 | JEDEC J-STD-020 JESD22-A113 | 3 | 77 | Automotive Preconditioning Level 3 | 260C peak | - | 3/all/0 | 3/all/0 |
| HAST | A2 | JEDEC JESD22-A110 | 3 | 77 | Biased HAST, 130C/85 %RH | 96 hours | - | 3/231/0 | 3/231/0 |
| | A3 | JEDEC JESD22-A102 | 3 | 77 | Autoclave 121C | 96 hours | - | 3/231/0 | 3/231/0 |
| TC | A4 | JEDEC JESD22-A104 and Appendix 3 | 3 | 77 | Temperature Cycle, -65/150C | 500 cycles | - | 3/227/0 | 3/227/0 |
| | | | 1 | 5 | Bond Wire Pull | Post Temp Cycle 500 cycles | - | - | 1/5/0 |
| | | | 1 | 5 | Bond shear | Post Temp Cycle 500 cycles (for information only) | - | - | 1/5/0 |
| | | | 3 | 12 | SAM | Post Temp Cycle 500 cycles (for information only) | - | 3/36/0 | 3/36/0 |
| | | | | | Temperature Cycle, -65/150C | 1000 cycles (for information only) | - | 3/227/0 | 3/231/0 |
| PTC | A5 | JEDEC JESD22-A105 | 1 | 45 | Power Temperature Cycle, -40/125C | 1000 cycles | - | 1/45/0 | 3/135/0 |
| HTSL | A6 | JEDEC JESD22-A103 | 1 | 45 | High Temp Storage Bake 175C | 500 hours | - | 1/45/0 | 3/135/0 |
| Test Group B – Accelerated Lifetime Simulation Tests | | | | | | | | | |
| HTOL | B1 | JEDEC JESD22-A108 | 3 | 77 | HTOL 125C | 1000 hours | - | 1/77/0 (rev. C1) | 3/231/0 |
| | | | | | HTOL | 2000 hours | - | 1/77/0 | - |

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | 125C | (for information only) | | (rev. C1) | |
| ELFR | B2 | AEC Q100-008 | 3 | 800 | Early Life Failure Rate, 125C | 48 hours | - | 1/800/0 (rev. C1) | 3/2400/0 |
| **Test Group C – Package Assembly Integrity Tests** | | | | | | | | | |
| WBS | C1 | AEC Q100-001 | 1 | 30 | Wire Bond Shear | Cpk>1.67 | 1/30/0 | 1/30/0 | 1/30/0 |
| WBP | C2 | MIL-STD883 Method 2011 | 1 | 30 | Wire Pull | Cpk>1.67 | 1/30/0 | 1/30/0 | 1/30/0 |
| SD | C3 | JEDEC JESD22-B102 | 1 | 15 | Surface Mount Solderability | - | - | 1/15/0* | 1/15/0 |
| PD | C4 | JEDEC JESD22-B100 and B108 | 3 | 10 | Physical Dimensions | Cpk>1.67 | - | 3/30/0* | 3/30/0* |
| SBS | C5 | AEC Q100-010 | 3 | 50 | Solder Ball Shear (Cpk>1.67) | Post HTSL/Bump | NA | NA | NA |
| LI | C6 | JEDEC JESD22-B105 | 1 | 50 | Lead Integrity | - | NA | NA | NA |
| **Test Group D – Die Fabrication Reliability Tests** | | | | | | | | | |
| EM | D1 | JESD61 | - | - | Electromigration | - | Completed Per Process Technology Requirements | Completed Per Process Technology Requirements | Completed Per Process Technology Requirements |
| TDDB | D2 | JESD35 | - | - | Time Dependent Dielectric Breakdown | - | Completed Per Process Technology Requirements | Completed Per Process Technology Requirements | Completed Per Process Technology Requirements |
| HCI | D3 | JESD60 & 28 | - | - | Hot Injection Carrier | - | Completed Per Process Technology Requirements | Completed Per Process Technology Requirements | Completed Per Process Technology Requirements |
| NBTI | D4 | - | - | - | Negative Bias Temperature Instability | - | Completed Per Process Technology Requirements | Completed Per Process Technology Requirements | Completed Per Process Technology Requirements |
| SM | D5 | - | - | - | Stress Migration | - | Completed Per Process Technology Requirements | Completed Per Process Technology Requirements | Completed Per Process Technology Requirements |
| **Test Group E – Electrical Verification Tests** | | | | | | | | | |
| HBM | E2 | AEC Q100-002 | 1 | 3 | ESD - HBM - Q100 | 2000 V | 1/3/0 | 1/3/0 | 1/3/0 |
| CDM | E3 | AEC Q100-011 | 1 | 3 | ESD - CDM - Q100 | 500 V (all pins) 750 V (corner | 1/3/0 | 1/3/0 | 1/3/0 |

| | | | | | | pins) | | | |
|---|---|---|---|---|---|---|---|---|---|
| LU | E4 | AEC Q100-004 | 1 | 6 | Latch-up | RT and 125C | 1/6/0 | 1/6/0 | 1/6/0 |
| ED | E5 | AEC Q100-009 | 3 | 30 | Auto Electrical Distributi ons | Cpk>1.67 Room, hot, and cold test | 1/30/0 | 3/90/0 | 3/90/0 |

**A1 (PC): Preconditioning:** Performed for THB, Biased HAST, AC, uHAST &TC samples, as applicable.

**Operating Temperature by Automotive Grade Level:**
Grade 0 (or E): -40°C to +150°C
Grade 1 (or Q): -40°C to +125°C
Grade 2 (or T): -40°C to +105°C
Grade 3 (or I): -40°C to +85°C

**E1 (TEST): Electrical test temperatures of Qual samples (High temperature according to Grade level):**
Room/Hot/Cold: HTOL, ED
Room/Hot: THB / HAST, TC / PTC, HTSL, ELFR, ESD & LU
Room: AC/uHAST

**Green/Pb-free Status:**
Qualified Pb-Free(SMT) and Green

Note: QBS data for solderability (NiPdAu) and Physical Dimensions (DAP) are taken using different devices with same package material and process by same assembly site.

**Quality and Reliability Data Disclaimer**

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Reliability data shows characteristic failure mechanisms of the specific environmental stress as documented in the industry standards for each stress condition.

For questions regarding this notice, e-mails can be sent to the regional contacts shown below or your local Field Sales Representative.

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