DP83TG720S-Q1 1000BASE-T1 Automotive Ethernet PHY with SGMII and RGMII

1 Features

- IEEE802.3bp 1000BASE-T1 compliant
- Open Alliance TC12 Interoperability and EMC compliant
  - Interoperability tested with OA/IEEE compliant PHYs
  - EMC immunity Class-IV compliant for UTP (unshielded twisted pair)
- Integrated LPF on MDI pins
- MAC Interfaces: RGMII and SGMII
- Supported I/O voltages: 3.3 V, 2.5 V, and 1.8 V
- Pin compatible with TI's 100BASE-T1 PHY
  - Single board design for 100BASE-T1 and 1000BASE-T1 with required BOM change
- Power savings features:
  - Standby and sleep
  - Local and remote wake-up
- Diagnostic tool kit
  - High accuracy temperature monitor
  - Voltage monitor
  - ESD event monitor
  - Data throughput calculator: inbuilt MAC packet generator, counter and error checker
  - Link quality monitoring
  - Cable open and short fault detection
  - Loopback modes
- 25 MHz clock output source
- VQFN, wettable flank packaging
- AEC-Q100 Qualified
  - Inbuilt ESD protection : IEC61000-4-2 ESD : ±8 kV contact discharge
  - Device temperature grade 1: –40°C to +125°C ambient operating temperature

2 Applications

- Telematics control unit (TCU, TBOX)
- Gateway and Body Control Module (BCM)
- ADAS: LIDAR, RADAR, Front Camera

3 Description

The DP83TG720S-Q1 device is an IEEE 802.3bp and Open Alliance compliant automotive Ethernet physical layer transceiver. It provides all physical layer functions needed to transmit and receive data over unshielded/shielded single twisted-pair cables. The device provides xMII flexibility with support for RGMII and SGMII MAC interfaces.

DP83TG720 is compliant to Open Alliance EMC and interoperable specifications over unshielded twisted cable. DP83TG720 is front print compatible to TI's 100BASE-T1 PHY enabling design scalability with single board for both speeds. This device offers the Diagnostic Tool Kit, with an extensive list of real-time monitoring tools, debug tools and test modes. Within the tool kit is the first integrated electrostatic discharge (ESD) monitoring tool. It is capable of counting ESD events on both the xMII and MDI as well as providing real-time monitoring through the use of a programmable interrupt. Additionally, the DP83TG720S-Q1 includes a data generator and checker tool to generate customizable MAC packets and check the errors on incoming packets. This enables system level datapath tests/optimizations without dependency on MAC.

Device Information

PART NUMBER	PACKAGE (1)	BODY SIZE (NOM)
DP83TG720S-Q1	VQFN (36)	6.00 mm × 6.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

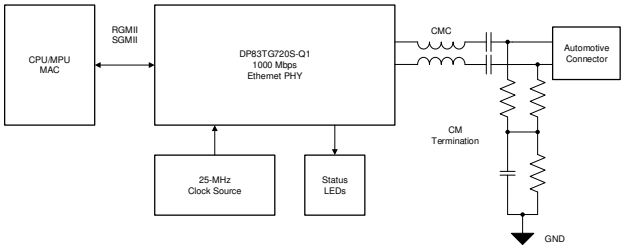

Figure 3-1. Simplified Schematic

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (March 2021) to Revision E (February 2022) — **Page**

- Updated the title of document....0
- Updated the Strap_1 pin state in the Pin Function table to input only. Separated the Pin states table and Pin Power domain tables....4
- Updated the INH pin in power/reset to PMOS, OD, O in the Pin States table. Updated abbreviations....6
- Added the Pin Power Domain Table....9
- SQI section updated to indicate improved number of SQI levels with updated computation method....26
- Updated the link for the TDR application note....26
- Changed the 0x0016 register value to 0x0108, 0x0104, 0x0101 for analog loopback, digital loopback, and PCS loopback....31
- Updated the step of local and remote sleep entry....41
- Formatted the bit descriptions for more clarity, removed the reserved registers and added extra registers as required by some customer applications....191
- Updated the CM resistor packaging recommendation 0805....202

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- IOZ, 2 level boot-strap's Mode 2 threshold and Rpull-down min/max datasheet limits updated to give more margin to customer application....10
- Min/Max values of rgmii DLL_TX_DELAY, sleep mode timing parameters, latency parameters, reset mode power, standby mode power and sleep mode power added....10
- Changed Integrated Pull-Down Resistance from 4.5 kΩ to 4.725 kΩ....10
- Further details added to remote sleep exit procedure....41
- Note added for more margins for 1.8V two level straps....54

Changes from Revision B (February 2021) to Revision C (February 2021) — **Page**

- Updated the Pull-down resistor value of rx_cntrl and strp_1 pins in pin-state tables. Changed from 6 K to 6.3 K to match exact value in the Specifications section....4
- SQI section updated to meet OA requirements....26

- Strap circuit diagram updated to remove external pull-down.....54

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- Updated Power Supply Recommendation Note..... 203

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- Changed marketing status from Advance Information to initial release.....1

5 Pin Configuration and Functions

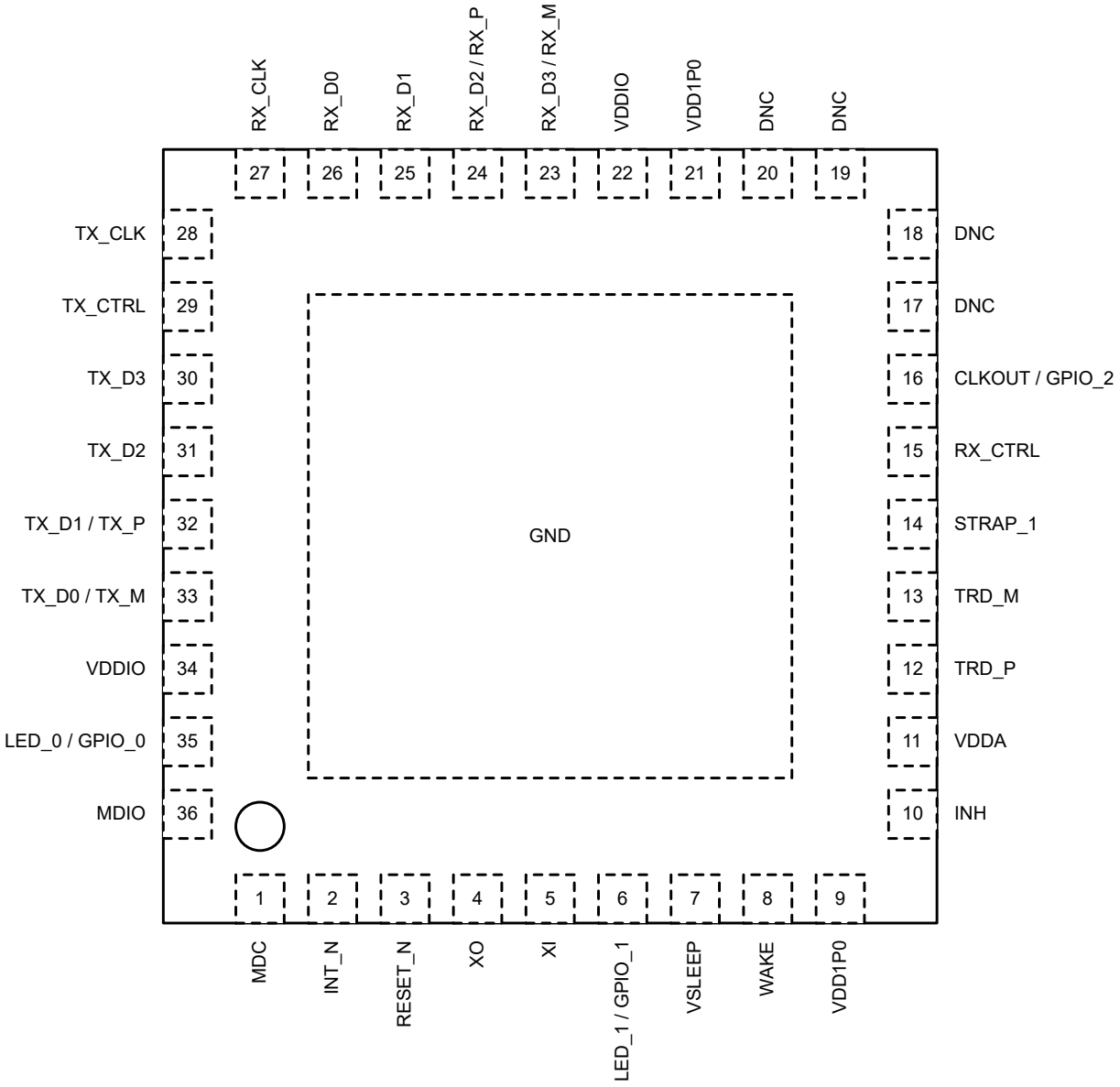

Figure 5-1. RHA Package
36-Pin VQFN
Top View

Pin Functions

Table 5-1. Pin Functions

PIN		STATE[1]	DESCRIPTION [2]
NAME	NO.		
MAC INTERFACE			
RX_D3 RX_M	23	S, PD, O	**Receive Data:** Symbols received on the cable are decoded and transmitted out of these pins synchronous to the rising edge of RX_CLK. They contain valid data when RX_DV(decoded from RX_CTL) is asserted. A nibble, RX_D[3:0], is transmitted in RGMII mode. **RX_M / RX_P:** Differential SGMII Data Output. These pins transmit data from the PHY to the MAC.
RX_D2 RX_P	24		
RX_D1	25		
RX_D0	26		
RX_CLK	27	O	**Receive Clock:** In RGMII mode, PHY provides this 125-MHz clock to MAC. **Unused in SGMII mode**
RX_CTRL	15	S, PD, O	**RGMII Receive Control:** Receive control combines receive data valid indication and receive error indication into a single signal. RX_DV is presented on the rising edge of RX_CLK and RX_ER is presented on the falling edge of RX_CLK. **Used only as strap in SGMII mode**
TX_CLK	28	I	**Transmit Clock:** In RGMII mode, MAC provides this 125-MHz clock to PHY. **Unused in SGMII mode**
TX_CTRL	29	I	**RGMII Transmit Control:** Transmit control combines transmit enable and transmit error indication into a single signal. TX_EN is presented prior to the rising edge of TX_CLK; TX_ER is presented on the falling edge of TX_CLK. **Unused in SGMII mode**
TX_D3	30	I	**Transmit Data:** In RGMII mode, the transmit data nibble, TX_D[3:0], is received from the MAC . **TX_M / TX_P:** Differential SGMII Data Input. These pins receive data that is transmitted from the MAC to the PHY.
TX_D2	31		
TX_D1 TX_P	32		
TX_D0 TX_M	33		
SERIAL MANAGEMENT INTERFACE			
MDC	1	I	**Management Data Clock:** Synchronous clock to the MDIO serial management input and output data.
MDIO	36	OD, IO	**Management Data Input/Output:** Bidirectional management data signal that may be sourced by the management station or the PHY. This pin requires an external pull-up resistor (recommended value = 2.2-kΩ) .
CONTROL INTERFACE			
$\overline{\text{INT}}$	2	PU, OD, O	**Interrupt:** Active-LOW output, which will be asserted LOW when an interrupt condition occurs. This pin has a weak internal pullup. Register access is necessary to enable various interrupt triggers. Once an interrupt event flag is set, register access is required to clear the interrupt event on this pin. This pin can be configured as an Active-HIGH output using register[0x0011]. To capture the interrupt source reliably, status from interrupt registers x12, x13, x18 is recommended to be read after interrupt is asserted on int_n pin.
$\overline{\text{RESET}}$	3	PU, I	**RESET:** Active-LOW input, which initializes or reinitializes the DP83TG720S-Q1. Asserting this pin LOW for at least 10 µs will force a reset process to occur. All internal registers will reinitialize to their default states as specified for each bit in the Register Map section. All bootstrap pins are resampled upon deassertion of reset.
INH	10	PMOS OD	**INH:** Active-HIGH PMOS open-drain output. When the PHY enters the sleep state, PHY will release the INH pin to allow an external pull-down resistor (recommended value = 10 kΩ) to pull the line to ground. When in any other state, the INH pin will drive a HIGH state to the VSLEEP rail.
WAKE	8	PD, I	**WAKE:** Active-HIGH (this pin works on VSLEEP domain) pulse on wake-up pin wakes up the PHY from the sleep state. For pulse width, refer to timing section. This pin can be directly tied to the VSLEEP rail when the sleep state is not used or left float.

Table 5-1. Pin Functions (continued)

PIN		STATE[1]	DESCRIPTION [2]
NAME	NO.		
STRP_1	14	I	**Strap 1:** This pin is for strapping PHY_AD bits.
CLOCK INTERFACE			
XI	5	I	**Reference Clock Input:** Reference clock 25-MHz ±100 ppm-tolerance crystal or oscillator input. The device supports either an external crystal resonator connected across pins XI and XO, or an external CMOS-level oscillator connected to pin XI only and XO left floating.
XO	4	O	**Reference Clock Output:** XO pin is used for crystal only. This pin should be left floating when a CMOS-level oscillator is connected to XI.
LED/GPIO INTERFACE			
LED_0 / GPIO_0	35	S, PD, IO	**LED_0:** Link Status
LED_1 / GPIO_1	6	S, PD, IO	**LED_1:** Link Status and BLINK for TX/RX Activity
CLKOUT / GPIO_2	16	IO	**Clock Output:** 25-MHz reference clock(buffered replication of XI) by default. If not used, clock output can be disabled by writing register 0x0453 = 0x0006.
MEDIUM DEPENDENT INTERFACE			
TRD_M	13	IO	**Differential Transmit and Receive:** Bidirectional differential signaling configured for 1000BASE-T1 operation, IEEE 802.3bp compliant.
TRD_P	12		
POWER AND GROUND CONNECTIONS			
VDDA3P3	11	SUPPLY	**Core Supply:** 3.3 V. Refer to power supply recommendations for decoupling network.
VDDIO	22, 34	SUPPLY	**IO Supply:** 1.8 V, 2.5 V, or 3.3 V. Refer to power supply recommendations for decoupling network.
VDD1P0	9, 21	SUPPLY	**Core Supply:** 1.0 V. Refer to power supply recommendations for decoupling network.
VSLEEP	7	SUPPLY	**Sleep Supply:** 3.3 V. Refer to power supply recommendations for decoupling network. This pin shall be tied to VDDA3P3 if sleep functionality is not used.
GROUND	DAP	GROUND	**Ground**
DO NOT CONNECT			
DNC	17, 18, 19, 20	DNC	**DNC:** Do Not Connect (test structures connected to these pins and should be kept floating to avoid damage or wrong mode entry of PHY)

(1) Type: I = Input
O = Output
IO = Input/Output
OD = Open Drain
PD = Internal Pulldown
PU = Internal Pullup
S = Strap: Configuration pin (all configuration pins have weak internal pullups or pulldowns)

(2) When pins are unused, follow the recommended connection requirements provided in the table above. If pins do not have required termination, they may be left floating.

5.1 Pin States

Table 5-2. Pin States - RGMII

PIN NAME	POWER-UP / RESET			NORMAL OPERATION - RGMII		
	PIN STATE(1)	PULL TYPE	PULL VALUE (kΩ)	PIN STATE (1)	PULL TYPE	PULL VALUE (kΩ)
MDC	I	none	-	I	none	-
INT_N	I	PU	9	OD	PU	9
RESET_N	I	PU	9	I	PU	9
XO	O	none	-	O	none	-
XI	I	none	-	I	none	-
LED_1	I	PD	9	O	none	-
WAKE	I	PD	50	I	PD	50
STRP_1	I	PD	6.3	I	none	-
INH	PMOS,OD,O	none	-	PMOS OD, O	none	-
RX_CTRL	I	PD	6.3	O	none	-
CLKOUT/GPIO_2	O	none	-	O	none	-
RX_D3	I	PD	9	O	none	-
RX_D2	I	PD	9	O	none	-
RX_D1	I	PD	9	O	none	-
RX_D0	I	PD	9	O	none	-
RX_CLK	I	PD	9	O	none	-
TX_CLK	I	none	-	I	none	-
TX_CTRL	I	none	-	I	none	-
TX_D3	I	none	-	I	none	-
TX_D2	I	none	-	I	none	-
TX_D1	I	none	-	I	none	-
TX_D0	I	none	-	I	none	-
LED_0	I	PD	9	O	none	-
MDIO	I	none	-	IO	none	-

(1) Type: I = Input
O = Output
IO = Input/Output
OD = Open Drain
PD = Internal pulldown
PU = Internal pullup

Table 5-3. Pin States - SGMII

PIN NAME	POWER-UP / RESET			NORMAL OPERATION - SGMII		
	PIN STATE (1)	PULL TYPE	PULL VALUE (kΩ)	PIN STATE (1)	PULL TYPE	PULL VALUE (kΩ)
MDC	I	none	-	I	none	-
INT_N	I	PU	9	OD	PU	9
RESET_N	I	PU	9	I	PU	9
XO	O	none	-	O	none	-
XI	I	none	-	I	none	-
LED_1	I	PD	9	O	none	-
WAKE	I	PD	50	I	PD	50
STRP_1	I	PD	6.3	I	none	-
INH	PMOS,OD,O	none	-	PMOS OD, O	none	-
RX_CTRL	I	PD	6.3	I	PD	6.3
CLKOUT/GPIO_2	O	none	-	O	none	-
RX_D3	I	PD	9	O	none	-
RX_D2	I	PD	9	O	none	-
RX_D1	I	PD	9	Hi-Z	PD	9
RX_D0	I	PD	9	Hi-Z	PD	9
RX_CLK	I	PD	9	Hi-Z	PD	9
TX_CLK	I	none	-	Hi-Z	none	-
TX_CTRL	I	none	-	Hi-Z	none	-
TX_D3	I	none	-	Hi-Z	none	-
TX_D2	I	none	-	Hi-Z	none	-
TX_D1	I	none	-	I	none	-
TX_D0	I	none	-	I	none	-
LED_0	I	PD	9	O	none	-
MDIO	I	none	-	IO	none	-

(1) Type: I = Input
O = Output
IO = Input/Output
OD = Open Drain
PD = Internal pulldown
PU = Internal pullup
Hi-Z = High Impedence

Table 5-4. Pin States - Sleep and Isolate

PIN NAME	MAC ISOLATE			SLEEP		
	PIN STATE (1)	PULL TYPE	PULL VALUE (kΩ)	PIN STATE (1)	PULL TYPE	PULL VALUE (kΩ)
MDC	I	none	-	Float	none	-
INT_N	O	PU	9	Float	none	-
RESET_N	I	PU	9	Float	none	-
XO	O	none	-	Float	none	-
XI	I	none	-	Float	none	-
LED_1	O	none	-	Float	none	-
WAKE	I	PD	50	I	none	50
STRP_1	I	none	-	Float	none	-
INH	PMOS,OD,O	none	-	PMOS OD, O	none	-
RX_CTRL	I	PD	6.3	Float	none	-
CLKOUT/GPIO_2	O	none	-	Float	none	-
RX_D3	I	PD/none(2)	9	Float	none	-
RX_D2	I	PD/none(2)	9	Float	none	-
RX_D1	I	PD	9	Float	none	-
RX_D0	I	PD	9	Float	none	-
RX_CLK	I	PD	9	Float	none	-
TX_CLK	I	none	-	Float	none	-
TX_CTRL	I	none	-	Float	none	-
TX_D3	I	none	-	Float	none	-
TX_D2	I	none	-	Float	none	-
TX_D1	I	none	-	Float	none	-
TX_D0	I	none	-	Float	none	-
LED_0	O	none	-	Float	none	-
MDIO	IO	none	-	Float	none	-

(1) Type: I = Input
O = Output
IO = Input/Output
OD = Open Drain
PD = Internal pulldown
PU = Internal pullup
Hi-Z = High Impedence
Float = IO is not powered and hence pin is not biased by the PHY

(2) PD only for Rgmii's isolate mode.

Note

For sleep mode entry vdda, vddio and vdd1p0 are supposed to be powered-down. See figure Required Implementation of Sleep Mode for further details.

5.2 Pin Power Domain

Table 5-5. Pin Power Domain Table

Pin	RGMII Mode	SGMII Mode
MDC	VDDIO	VDDIO
INT_N	VDDIO	VDDIO
RESET_N	VDDIO	VDDIO
XI	VDDA	VDDA
XO	VDDA	VDDA
LED_1	VDDIO	VDDIO
WAKE	VSLEEP	VSLEEP
STRP_1	VDDIO	VDDIO
INH	VSLEEP	VSLEEP
RX_CTRL	VDDIO	VDDIO
CLKOUT/GPIO_2	VDDIO	VDDIO
RX_D3	VDDIO	VDDA
RX_D2	VDDIO	VDDA
RX_D1	VDDIO	VDDIO
RX_D0	VDDIO	VDDIO
RX_CLK	VDDIO	VDDIO
TX_CLK	VDDIO	VDDIO
TX_CTRL	VDDIO	VDDIO
TX_D3	VDDIO	VDDIO
TX_D2	VDDIO	VDDIO
TX_D1	VDDIO	VDDA
TX_D0	VDDIO	VDDA
LED_0	VDDIO	VDDIO
MDIO	VDDIO	VDDIO
TRD_P	VDDA	VDDA
TRD_M	VDDA	VDDA

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	TYP	MAX	UNIT
Supply Voltage	VDDA3P3	-0.5		4	V
Supply Voltage	VDD1P0	-0.5		1.4	V
Supply Voltage	VDDIO (3.3V)	-0.5		4	V
Supply Voltage	VDDIO (2.5V)	-0.5		2.9	V
Supply Voltage	VDDIO (1.8V)	-0.5		2.2	V
Supply Voltage	V_{SLEEP}	-0.5		4	V
MDI Pins	TRD_M, TRD_P	-0.5		4	V
LVCMOS/ LVTTL Input Voltage	MDC, $\overline{RESET}$, XI, LED_1, STRP_1, RX_CTRL, CLKOUT, RX_D[3:0], TX_CLK, TX_CTRL, TX_D[3:0], LED_0, MDIO	-0.5		VDDIO + 0.3	V
LVCMOS/ LVTTL Input Voltage	WAKE	-0.5		V_{SLEEP} + 0.3	V
LVCMOS/ LVTTL Output Voltage	$\overline{INT}$, LED_1, RX_CTRL, CLKOUT, RX_D[3:0], RX_CLK, LED_0, MDIO	-0.5		VDDIO + 0.3	V
LVCMOS/ LVTTL Output Voltage	INH	-0.5		VSLEEP + 0.3	V
T_J	Junction Temperature			150	°C
T_{stg}	Storage temperature	-65		150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)	All pins	±2000	V
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)	TRD_M, TRD_P	±8000	V
$V_{(ESD)}$	Electrostatic discharge	Charged device model (CDM), per AEC Q100-011	All pins	±500	V
$V_{(ESD)}$	Electrostatic discharge	IEC 61000-4-2 contact discharge	TRD_M, TRD_P	±8000	V

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VDDIO	IO Supply Voltage, 1.8V operation	1.62	1.8	1.98	V
	IO Supply Voltage, 2.5V operation	2.25	2.5	2.75	
	IO Supply Voltage, 3.3V operation	2.97	3.3	3.63	
VDDA3P3	Core Supply Voltage, 3.3V	2.97	3.3	3.63	V
VDD1P0	Core Supply Voltage, 1.0V	0.95	1	1.1	V
V_{SLEEP}	Sleep Supply Voltage, 3.3V	2.97	3.3	3.63	V
T_A	Ambient temperature	–40		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		DP83TG720 RHA (VQFN) 36 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	32.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	22.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	13.3	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	13.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	3.2	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics

Over operating free-air temperature range (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DC CHARACTERISTICS						
XI						
V_{IH}	High-level Input Voltage		1.3			V
V_{IL}	Low-level Input Voltage				0.5	V
WAKE pin	WAKE pin	WAKE pin	WAKE pin	WAKE pin	WAKE pin	WAKE pin
V_{IH}	High-level Input Voltage	V_{SLEEP} = 3.3V ± 10%	2			V
V_{IL}	Low-level Input Voltage	V_{SLEEP} = 3.3V ± 10%			0.8	V
INH pin	INH pin	INH pin	INH pin	INH pin	INH pin	INH pin
V_{OH}	High-level Output Voltage	I_{OH} = -2mA, V_{SLEEP} = 3.3V ± 10%	2.4			V
3.3V VDDIO (2)						
V_{OH}	High-level Output Voltage	I_{OH} = -2mA, VDDIO = 3.3V ± 10%	2.4			V
V_{OL}	Low-level Output Voltage	I_{OL} = 2mA, VDDIO = 3.3V ± 10%			0.4	V
V_{IH}	High-level Input Voltage	VDDIO = 3.3V ± 10%	2			V
V_{IL}	Low-level Input Voltage	VDDIO = 3.3V ± 10%			0.8	V
2.5V VDDIO (2)						
V_{OH}	High-level Output Voltage	I_{OH} = -2mA, VDDIO = 2.5V ± 10%	2			V
V_{OL}	Low-level Output Voltage	I_{OL} = 2mA, VDDIO = 2.5V ± 10%			0.4	V
V_{IH}	High-level Input Voltage	VDDIO = 2.5V ± 10%	1.7			V
V_{IL}	Low-level Input Voltage	VDDIO = 2.5V ± 10%			0.7	V

6.5 Electrical Characteristics (continued)

Over operating free-air temperature range (unless otherwise noted)[1]

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
1.8V VDDIO [2]						
V_{OH}	High-level Output Voltage	I_{OH} = -2mA, VDDIO = 1.8V ± 10%	VDDIO – 0.45			V
V_{OL}	Low-level Output Voltage	I_{OL} = 2mA, VDDIO = 1.8V ± 10%			0.45	V
V_{IH}	High-level Input Voltage	VDDIO = 1.8V ± 10%	0.7 * VDDIO			V
V_{IL}	Low-level Input Voltage	VDDIO = 1.8V ± 10%			0.3 * VDDIO	V
I_{IH}	Input High Current (MDIO)	VIN = VCC, -40°C to 125°C	-5		5	µA
I_{IH}	Input High Current (RGMII Input pin,MDC)	VIN = VCC, -40°C to 125°C	-20		20	µA
I_{OZ}	Input High Current (MDIO)	VIN swept from 0V till VCC, -40°C to 125°C	-40		40	µA
I_{IL}	Input Low Current (RGMII Input pin, MDC, MDIO)	VIN = GND, -40°C to 125°C	-40		5	µA
I_{OZL}		INH			6	µA
I_{OZ}	Tri-state Output Current [5]	VIN swept from 0V till VCC, -40°C to 125°C	-40		10	µA
I_{OZ}	Tri-state Output Current [6]	VIN swept from 0V till VCC, -40°C to 125°C	-60		60	µA
C_{IN}	Input Capacitance	LVCMOS/LVTTL pins [3]			2	pF
C_{IN}	Input Capacitance	LVCMOS/LVTTL pins [4]			4	pF
		XI			1	pF
C_{OUT}	Output Capacitance	LVCMOS/LVTTL pins [3]			2	pF
C_{OUT}	Output Capacitance	LVCMOS/LVTTL pins [4]			4	pF
		XO			1	pF
$R_{pull-up}$	Integrated Pull-Up Resistance	$\overline{INT}$, $\overline{RESET}$	6.5	9	12.5	kΩ
$R_{pull-down}$	Integrated Pull-Down Resistance	STRP_1, RX_CTRL	4.725	6.3	7.875	kΩ
$R_{pull-down}$	Integrated Pull-Down Resistance	LED_1, RX_D[3:0], RX_CLK, LED_0	7.3	9	13	kΩ
		WAKE	35	50	62.5	kΩ
$R_{pull-down}$	Integrated Pull-Up Resistance when Active	INH		106		Ω
R_{series}	Integrated MAC Series Termination Resistor (Default)	RX_D[3:0], RX_CTRL, and RX_CLK	24	42	52	Ω
Rseries	Integrated MAC Series Terminatin Resistor (with register<0x0456> = 0x0148)	RX_D[3:0], RX_CTRL, and RX_CLK	30	52	65	Ω
Rseries	Integrated MAC Series Terminatin Resistor (with register<0x0456> = 0x0168)	RX_D[3:0], RX_CTRL, and RX_CLK	40	70	84	Ω
CURRENT CONSUMPTION, SLEEP MODE						
I_{SLEEP}	Sleep Supply Current	V_{SLEEP}		485	840	µA
CURRENT CONSUMPTION, RESET ASSERTED						
I_{DDIO}	IO Supply Current, VDDIO = 1.8V	VDDIO		4	9	mA
I_{DDIO}	IO Supply Current, VDDIO = 2.5V	VDDIO		5	12	mA
I_{DDIO}	IO Supply Current, VDDIO = 3.3V	VDDIO		6.5	15	mA
I_{DDA3P3}	Core Supply Current, 3.3V	VDDA3P3		5	8	mA
I_{DD1P0}	Core Supply Current, 1.0V	VDD1P0		30	110	mA
CURRENT CONSUMPTION, STANDBY						

6.5 Electrical Characteristics (continued)

Over operating free-air temperature range (unless otherwise noted)[1]

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{DDIO}	IO Supply Current, VDDIO = 1.8V	VDDIO		4	11	mA
I_{DDIO}	IO Supply Current, VDDIO = 2.5V	VDDIO		6	13	mA
I_{DDIO}	IO Supply Current, VDDIO = 3.3V	VDDIO		8	15	mA
I_{DDA3P3}	Core Supply Current, 3.3V	VDDA3P3		16	18	mA
I_{DD1P0}	Core Supply Current, 1.0V	VDD1P0		33	112	mA
CURRENT CONSUMPTION, ACTIVE MODE, Voltage: +/- 10%, Traffic : 100%,Packet Size: 1518, Content : Random						
I_{DDIO}	IO Supply Current, VDDIO = 1.8V	RGMII		20	25	mA
I_{DDIO}	IO Supply Current, VDDIO = 2.5V	RGMII		26	30	mA
I_{DDIO}	IO Supply Current, VDDIO = 3.3V	RGMII		33	40	mA
I_{DDIO}	IO Supply Current, VDDIO = 1.8V	SGMII		3.5	5	mA
I_{DDIO}	IO Supply Current, VDDIO = 2.5V	SGMII		5	7	mA
I_{DDIO}	IO Supply Current, VDDIO = 3.3V	SGMII		6.5	8	mA
I_{DDA3P3}	Core Supply Current, 3.3V	RGMII		85	89	mA
I_{DD1P0}	Core Supply Current, 1.0V	RGMII		177	250	mA
I_{DDA3P3}	Core Supply Current, 3.3V	SGMII		95	100	mA
I_{DD1P0}	Core Supply Current, 1.0V	SGMII		200	260	mA
I_{SLEEP}	Sleep Supply Current	$V_{SLEEP = 3.3V +/- 10\%}$		1000	1500	µA
MDI CHARACTERISTICS						
V_{OD-MDI}	Output Differential Voltage	$R_{L(diff)}$ = 100 Ω			1.3	V
$R_{MDI-DIFF}$	Integrated Differential MDI Termination (Active State)	TRD_P, TRD_M		100		Ω
$R_{MDI-DIFF}$	Integrated Differential MDI Termination (Sleep State)	TRD_P, TRD_M		100		Ω
SGMII DRIVER DC SPECIFICATIONS						
$V_{OD-SGMII}$	Output Differential Voltage	$R_{L(diff)}$ = 100 Ω	150		400	mV
$R_{OUT-DIFF}$	Integrated Differential Output Termination	RX_P, RX_M	78	100	130	Ω
SGMII RECEIVER DC SPECIFICATIONS						
V_{IDTH}	Input Differential Threshold		100			mV
$R_{IN-DIFF}$	Integrated Differential Input Termination	TX_P, TX_M	82	100	121	Ω
BOOTSTRAP DC CHARACTERISTICS						
2 level straps						
Vbsl_1v8	Bootstrap Threshold	Mode 1, VDDIO = 1.8V ± 10%, 2-level	0		0.35*VDDIO	V
Vbsh_1v8	Bootstrap Threshold	Mode 2, VDDIO = 1.8V ± 10%, 2-level	1.175		VDDIO	V
Vbsl_2v5	Bootstrap Threshold	Mode 1, VDDIO = 2.5V ± 10%, 2-level	0		0.7	V
Vbsh_2v5	Bootstrap Threshold	Mode 2, VDDIO = 2.5V ± 10%, 2-level	1.175		VDDIO	V
Vbsl_3v3	Bootstrap Threshold	Mode 1, VDDIO = 3.3V ± 10%, 2-level	0		0.7	V
Vbsh_3v3	Bootstrap Threshold	Mode 2, VDDIO = 3.3V ± 10%, 2-level	1.175		VDDIO	V
3 level straps						
V_{bs1_1V8}	Bootstrap Threshold	Mode 1, VDDIO = 1.8V ± 10%, 3-level	0		0.35 * VDDIO	V

6.5 Electrical Characteristics (continued)

Over operating free-air temperature range (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{bs2_1V8}	Bootstrap Threshold	Mode 2, VDDIO = 1.8V ± 10%, 3-level	0.40 * VDDIO		0.75 * VDDIO	V
V_{bs3_1V8}	Bootstrap Threshold	Mode 3, VDDIO = 1.8V ± 10%, 3-level	0.84 * VDDIO		VDDIO	V
V_{bs1_2V5}	Bootstrap Threshold	Mode 1, VDDIO = 2.5V ± 10%, 3-level	0		0.19 * VDDIO	V
V_{bs2_2V5}	Bootstrap Threshold	Mode 2, VDDIO = 2.5V ± 10%, 3-level	0.27 * VDDIO		0.41 * VDDIO	V
V_{bs3_2V5}	Bootstrap Threshold	Mode 3, VDDIO = 2.5V ± 10%, 3-level	0.58 * VDDIO		VDDIO	V
V_{bs1_3V3}	Bootstrap Threshold	Mode 1, VDDIO = 3.3V ± 10%, 3-level	0		0.18 * VDDIO	V
V_{bs2_3V3}	Bootstrap Threshold	Mode 2, VDDIO = 3.3V ± 10%, 3-level	0.22 * VDDIO		0.42 * VDDIO	V
V_{bs3_3V3}	Bootstrap Threshold	Mode 3, VDDIO = 3.3V ± 10%, 3-level	0.46 * VDDIO		VDDIO	V
Temperature Sensor						
	Temperature Sensor Resolution (LSB)	-40℃ to 125℃		1.5		℃
	Temperature Sensor Accuracy (Voltage and Temperature Variation on single part)	-40℃ to 125℃	-7.5		7.5	℃
	Temperature Sensor Accuracy (Voltage, Temperature and Part-to-Part variation)	-40℃ to 125℃	-21.5		20	℃
	Temperature Sensor Range		-40		140	℃
Voltage Sensor						
	VDDA3P3 Sensor Range		2.66	3.3	3.96	V
	VDDA3P3 Sensor Resolution (LSB)	-40℃ to 125℃		8.6		mV
	VDDA3P3 Sensor Accuracy (Voltage and Temperature Variation)	-40℃ to 125℃		8.6		mV
	VDDA3P3 Sensor Accuracy Part-to-Part	-40℃ to 125℃	-68.8		68.8	mV
	VDD1P0 Sensor Range		0.8		1.2	V
	VDD1P0 Sensor Resolution (LSB)	-40℃ to 125℃		2.8		mV
	VDD1P0 Sensor Accuracy (Voltage and Temperature Variation)	-40℃ to 125℃		2.8		mV
	VDD1P0 Sensor Accuracy Part-to-Part	-40℃ to 125℃	-22.4		22.4	mV
	VDDIO Sensor Range		1.44		3.8	V
	VDDIO Sensor Resolution (LSB)	-40℃ to 125℃		15.4		mV
	VDDIO Sensor Accuracy (Voltage and Temperature Variation)	-40℃ to 125℃		15.4		mV
	VDDIO Sensor Accuracy Part-to-Part	-40℃ to 125℃	-78		78	mV

(1) Ensured by production test, characterization or design
(2) For pins: LED_1, STRP_1, RX_CTRL, CLKOUT, RX_D[3:0], RX_CLK, LED_0
(3) For pins: MDC, INT, RESET, LED_1, STRP_1, RX_CTRL, CLKOUT, RX_D0, RX_D1, RX_CLK, TX_CLK, TX_CTRL, TX_D2, TX_D3, LED_0, and MDIO
(4) For pins: TX_D0, TX_D1, RX_D2, and RX_D3
(5) For pins : LED_1, RX_D[3:0], RX_CLK, LED_0
(6) For pins : STRP_1 and RX_CTRL

6.6 Timing Requirements

(1)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
POWER-UP TIMING						
T5.1	VDDA3P3 Duration(2)	0% to 100% (+/- 10 VDDA3P3)	0.5		40	ms
T5.2	VDD1P0 Duration(2)	0% to 100% (+/- 10 VDD1P0)	0.1		40	ms
T5.2	VDDIO Duration(2)	VDDIO = 1.8V	0.1		40	ms
T5.2	VDDIO Duration(2)	VDDIO = 2.5V	0.1		40	ms
T5.2	VDDIO Duration(2)	VDDIO = 3.3V	0.1		40	ms
T5.2	$V_{SLEEP\ Duration}$ (2)	0% to 100% (+/- 10 V_{SLEEP})	0.1		40	ms
T5.3	Crystal stabilization-time post power-up (from last power rail ramp to 100%)			1500		µs
T5.4	Osillator stabilization-time post power-up (from last power rail ramp to 100%)(3)				20	ms
T5.5	Post power-up stabilization-time prior to MDC preamble for register access		65			ms
T5.6	Hardware configuration latch-in time from power-up				60	ms
T5.7	Hardware configuration pins transition to functional mode from latch-in completion				110	ns
T5.8	PAM3 IDLE Stream from power-up (Master Mode)				60	ms
RESET TIMING (RESET_N)						
T6.1	RESET pulse width		5			µs
T6.2	Post reset stabilization-time prior to MDC preamble for register access		1			ms
T6.3	Hardware configuration latch-in time from reset				2	µs
T6.4	Hardware configuration pins transition to functional mode from latch-in completion				1.5	µs
T6.5	PAM3 IDLE Stream from reset (Master Mode)				1500	µs
SMI TIMING						
T4.1	MDC to MDIO (Output) Delay Time (25 pF load)		0	6	10	ns
T4.2	MDIO (Input) to MDC Setup Time		10			ns
T4.3	MDIO (Input) to MDC Hold Time		10			ns
	MDC Frequency (25 pF load)			2.5	20	MHz
RECEIVE LATENCY TIMING						
	SSD symbol on MDI to Rising edge of RGMII RX_CLK with assertion of RX_CTRL				8	µs
	SSD symbol on MDI to Rising edge of RGMII RX_CLK with assertion of RX_CTRL (RS-FEC bypass mode)				400	ns
	SSD symbol on MDI to first symbol of SGMII				9	µs
	SSD symbol on MDI to first symbol of SGMII (RS-FEC bypass mode)				450	ns
TRANSMIT LATENCY TIMING						
	RGMII Rising edge TX_CLK with assertion TX_CTRL to SSD symbol on MDI				0.8	µs
	RGMII Rising edge TX_CLK with assertion TX_CTRL to SSD symbol on MDI (RS-FEC bypass mode)				600	ns
	First symbol of SGMII to SSD symbol on MDI				0.9	µs

6.6 Timing Requirements (continued)

(1)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
	First symbol of SGMII to SSD symbol on MDI (RS-FEC bypass mode)				700	ns
25 MHz OSCILLATOR REQUIREMENTS						
	Frequency (XI)			25		MHz
	Frequency Tolerance and Stability Over temperature and aging		–100		100	ppm
	Rise / Fall Time (10% - 90%)(6)				8	ns
	Jitter (RMS)	Integrated upto 5MHz			1	ps
	Duty Cycle		40	50	60	%
RGMII TIMING						
T_{setupR}	TX_D[3:0], TX_CTRL Setup to TX_CLK	on PHY pins	1	2		ns
T_{holdR}	TX_D[3:0], TX_CTRL Hold from TX_CLK (5)	on PHY pins	1	2		ns
T_{skewT}	RX_D[3:0], RX_CTRL Delay from RX_CLK (Align Mode Enabled)	On PHY Pins	-500	0	500	ps
T_{skewT} (Shift)	RX_D[3:0], RX_CTRL Delay from RX_CLK (Shift Mode Enabled, default)(4)	On PHY Pins	2.190	2.650	2.970	ns
T_{cyc}	Clock Cycle Duration	RX_CLK	7.2	8	8.8	ns
T_{cyc}	Clock Cycle Duration	TX_CLK	7.2	8	8.8	ns
Duty_G	Duty Cycle	RX_CLK	45	50	55	%
Duty_G	Duty Cycle	TX_CLK	45	50	55	%
Tr	Rise Time (20% - 80%)	CL=Ctrace=5pF			0.75	ns
Tf	Fall Time (20% - 80%)	$C_{L=Ctrace}$ = 5pF			0.75	ns
RGMII RX Shift Mode Delays	DLL DLL_RX_DELAY_CTRL_SL=0(4)		0.330	0.650	0.970	ns
	DLL DLL_RX_DELAY_CTRL_SL=1(4)		0.580	0.900	1.220	ns
	DLL DLL_RX_DELAY_CTRL_SL=2(4)		0.830	1.150	1470	ns
	DLL DLL_RX_DELAY_CTRL_SL=3(4)		1.000	1.400	1.720	ns
	DLL DLL_RX_DELAY_CTRL_SL=4(4)		1.230	1.650	1.970	ns
	DLL DLL_RX_DELAY_CTRL_SL=5(4)		1.490	1.990	2.220	ns
	DLL DLL_RX_DELAY_CTRL_SL=6(4)		1.690	2.150	2.470	ns
	DLL DLL_RX_DELAY_CTRL_SL=7(4)		1.960	2.400	2.730	ns
	DLL DLL_RX_DELAY_CTRL_SL=8(4)		2.180	2.650	2.970	ns
	DLL DLL_RX_DELAY_CTRL_SL=9(4)		2.490	2.900	3.220	ns
RGMII Shift TX Mode Delays						
	DLL DLL_TX_DELAY_CTRL_SL=1(4) (8)		0.08	0.25	0.38	ns
	DLL DLL_TX_DELAY_CTRL_SL=2(4) (8)		0.27	0.49	0.67	ns
	DLL DLL_TX_DELAY_CTRL_SL=3(4) (8)		0.51	0.73	0.91	ns
	DLL DLL_TX_DELAY_CTRL_SL=4(4) (8)		0.75	0.97	1.15	ns
	DLL DLL_TX_DELAY_CTRL_SL=5(4) (8)		0.94	1.21	1.44	ns
	DLL DLL_TX_DELAY_CTRL_SL=6(4) (8)		1.18	1.45	1.68	ns
	DLL DLL_TX_DELAY_CTRL_SL=7(4) (8)		1.37	1.69	1.98	ns
	DLL DLL_TX_DELAY_CTRL_SL=8(4) (8)		1.61	1.93	2.22	ns

6.6 Timing Requirements (continued)

(1)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
	DLL DLL_TX_DELAY_CTRL_SL=9(4) (8)		1.85	2.17	2.46	ns
	DLL DLL_TX_DELAY_CTRL_SL=10(4) (8)		2.04	2.42	2.75	ns
	DLL DLL_TX_DELAY_CTRL_SL=11(4) (8)		2.28	2.65	2.99	ns
	DLL DLL_TX_DELAY_CTRL_SL=12(4) (8)		2.52	2.9	3.23	ns
SGMII TRANSMITTER AC TIMING						
	Clock signal duty cycle at 625 MHz		48		52	%
T_{rise}	Vod Rise Time		100		200	ps
T_{fall}	Vod Fall Time		100		200	ps
Jitter	Output jitter			200	320 (7)	ps
25 MHz CRYSTAL REQUIREMENTS						
	Frequency			25		MHz
	Frequency Tolerance and Stability Over temperature and aging		–100		100	ppm
	Equivalent Series Resistance				100	Ω
OUTPUT CLOCK TIMING (CLKOUT)						
	Frequency			25		MHz
	Duty Cycle (With crystal attached)		45		55	%
	Rise / Fall Time (10% - 90%)				2.5	ns
	Jitter (RMS) (Slave Mode, MAC Iinterface : SGMII)				5	ps
	Jitter (RMS) (Master Mode, MAC Iinterface : SGMII)				2.4	ps
	Jitter (RMS) (Slave Mode, MAC Interface : RGMII)				11	ps
	Jitter (RMS) (Master Mode, MAC Interface : RGMII)				15	ps
Sleep Entry and Wake-Up						
	WAKE LOW to Sleep Entry; INH Transition LOW	Normal Mode, MDI_Energy = FALSE sleep_en = TRUE		64	85	us
	sleep_en = True to Sleep Entry; INH Transition LOW (master mode)	Normal Mode, WAKE = LOW, MDI_Energy = FALSE		5	85	us
	sleep_en = True to Sleep Entry; INH Transition LOW (slave mode)	Normal Mode, WAKE = LOW, MDI_Energy = FALSE			5000	us
	MDI Energy Loss to Sleep Entry; INH Transition LOW	Normal Mode, WAKE = LOW, sleep_en = TRUE			5	ms
	Local Wake-Up Pulse Duration (on Wake pin)	Sleep Mode, WAKE pin	80			µs
	Send-S/Send-T pattern duration for wake up from MDI	Sleep Mode, Slave	1.25			ms
	Local Wake-Up; INH Transition HIGH	Sleep Mode, rising edge of WAKE pin to rising edge of INH			85	us
	Tolerable differential noise level on MDI for PHY to stay in sleep mode	Sleep Mode			200	mV pk-pk
	Link-partner's VOD for valid wake-up (for 5m cable)	Sleep Mode	840			mV pk-pk

(1) Ensured by production test or characterization or design.
(2) No supply sequencing constraint across power rails

(3) In case OSC clock is delayed, additional reset is needed post Osc clock stablisation
(4) Refer register[0x0430] for programmability of RX and TX delay codes
(5) PHY provides internal delays on TX_CLK to TX_D[3:0] to add additional skew upto 2 ns. Refer to register[0x0430] for programmability
(6) Max rise/fall time of 8ns is supported for duty cycle of 40% to 55%. Max rise/fall time will be 6 ns for duty cycle of 40% to 60%
(7) Additional register configuration available to reduce this max number to 300ps (if required)
(8) Data for 1.8V VDDIO.

6.7 Timing Diagrams

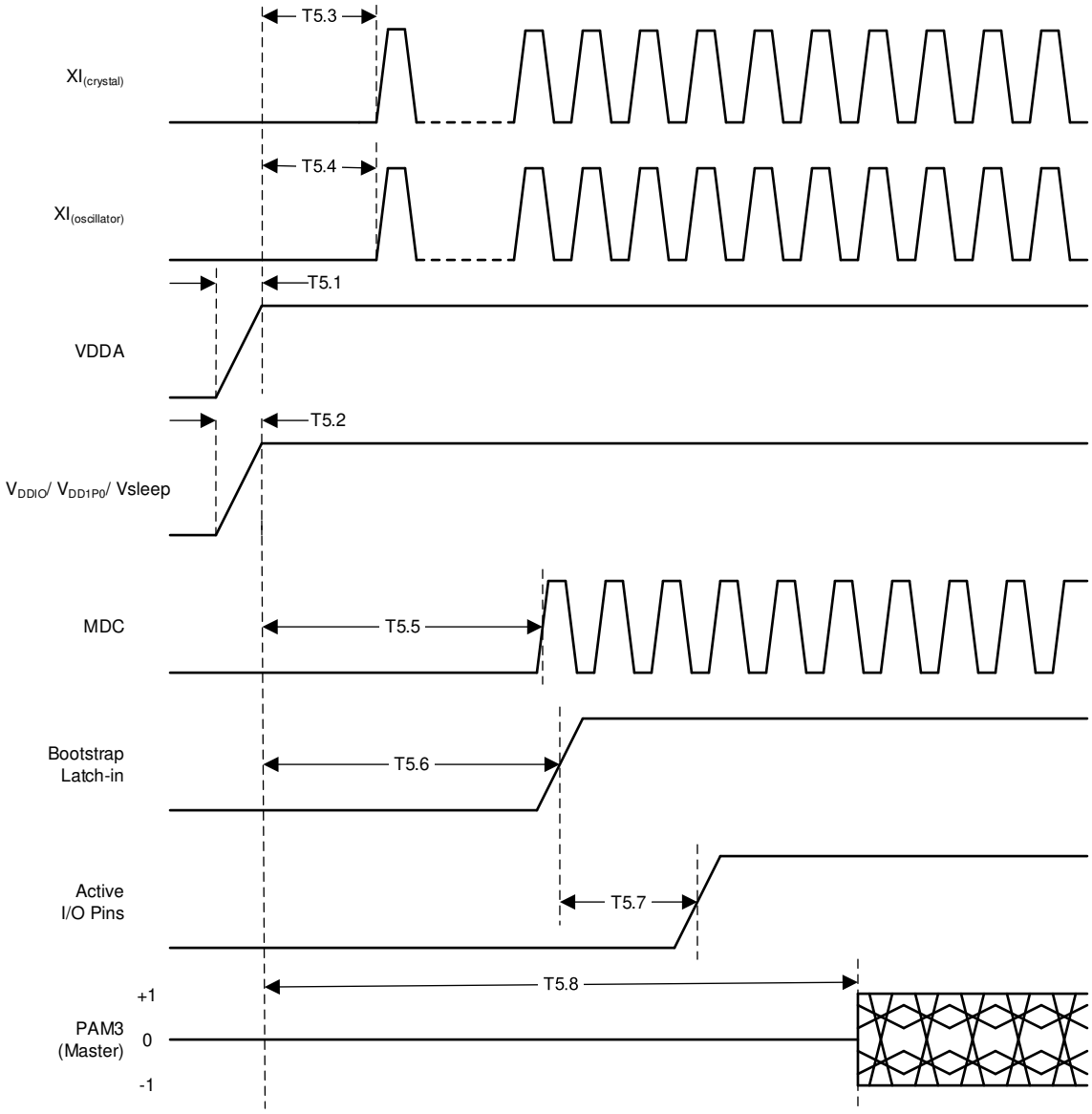

Figure 6-1. Power Up Timing

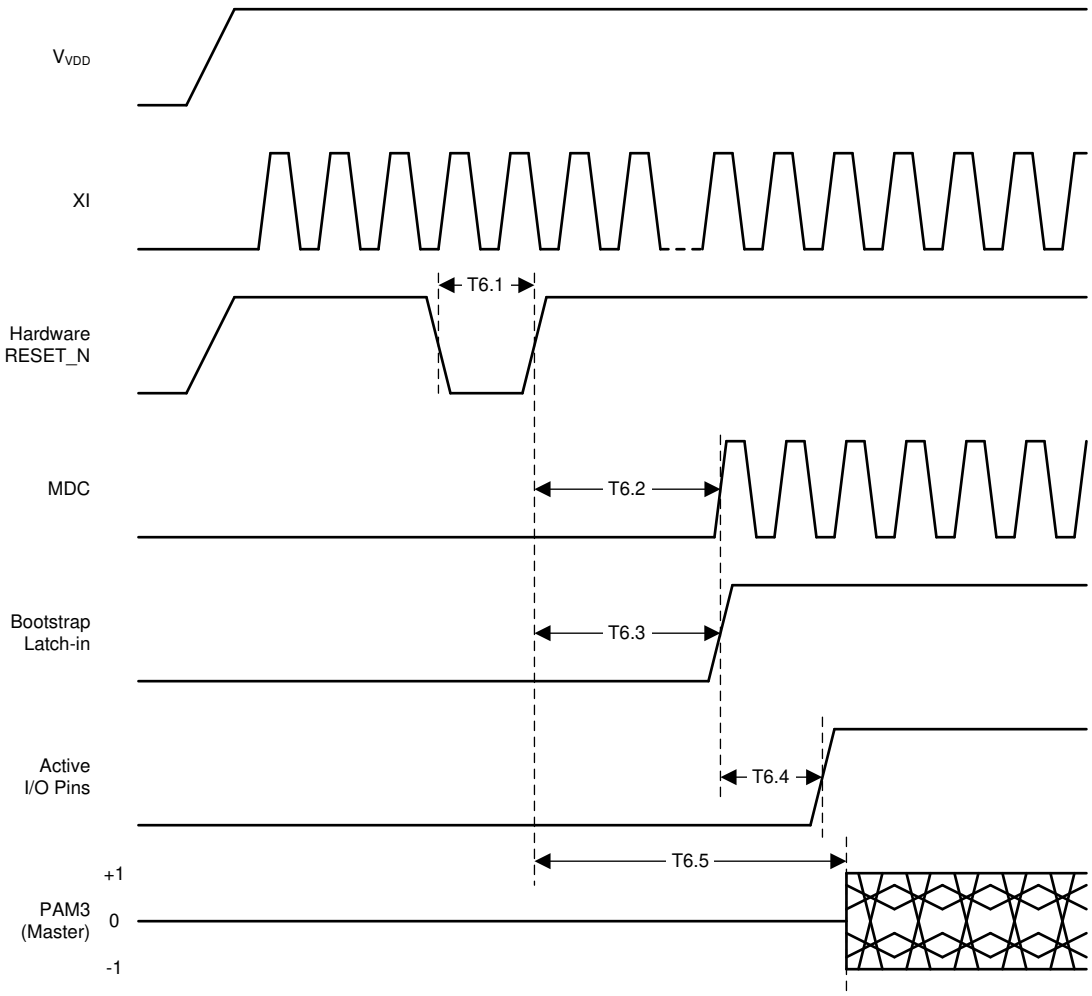

Figure 6-2. Reset Timing

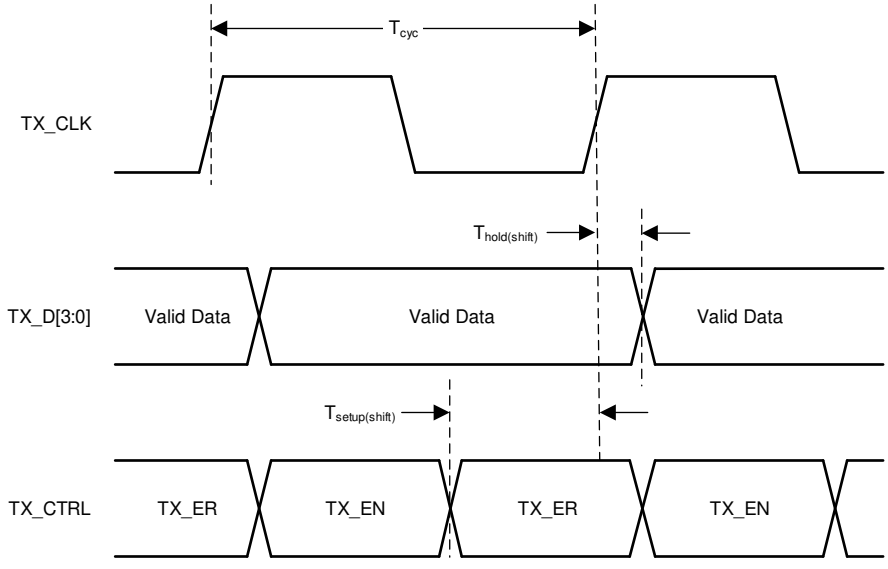

Figure 6-3. RGMII Transmit Timing (Internal Delay Enabled)

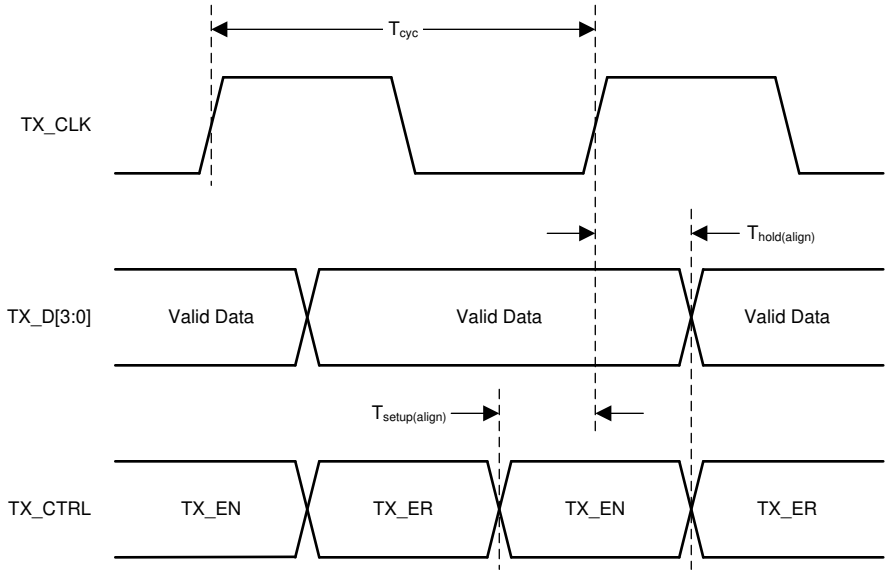

Figure 6-4. RGMII Transmit Timing (Internal Delay Disabled)

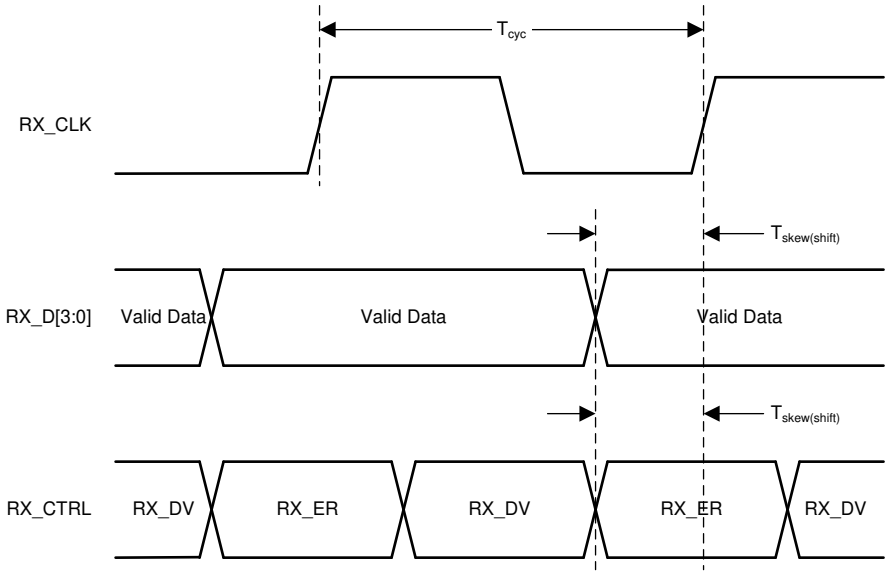

Figure 6-5. RGMII Receive Timing (Internal Delay Enabled)

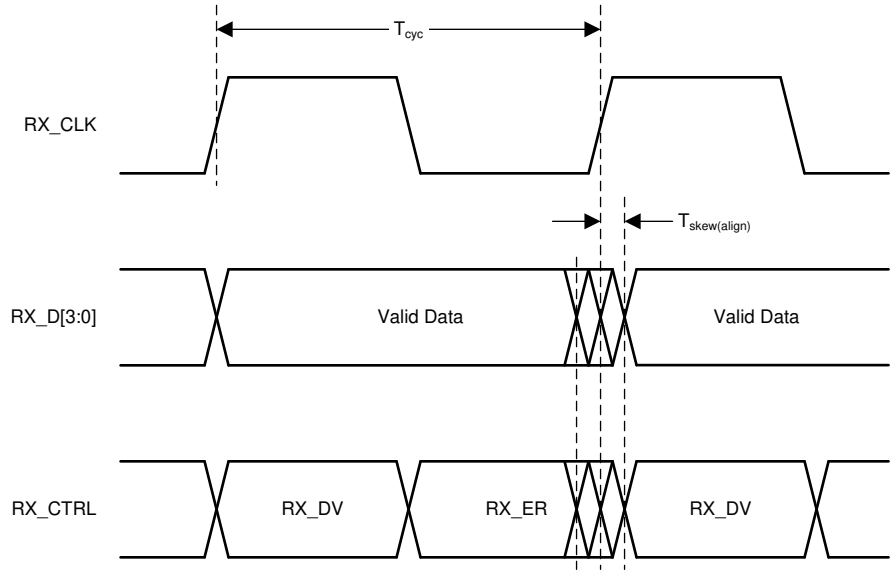

Figure 6-6. RGMII Receive Timing (Internal Delay Disabled)

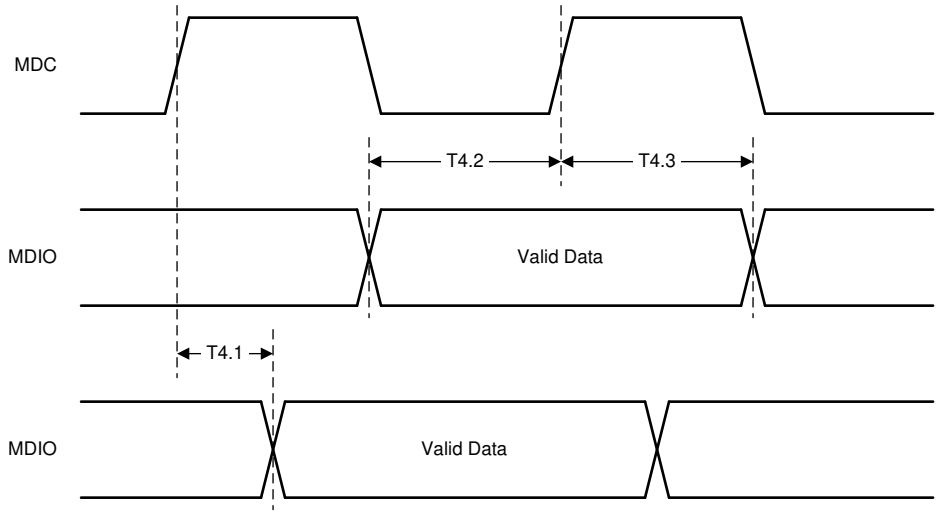

Figure 6-7. Serial Management Timing

6.8 LED Drive Characteristics

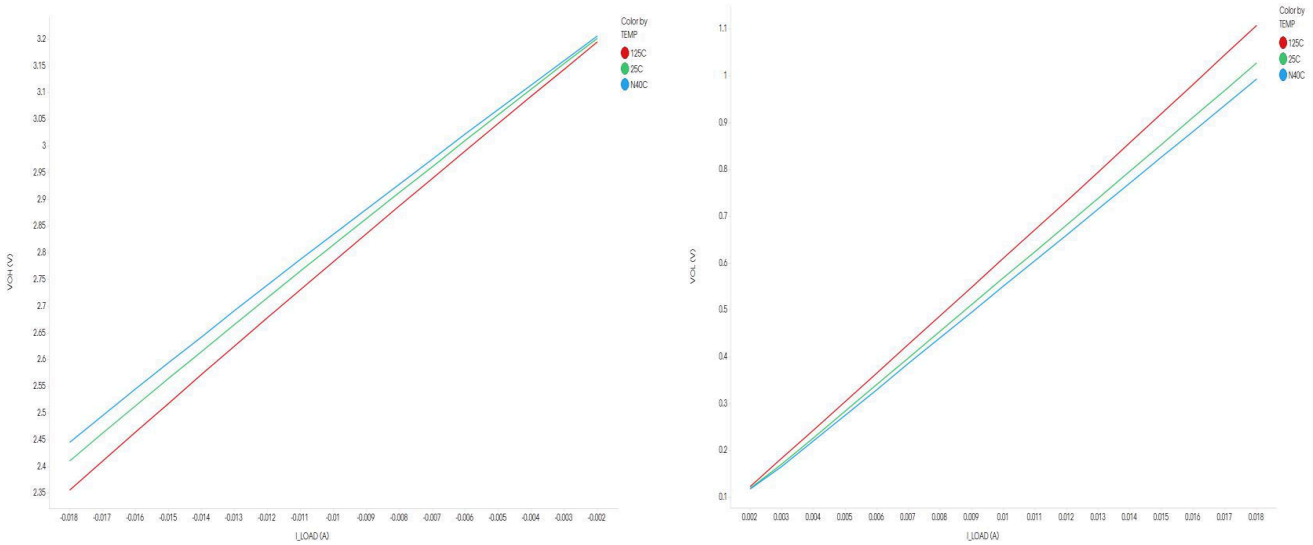

Figure 6-8. LED V vs I for 3.3V VDDIO

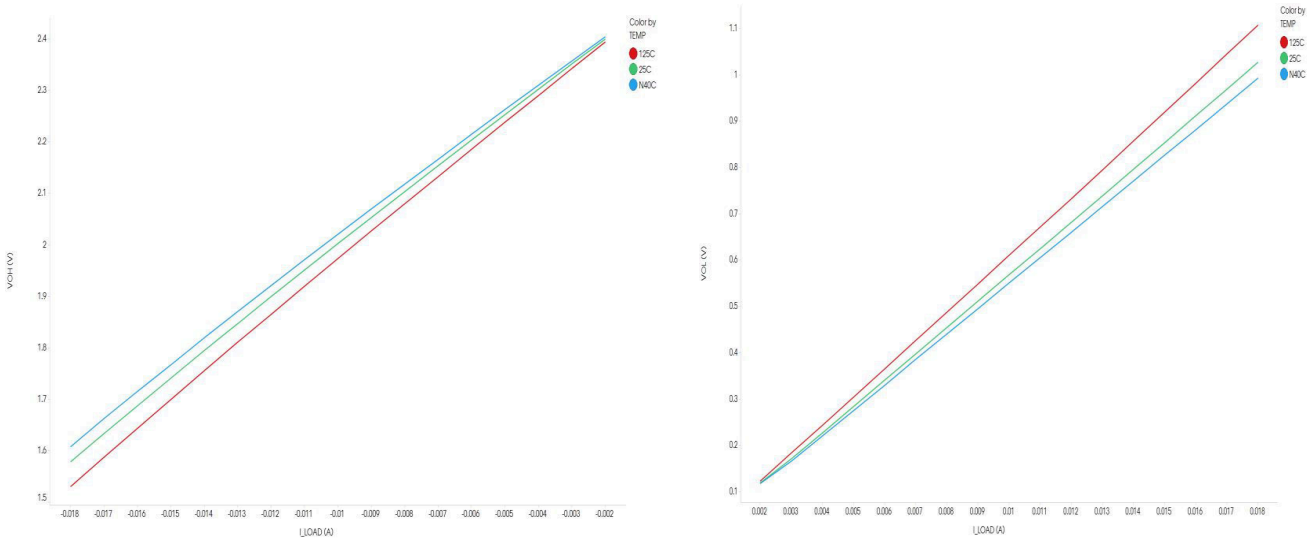

Figure 6-9. LED V vs I for 2.5V VDDIO

7 Detailed Description

7.1 Overview

The DP83TG720S-Q1 is a 1000BASE-T1 automotive Ethernet Physical Layer transceiver. It is IEEE 802.3bp compliant and AEC-Q100 qualified for automotive applications.

This device is specifically designed to operate at 1-Gbps speed while meeting stringent automotive EMC requirements. The DP83TG720S-Q1 transmits PAM3 ternary symbols at 750-MBd over unshielded/shielded single-twisted pair cable. It is designed for RGMII or SGMII support in a single 36-pin VQFN wettable flank package.

7.2 Functional Block Diagram

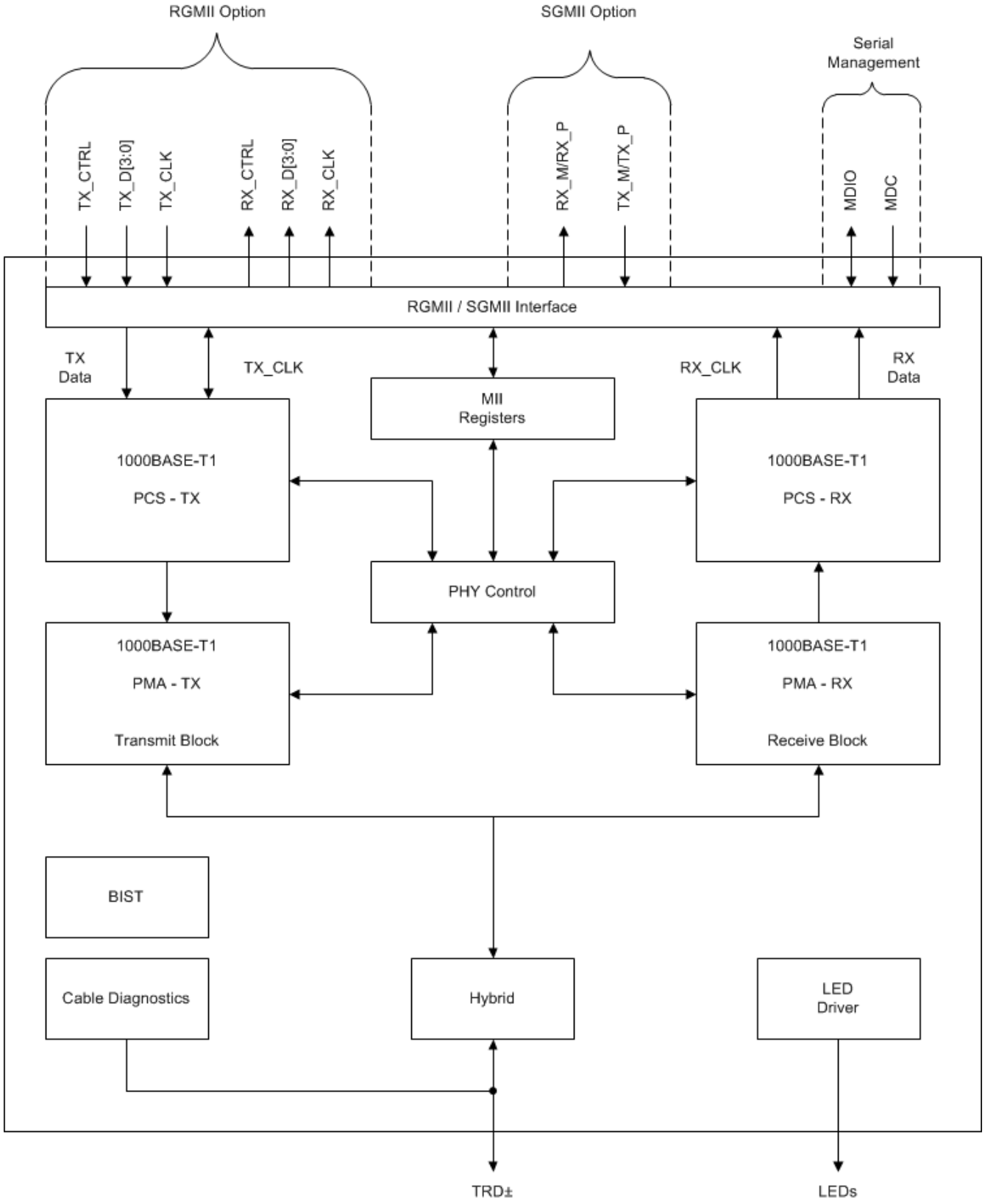

Figure 7-1. DP83TG720S-Q1 Functional Block Diagram

7.3 Feature Description

7.3.1 Diagnostic Tool Kit

The DP83TG720S-Q1 diagnostic tool kit provides mechanisms for monitoring normal operation, device-level debugging, system-level debugging, fault detection, and compliance testing. This tool kit includes a built-in self-test with PRBS data, various loopback modes, Signal Quality Indicator (SQI), Time Domain Reflectometry (TDR), voltage monitor, temperature monitor, electrostatic discharge monitor, and IEEE 802.3bp test modes.

7.3.1.1 Signal Quality Indicator

When the DP83TG720S-Q1 is active, the Signal Quality Indicator may be used to determine the quality of link based on SNR readings made by the device.

SQI is derived based on the calculated SNR value and is presented as 8 level indication, where level of 5 ensures a BER better than 10^{-10}.

Note

Refer to *DP83TG720: Configuring for Open Alliance Specification Compliance* application note for details on using SQI register for Open Alliance TC12 SQI tests.

7.3.1.2 Time Domain Reflectometry

Time domain reflectometry helps detecting and estimating the location of OPEN and SHORT faults along a cable.

TDR is activated by setting bit[15] = 'b1 in the register[0x001E]. When TDR diagnostic process gets completed successfully, Bit[1:0] of register[0x001E] will become 'b10. After this status change, TDR results can be read in the register of following table.

Table 7-1. TDR Result Registers : 0x030F

Register Bits	Description
[1:0]	• 01 = TDR Activation • 10 = TDR On • 00,11 = TDR Not Available
[3:2]	Reserved
[7:4]	• 0011 = Short • 0110 = Open • 0101 = Noise • 0111 = Cable OK • 1000 = Test in progress; initial value with TDR ON • 1101 = Test not possible (for example, noise, active link) • Other values are not valid
[13:8]	• Fault distance = Value in decimal of [13:8] • 'b111111 = Resolution not possible/out of distance
[15:14]	Reserved

Note

TDR should not be run if the link is already active. Running TDR on active line can make TDR fail and also can result in disruption of link.

Refer to *DP83TG720: Configuring for Open Alliance Specification Compliance* application note for detailed procedure of running TDR.

7.3.1.3 Built-In Self-Test For Datapath

The DP83TG720S-Q1 incorporates a data-path's Built-In-Self-Test (BIST) to check the PHY level and system level data-paths. BIST has following integrated features which make the system level data transfer tests (through-put etc) and diagnostics possible without relying on MAC or external data generator hardware/software.

1. Loopback modes
2. Data generator
   a. Customizable MAC packets generator.
   b. Transmitted packet counter.
   c. PRBS stream generator.
3. Data checker
   a. Received MAC packets error checker.
   b. Received packet counter: Counts total packets received and packets received with errors.
   c. PRBS lock and PRBS error checker.

7.3.1.3.1 Loopback Modes

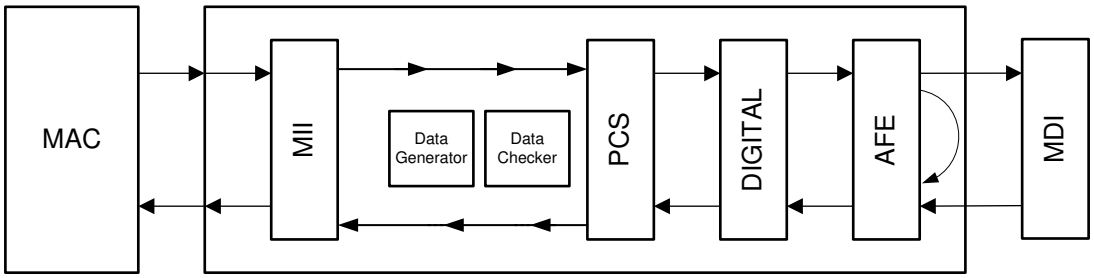

Figure 7-2. All Loopbacks

There are several loopback options within the DP83TG720S-Q1. Enabling different loopback modes enables/ bypass different data-paths according to system verification requirements. Different loopbacks can be enabled along-side following data generation options :

a. Inbuilt data-generator

b. External data-generator (on Ethernet cable or MAC side)

Following diagrams illustrate data-flow during different loopback options :

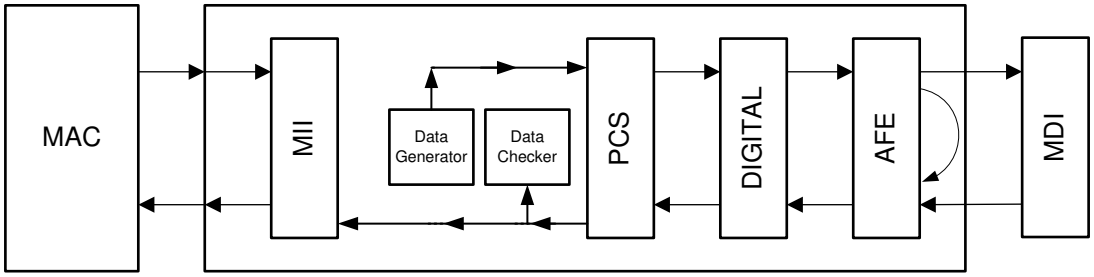

Figure 7-3. Analog Loopback With Inbuilt Data-Gen

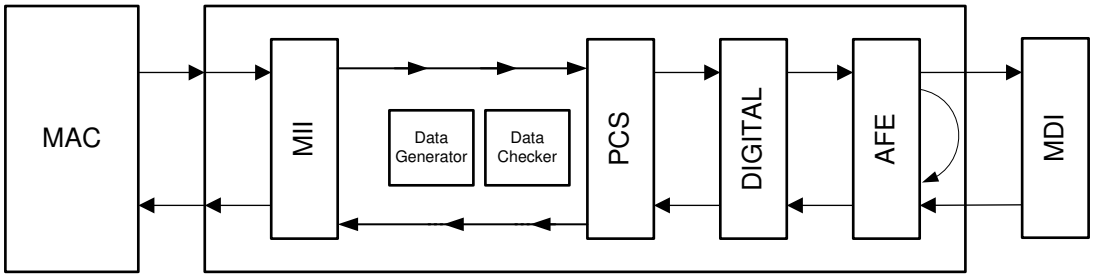

Figure 7-4. Analog Loopback With External Data-Gen

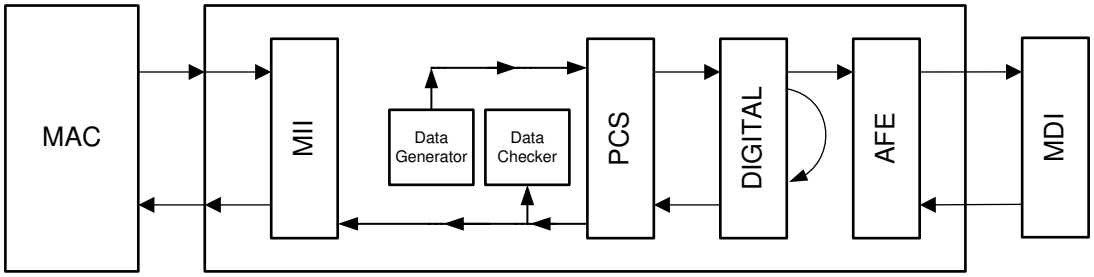

Figure 7-5. Digital Loopback With Inbuilt Data-Gen

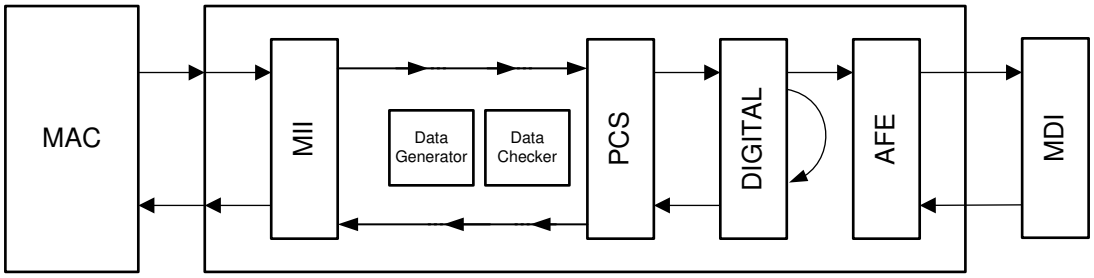

Figure 7-6. Digital Loopback With External Data-Gen

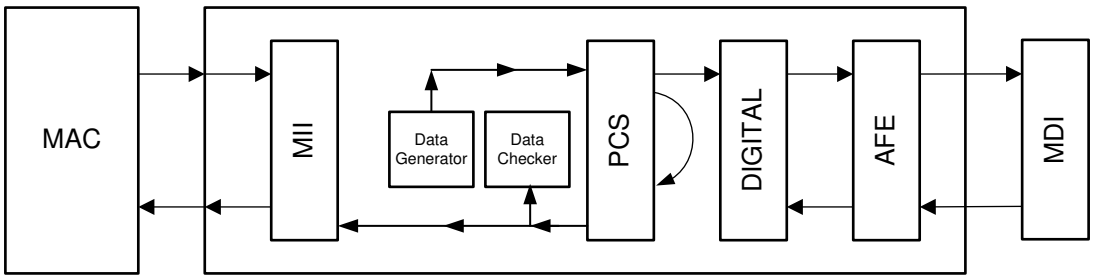

Figure 7-7. PCS Loopback With Inbuilt Data-Gen

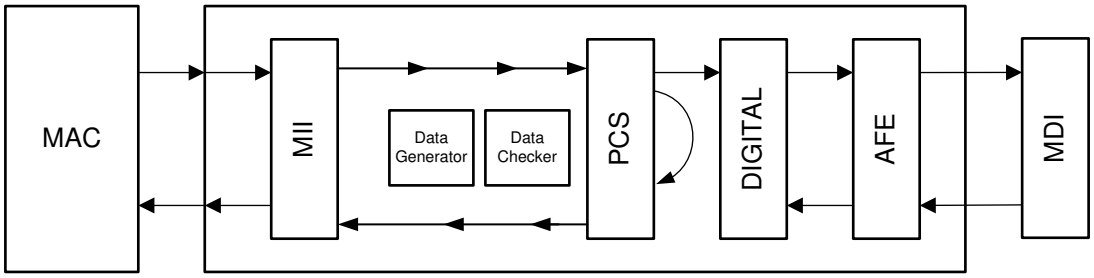

Figure 7-8. PCS Loopback With External Data-Gen

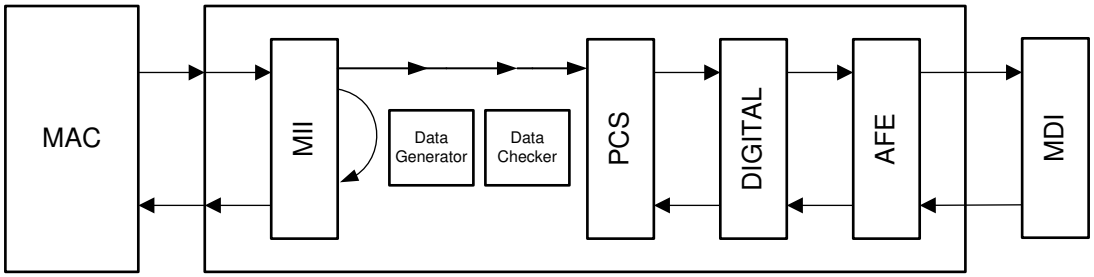

Figure 7-9. xMII Loopback With External Data-Gen

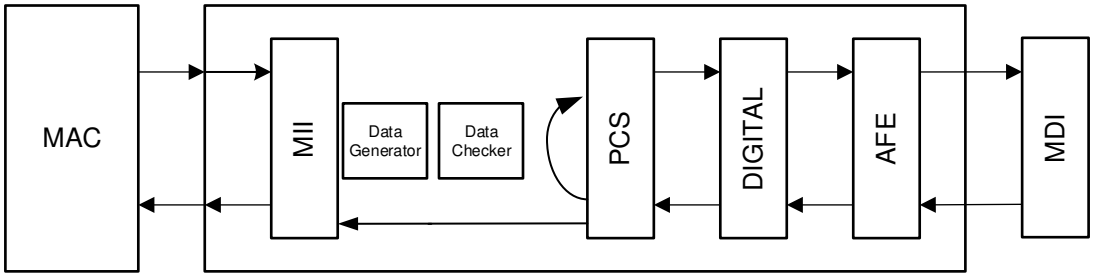

Figure 7-10. xMII Reverse Loopback With External Data-Gen

7.3.1.3.2 Data Generator

Data generator can be programmed to generate either user defined MAC packets or PRBS stream.

Following parameters of generated MAC packets can be configured (refer to registers<0x061B>,register<0x061A> and register<0x0624> for required configuration):

- Packet Length
- Inter-packet gap
- Defined number of packets to be sent or continuous transmission
- Packet data-type: Incremental/Fixed/PRBS
- Number of valid bytes per packet

7.3.1.3.3 Programming Datapath BIST

The following register settings enable different loopbacks, data generation and data checker procedures.

Table 7-2. Datapath BIST Programming

	Loopback Mode	To enable loopback mode	To enable data generator and checker: MAC packets	To check in-coming MAC packets status	To enable data generator and checker: PRBS stream	To check in-coming PRBS status: PRBS stream	Other care-abouts
1	Analog loopback	write : reg[0x0016]=0x0108 write : reg[0x0405]=0x2800	write : reg[0x0619]=0x1555 write : reg[0x0624]=0x55BF	read : reg[0x063C] for (15:0) of total received packets count. read : reg[0x063D] for (31:16) of total received packets count. read : reg[0x063E] for Packets received with CRC errors	write : reg[0x0619]= 0x0557 write : reg[0x0624]= 0x55BF	Step 1: write : reg[0x0620](1) = 1'b1 Step 2 : read : reg[0x0620] (7:0) = Number of error bytes received. read : reg[0x0620] (8) (1 indicates PRBS data is coming in and checker is locked)	Disconnect the cable/link-partner. Generated data will be going to MAC side, to disable MAC side : write : reg[0x0000]=0x0540
2	Digital loopback	write : reg[0x0016] = 0x0104 write : reg[0x0800] [11]=1	write : reg[0x0619]=0x1555 write : reg[0x0624]=0x55BF	read : reg[0x063C] = [15:0] of total received packets count. read : reg[0x063D]= [31:16] of total received packets count. read : reg<0x063E> -> Packets received with CRC errors	write : reg[0x0619]= 0x0557 write : reg[0x0624]= 0x55BF	Step 1 : write : reg[0x0620][1] = 1'b1 Step 2 : read : reg[0x0620] [7:0] = Number of error bytes received. read : reg[0x0620] [8] (1 indicates PRBS data is coming in and checker is locked)	Generated data will be going to Cu cable side, to disable this transmission : write : reg[0x041F] = 0x1000 Generated data will be going to MAC side, to disable MAC side : write : reg[0x0000]=0x0540
3	PCS loopback	write : reg<0x0016> = 0x0101	write : reg[0x0619]=0x1555 write : reg[0x0624]=0x55BF	read : reg[0x063C]= [15:0] of total received packets count. read : reg[0x063D]= [31:16] of total received packets count. read : reg[0x063E]= Packets received with CRC errors	write : reg[0x0619]= 0x0557 write : reg[0x0624]= 0x55BF	Step 1 : write : reg[0x0620][1] = 1'b1 Step 2 : read : reg[0x0620] [7:0] = Number of error bytes received. read : reg[0x0620] [8] (1 indicates PRBS data is coming in and checker is locked)	Generated data will be going to Cu cable side, to disable this transmission : write : reg[0x041F] = 0x1000 Generated data will be going to MAC side, to disable MAC side : write : reg[0x0000]=0x0540

Table 7-2. Datapath BIST Programming (continued)

	Loopback Mode	To enable loopback mode	To enable data generator and checker: MAC packets	To check in-coming MAC packets status	To enable data generator and checker: PRBS stream	To check in-coming PRBS status: PRBS stream	Other care-abouts
4	RGMII loopback	write : reg<0x0000> = 0x4140	Data is generated externally at Rgmii TX pins Write : reg[0x0619]= 0x1004	Data can be verified at Rgmii RX pins. Packet errors can additionaly be checked internally by : read : reg[0x063C]= [15:0] of total received packets count. read : reg[0x063D] = [31:16] of total received packets count. read : reg[0x063E]= Packets received with CRC errors	Data is generated externally at Rgmii Tx pins.	Not applicable as data is external. PRBS stream checker works only with internal data generator.	Generated data will be going to Cu cable side, to disable this transmission : write : reg[0x041F] = 0x1000
5	SGMII loopback	write : reg[0x0000] = 0x4140	Data is generated externally at Sgmii TX pins Write : reg[0x0619] = 0x1114	Data can be verified at Sgmii RX pins. Packet errors can additionaly be checked internally by : read : reg[0x063C]= [15:0] of total received packets count. read : reg[0x063D] = [31:16] of total received packets count. read : reg[0x063E] = Packets received with CRC errors	Data is generated externally at Sgmii Tx pins.	Not applicable as data is external. PRBS stream checker works only with internal data generator.	Generated data will be going to Cu cable side, to disable this transmission : write : reg[0x041F] = 0x1000
6	RGMII Reverse loopback	write : reg[0x0016] = 0x0010	write : reg[0x0619]=0x1005 write : reg[0x0624]=0x55BF	read : reg[0x063C] = [15:0] of total received packets count. read : reg[0x063D] = [31:16] of total received packets count. read : reg[0x063E] = Packets received with CRC errors	write : reg[0x0619]= 0x0557 write : reg[0x0624]= 0x55BF	Step 1 : write : reg[0x0620][1] = 1'b1 Step 2 : read : reg[0x0620] [7:0] = Number of error bytes received. read : reg[0x0620] [8] (1 indicates PRBS data is coming in and checker is locked)	Generated data will be going to Cu cable side, to disable this transmission : write : reg[0x041F] = 0x1000

Table 7-2. Datapath BIST Programming (continued)

	Loopback Mode	To enable loopback mode	To enable data generator and checker: MAC packets	To check in-coming MAC packets status	To enable data generator and checker: PRBS stream	To check in-coming PRBS status: PRBS stream	Other care-abouts
7	SGMII Reverse loopback	write : reg[0x042C] = 0x0010	write : reg[0x0619]=0x1115 write : reg[0x0624]=0x55BF	read : reg[0x063C] for [15:0] of total received packets count. read : reg[0x063D] for [31:16] of total received packets count. read : reg[0x063E] for Packets received with CRC errors	write : reg[0x0619]= 0x0557 write : reg[0x0624]= 0x55BF	Step 1 : write : reg[0x0620][1] = 1'b1 Step 2 : read : reg[0x0620] [7:0] for Number of error bytes received. read : reg[0x0620] [8] (1 indicates PRBS data is coming in and checker is locked)	Generated data will be going to Cu cable side, to disable this transmission : write : reg[0x041F] = 0x1000

Note

Different MAC packet parameters can be further configured with register[0x061B] and register[0x0624]

7.3.1.4 Temperature and Voltage Sensing

Temperature sensor of PHY can be used to give the indication of the temperature of the system and reading can be taken on the fly by reading the temperature sensor output register.

Voltage sensor senses the voltage of all the supply pins: vdda, vddio and vdd1p0. Each pins active voltage can be sensed by reading the corresponding voltage sensor output register.

All sensors are always active and monitor state machine polls the value of each sensor periodically. Monitor state machine can be further programmed to give higher priority/sampling time to one sensor over another by using MONITOR_CTRL_3 register.

Following software sequence can be used to read out any sensor's output:

- Step1 : Program register[0x0467] = 0x6004 ; Initial configuration of monitors
- Step 2 : Program register [0x046A] = 0x00A6 and then register [0x046A]=0x00A3; Refresh the monitors
- Step 3 : Program register[0x0468] to select the corresponding sensor to be polled and read register [0x047B] [14:7] for selected sensor's output code.
- Step 4 : Feed the values of read sensor's output code (in decimal) in following equations to get the sensor's output value in decimals. Refer to Sensor Select Table for required value of constants to be used in equations :
  - vdda_value = 3.3 + (vdda_output_code - vdda_output_mean_code)*slope_vdda_sensor
  - vdd1p0_value = 1.0 + (vdd1p0_output_code - vdd1p0_ouput_mean_code)*slope_vdd1p0_sensor
  - vddio_calculated = 3.3 + (vddio_ouput_code - vddio_output_mean_code)*slope_vddio_sensor
  - temperature_calculated = 25 + (temperature_output_code - temperature_output_mean_code)*slope_temperature_sensor

Table 7-3. Sensor Select Table

Register[0x0468]	Sensor Selected To Read-out
0x1920	VDDA Voltage Sensor
0x2920	VDD1P0 Voltage Sensor
0x3920	VDDIO Voltage Sensor
0x4920	Temperature Sensor

Table 7-4. Sensor's Constant Values

Constant	Value (in decimal)
vdda_output_mean_code	128
slope_vdda3p3_sensor	8.63014e-3
vdd1p0_output_mean_code	93
slope_vdd1p0_sensor	2.85714e-3
vddio_output_mean_code	224
slope_vddio_sensor	15.686e-3
temperature_output_mean_code	161
slope_temperature_sensor	1.5

Note

Accuracy of temperature sensor can be maximized (7.5degreeC), if customer can sample "temperature_output_code" at 25C and use it as "temperature_output_mean_code".

7.3.1.5 Electrostatic Discharge Sensing

Electrostatic discharge is a serious issue for electronic circuits and if not properly mitigated can create short-term issues (signal integrity, link drops, packet loss) as well as long-term reliability faults. The DP83TG720S-Q1 has robust integrated ESD circuitry and offers an ESD sensing architecture. ESD events can be detected on MDI pins for further analysis and debug.

The ESD sensing tool is useful for both prototyping and end-applications. Additionally, the DP83TG720S-Q1 provides an interrupt status flag; when an ESD event is logged in the register<0x0442>. Hardware and software resets are ignored by the ESDS register to prevent unwarranted clearing.

Table 7-5. ESD Sensing : Interrupt Setting and Count Reading

Function	Required Read/Write
Interrupt Enable	• Write register<0x0012>[3] = 1
ESD Event Counter	• Read register<0x0442>[14:9] • Value in decimal indicates the ESD strikes since power-up.

7.3.2 Compliance Test Modes

The six test modes for the DP83TG720S-Q1 are compliant to IEEE 802.3bp, Sub-clause 97.5.2. Supported test modes allow testing of the transmitter waveform Power Spectral Density (PSD) mask, distortion, MDI Master jitter, MDI Slave jitter, droop, transmitter frequency, frequency tolerance, BER monitoring, return loss, and mode conversion. Any of the three GPIOs can be used to output TX_TCLK for MDI Slave jitter measurement.

7.3.2.1 Test Mode 1

Test mode 1 tests the transmitter clock jitter when linked to a partner. In test mode 1, the DP83TG720S-Q1 PHYs are connected over link segment defined in section 97.6 within IEEE 802.3bp. TX_TCLK125 is a divided clock derived from TX_TCLK, which is one sixth the frequency.

7.3.2.2 Test Mode 2

Test mode 2 tests the transmitter MDI Master mode jitter. In test mode 2, the DP83TG720S-Q1 will transmit a continuous pattern of three {+1} symbols followed by three {-1} symbols. The transmitted symbols are timed from the 750-MHz source, which results in a 125-MHz signal.

7.3.2.3 Test Mode 4

Test mode 4 tests the transmitter distortion. In test mode 4, the DP83TG720S-Q1 will transmit the sequence of symbols generated by Equation 1:

$$g(x) = 1 + x^9 + x^{11} \quad (1)$$

The bit sequences, x0n and x1n, are generated from combinations of the scrambler in accordance to and :

$$'x0_n = Scr_n[0] \quad (2)$$

$$x1_n = Scr_n[1] \text{ ^ } Scr_n[4] \quad (3)$$

$$x2_n = Scr_n[1] \text{ ^ } Scr_n[5] \quad (4)$$

Example streams of the 3-bit nibbles are shown in Table 7-6.

Table 7-6. Transmitter Test Mode 4 Symbol Mapping

x2n	x1n	x0n	T1n	T0n
0	0	0	-1	-1
0	0	1	0	-1
0	1	0	-1	0
0	1	1	-1	+1
1	0	0	+1	0
1	0	1	+1	-1
1	1	0	+1	+1
1	1	1	0	+1

7.3.2.4 Test Mode 5

Test mode 5 tests the transmitter PSD mask. In test mode 5, the DP83TG720S-Q1 will transmit normal Inter-Frame IDLE PAM3 symbols.

7.3.2.5 Test Mode 6

Test mode 6 tests the transmitter droop. In test mode 6, the DP83TG720S-Q1 transmits fifteen {+1} symbols followed by fifteen {-1} symbols with symbol transmission at 750-MHz. This 25-MHz pattern is repeated continuously until the test mode is disabled.

7.3.2.6 Test Mode 7

Test mode 7 enabled bit error rate measurement on a link segment. This mode uses zero data pattern on the MDI to check BER by comparing an expected zero data pattern to any non-zero bit received. Error checking is performed after FEC and 80B/81B decoding.

Table 7-7. Test Mode Register Setting

MMD	Register	Value	Test Mode
MMD1	0x0904	0x2000	Test Mode 1 : Tx_Tclk 125MHz is routed to clkout pin.
MMD1	0x0904	0x4000	Test Mode 2
MMD1	0x0904	0x8000	Test Mode 4 : Tx_Tclk 125MHz is routed to clkout pin.
MMD1F	0x0453	0x0019	
MMD1	0x0904	0xA000	Test Mode 5
MMD1	0x0904	0xC000	Test Mode 6
MMD1	0x0904	0xE000	Test Mode 7

7.4 Device Functional Modes

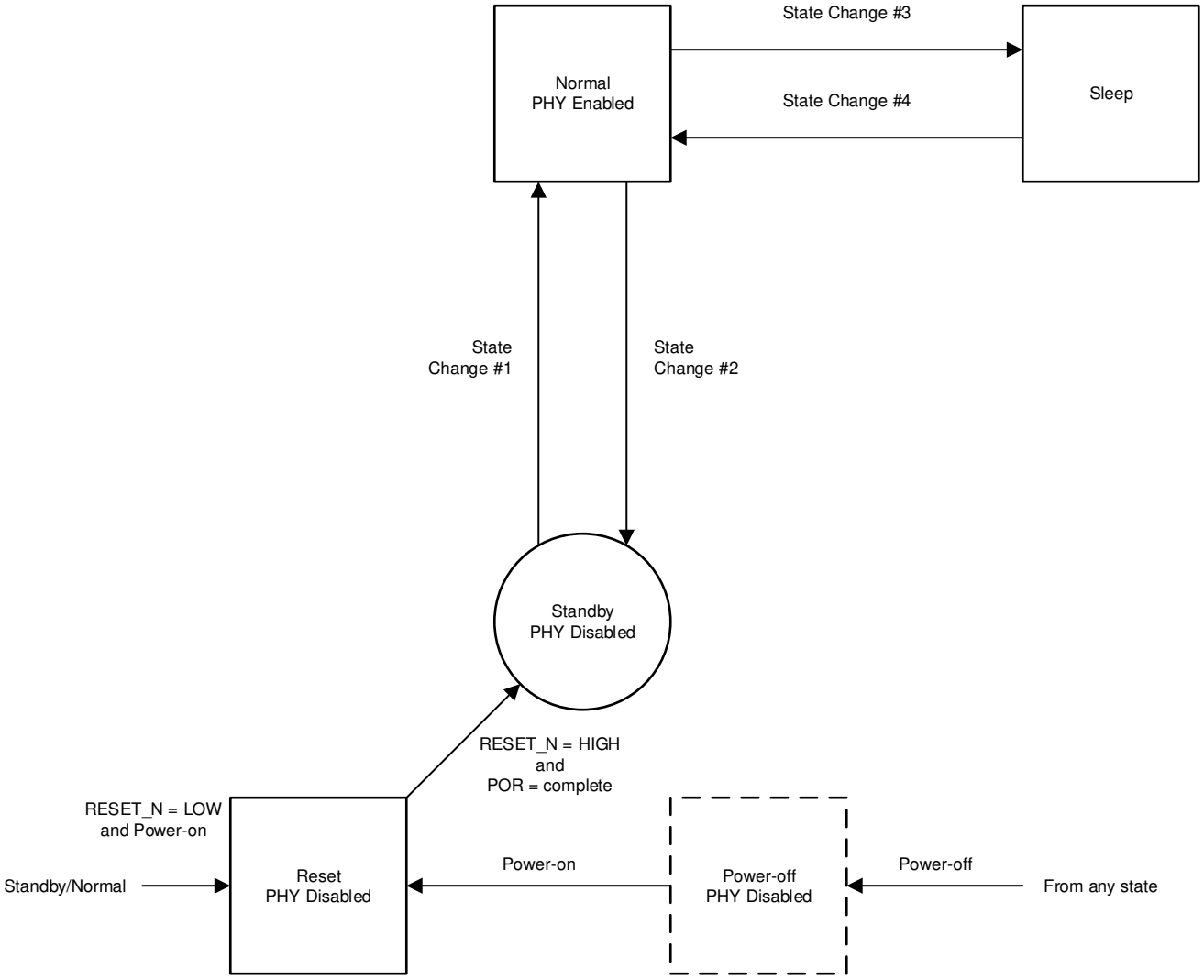

Figure 7-11. PHY Operation State Diagram

7.4.1 Power Down

When VDDA3P3 or VDDIO or VDD1P0 is below the POR threshold, the DP83TG720S-Q1 is in a power-down state. All digital IOs will remain in high impedance state and analog blocks are disabled. PMA termination is not present when in power-down.

7.4.2 Reset

Reset is activated upon power-up, when RESET_N is pulled LOW (for the minimum reset pulse time) or if hardware reset is initiated by setting bit[15] in the register[0x001F].

- Digital state machine restarts after reset and all the register settings are cleared to the boot-up state.
- 25MHz clock on clkout pin will remain active during reset state also.
- MDI/PMA will not have termination during reset state.

Note

Straps are re-latched only with pin reset and not by hardware reset through register (register [0x001F] = x8000.

7.4.3 Standby

The device (MDI Master mode or MDI Slave mode) automatically enters into standby post power-up and reset so long that the device is bootstrapped for managed operation.

In standby, all PHY functions are operational except for PCS and PMA blocks. Link establishment is not possible in standby and data cannot be transmitted or received. SMI functions are operational and register configurations are maintained.

If the device is configured for autonomous operation through bootstrap setting, the PHY automatically switches to normal operation once powered on and reset complete.

7.4.4 Normal

Normal mode can be entered from either autonomous or managed operation. When in autonomous operation, the PHY will automatically try to establish link with a valid Link Partner once powered on.

In managed operation, SMI access is required to allow the device to exit standby; commands issued through the SMI allow the device to exit standby and enables both the PCS and PMA blocks. All device features are operational in normal mode.

Autonomous operation can be enabled through SMI access by setting bit[6] in register 0x18B.

7.4.5 Sleep

Once in sleep mode, all PHY blocks are disabled except for energy detection. All register configurations are lost in sleep mode. No link can be established, data cannot be transmitted or received and SMI access is not available when in sleep mode.

To use sleep mode of PHY refer to implementation highlighted in following figure.

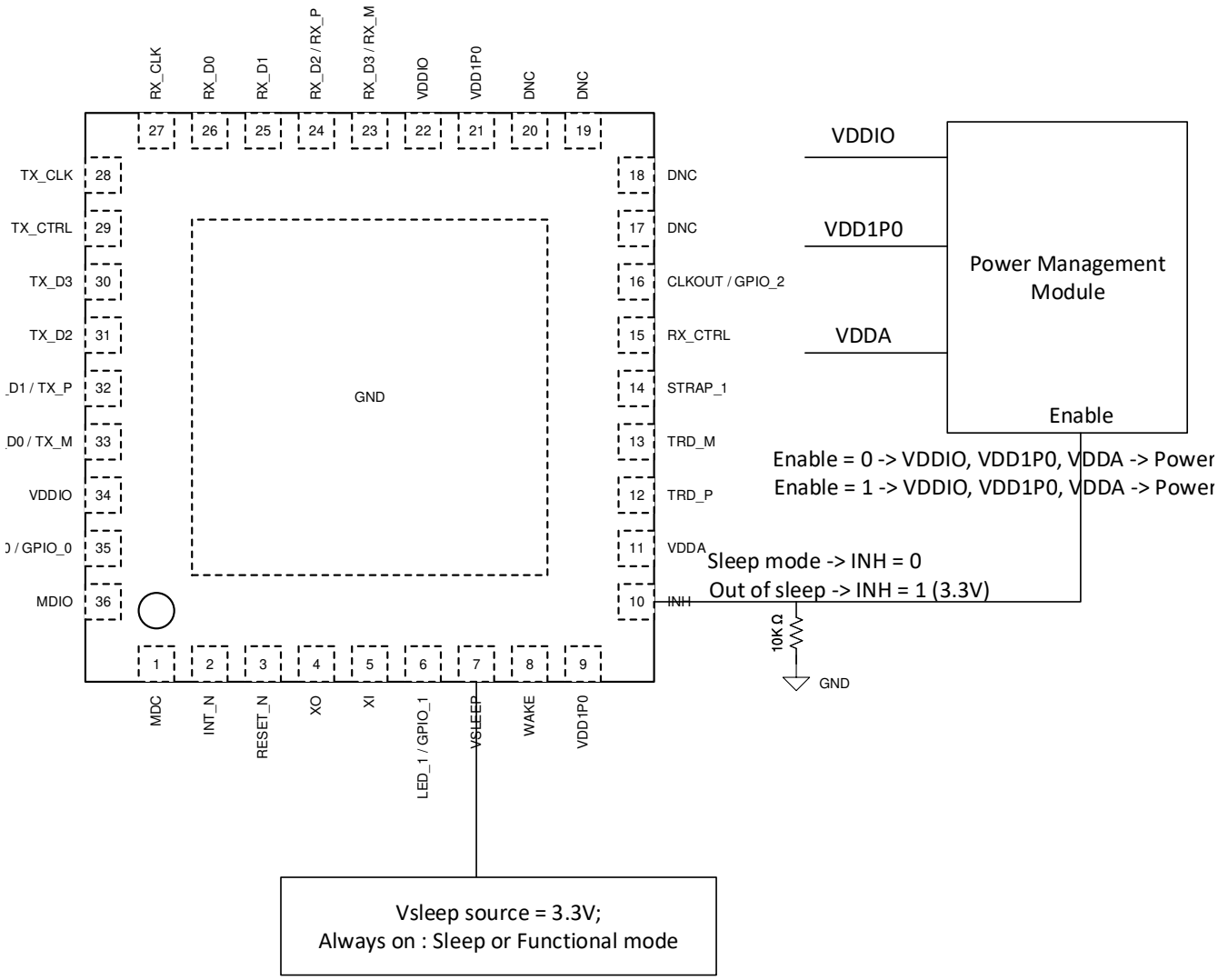

Figure 7-12. Required Implementation for Sleep Mode

Note

Phy will not go into sleep mode if supply sources are not disabled as per above figure.

7.4.6 State Transitions

7.4.6.1 State Transition #1 - Standby to Normal

Autonomous Operation: The PHY will automatically transition to Normal state upon POR completion.

Managed Operation: The PHY will transition to Normal state out of Standby only after writing register <0x018C> = 0x001.

7.4.6.2 State Transition #2 - Normal to Standby

The PHY can be forced back into Standby when in Normal state by writing register <0x018C> = 0x0010.

7.4.6.3 State Transition #3 - Normal to Sleep

Sleep state can be entered either locally (pin/register-write) or by remote link-partner.

Local sleep entry for Master mode phy :

- Step 1 : Write bit[7] = 'b1 of register[0x018B].
- Step 2 : Write reg0x042F = 0x0007, reg0x041E = 0x0100
- Step 3: Make "wake" pin low and hold it low for sleep mode.

Local sleep entry for Slave mode phy :

- Step 1 : Write bit[8] = 'b0 of register[0x018B] register.
- Step 2 : Write bit[7] = 'b1 of register[0x018B] register.
- Step 3 : Write reg0x042F = 0x0007, reg0x041E = 0x0100
- Step 4: Make "wake" pin low and hold it low for sleep mode.

Remote sleep entry for Master mode phy :

- Master can be put to sleep remotely by slave PHY provided the below instructions when the device is already linked-up with the link partner.
- Step 1: Write bit[8] = 'b1 of register [0x018B] register and bit[7] = 'b1 of register[0x018B] register.
- Step 2: Make "wake" pin low
- Step 3: Phy will go into sleep mode with loss of energy on Line

Remote sleep entry for Slave mode phy :

- Step 1 : Write bit[7] = 'b1 of register[0x018B] register.
- Step 2 : Make "wake" pin low.
- Step 3: Phy will go into sleep mode with loss of energy on line (when master will go quite : no data, no send-s).This can be achieved by putting link-partner in managed mode (where device is not allowed to start link-up sequence).

Note

Phy will go into sleep mode only if power supplies are disconnected using INH signal as shown in figure **Required Implementation for Sleep Mode**.

7.4.6.4 State Transition #4 - Sleep to Normal

Sleep state can be exited either locally (pin/register-write) or by remote link-partner.

Local Sleep Exit

Local sleep exit for Master mode PHY by :

- Making "wake" pin high (3.3V).

Local sleep exit for Slave mode PHY by :

- Making "wake" pin high (3.3V).

Remote Sleep Exit

Device can be made to exit the sleep mode by link-partner by either of the following :

1. Remote sleep exit using Send-S symbols from link-partner.
2. Remote sleep exit using Send-T symbols from link-partner

Details of these procedures are in the following table :

Table 7-8. Remote Sleep Exit Procedures

Method	Device Mode	Procedure	Required Link-partner Cabability
Using Send-S	Master	Step 1 : Start IEEE defined Send-S pattern from link-partner for atleast 1.25ms. Step 2 : Put link-partner in the normal mode to start the link-up. Note : Link-partner with low VOD may limit the remote wake-up upto a maximum of 5m cable.	Link-partner needs to have a mode to send Send-S pattern on demand in Slave mode also. One possible way is : Step 1 : Put link-partner in master mode for atleast 1.25ms. Step 2 : Put link-partner in normal mode to start the link-up
	Slave	Step 1 : Start IEEE defined Send-S pattern from link-partner for atleast 1.25ms. Step 2 : Put link-partner in the normal mode to start the link-up. Note : Link-partner with low VOD may limit the remote wake-up upto a maximum of 5m cable. Note : To keep the slave mode DP83TG720 in sleep mode, link-partner can be put in managed mode (where device is not allowed to start link-up sequence).	Any IEEE compliant link-partner will work, as master mode link-partner is supposed to send Send-S signals to start the link-up

Table 7-8. Remote Sleep Exit Procedures (continued)

Method	Device Mode	Procedure	Required Link-partner Cabability
Using Send-T	Master	Step 1 : Enable Send-T pattern on link-partner for atleast 1.25ms. Step 2 : Put link-partner in the normal mode to start the link-up.	Link-partner needs to have a mode to send Send-T pattern on demand. Swing during Send-T mode at pins of link-partner should be greater than 0.92V for remote wake-up over 15m cable. Link-partner with lower VOD may limit the remote wake-up to 5m cable. DP83T720 as link-partner can do the required with following steps : Step 1 : Enable Send-T pattern on DP83TG720 link-partner : write reg[0x0405]=0x7400; reg[0x0509]=0x4007 and reg[0x0576]=0x0500 Step 2 : After 100ms disable send-T pattern on DP83TG720 link-partner : write reg[0x0405]=x5800; reg[0x0509]=0x4005 and reg[0x0576]=0x0000
	Slave	Step 1 : Enable Send-T pattern on link-partner for atleast 1.25ms. Step 2 : Put link-partner in the normal mode to start the link-up.	Link-partner needs to have a mode to send Send-T pattern on demand. Swing during Send-T mode at pins of link-partner should be greater than 0.92V for remote wake-up over 15m cable. Link-partner with lower VOD may limit the remote wake-up to 5m cable. DP83T720 as link-partner can do the required with following steps : Step 1 : Enable Send-T pattern on DP83TG720 link-partner : write reg[0x0405]=0x7400; reg[0x0509]=0x4007 and reg[0x0576]=0x0500 Step 2 : After 100ms disable send-T pattern on DP83TG720 link-partner : write reg[0x0405]=x5800; reg[0x0509]=0x4005 and reg[0x0576]=0x0000

7.4.7 Media Dependent Interface

7.4.7.1 MDI Master and MDI Slave Configuration

MDI Master and MDI Slave are configured using either hardware bootstraps or through register access.

LED_0 controls the MDI Master and MDI Slave bootstrap configuration. By default, MDI Slave mode is configured because there is an internal pulldown resistor on LED_0 pin. If MDI Master mode configuration through hardware bootstrap is preferred, an external pullup resistor is required.

Additionally, bit[14] in the PMA_CTRL2 egister controls the MDI Master and MDI Slave configuration. When this bit is set, MDI Master mode is enabled.

7.4.7.2 Auto-Polarity Detection and Correction

During the link training process, the DP83TG720S-Q1 as MDI receiver is able to detect polarity reversal and automatically correct for the error. Both master and slave detects can do the required correction in the receiver polarity.

Refer to register 0x055B to control the polarity of the PHY's transmitter as required by application. Transmitter polarity can be controlled independent of the received polarity.

7.4.8 MAC Interfaces

7.4.8.1 Reduced Gigabit Media Independent Interface

The DP83TG720S-Q1 also supports Reduced Gigabit Media Independent Interface (RGMII) as specified by RGMII version 2.0. RGMII is designed to reduce the number of pins required to connect MAC and PHY. To accomplish this goal, the control signals are multiplexed. Both rising and falling edges of the clock are used to sample the control signal pin on transmit and receive paths. For 1-Gbps operation, RX_CLK and TX_CLK operate at 125 MHz.

The RGMII signals are summarized in Table 7-9:

Table 7-9. RGMII Signals

FUNCTION	PINS
Data Signals	TX_D[3:0]
	RX_D[3:0]
Control Signals	TX_CTRL
	RX_CTRL
Clock Signals	TX_CLK
	RX_CLK

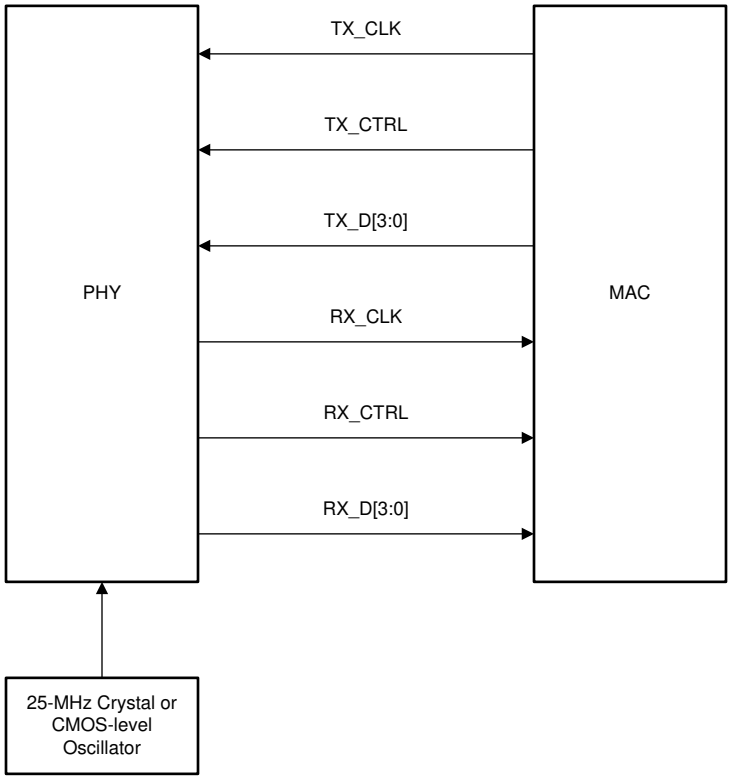

Figure 7-13. RGMII Connections

Table 7-10. RGMII Transmit Encoding

TX_CTRL (POSITIVE EDGE)	TX_CTRL (NEGATIVE EDGE)	TX_D[3:0]	DESCRIPTION
0	0	0000 through 1111	Normal Inter-Frame
0	1	0000 through 1111	Reserved
1	0	0000 through 1111	Normal Data Transmission
1	1	0000 through 1111	Transmit Error Propagation

Table 7-11. RGMII Receive Encoding

RX_CTRL (POSITIVE EDGE)	RX_CTRL (NEGATIVE EDGE)	RX_D[3:0]	DESCRIPTION
0	0	0000 through 1111	Normal Inter-Frame
0	1	0000 through 1101	Reserved
0	1	1110	False Carrier Indication
0	1	1111	Reserved
1	0	0000 through 1111	Normal Data Reception
1	1	0000 through 1111	Data Reception with Errors

The DP83TG720S-Q1 supports in-band status indication to help simplify link status detection. Inter-frame signals on RX_D[3:0] pins as specified in Table 7-12.

Table 7-12. RGMII In-Band Status

RX_CTRL	RX_D3	RX_D[2:1]	RX_D0
0 **Note:** In-band status is only valid when RX_CTRL is low	**Duplex Status:** 0 = Half-Duplex 1 = Full-Duplex	**RX_CLK Clock Speed:** 00 = 2.5 MHz 01 = 25 MHz 10 = 125 MHz 11 = Reserved	**Link Status:** 0 = Link not established 1 = Valid link established

RGMII MAC Interface for Gigabit Ethernet has stringent timing requirements to meet system level performance. To meet these timing requirements and to operate with different MACs over RGMII, it is advised to take the following requirements into consideration when designing PCB. It is also recommended to check board level signal integrity by using the DP83TG720 IBIS model.

RGMII-TX Requirements

- RGMII TX signals should be routed on board with control impedance of 50Ohm +/-15%.
- Max routing length should be limited to 5inch for better signal integrity performance.
- Figure 7-14 shows a RGMII interface requirements for TX* signals. MAC RGMII driver output impedance should be 50Ohm+/-20%.
- Skew for all RGMII TX signals at TP2, in Figure 7-14, should be <±500ps.
- Signal Integrity at TP1 and TP2, in Figure 7-14, should be verified with IBIS model simulation and ensured conformance to following requirements:
  - At TP2, signal should meet rise/fall time of 1ns (20-80%) of signal amplitude.
  - Rise/fall time should be monotonic between VIH/VIL level at TP2.

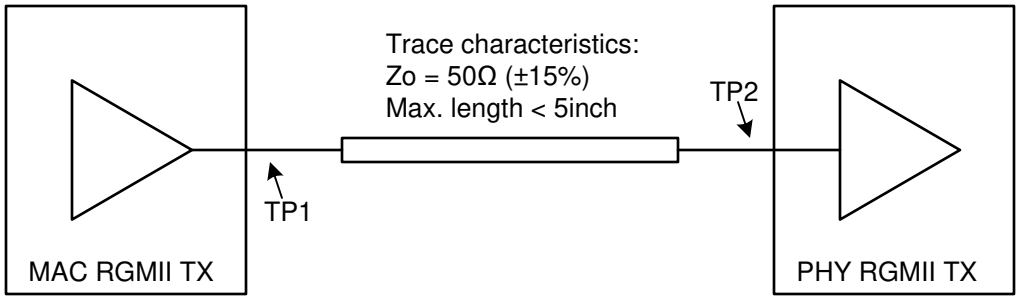

Figure 7-14. RGMII TX Requirements

RGMII-RX Requirements

- RGMII RX signals should be routed on board with control impedance of 50Ohm +/-15%.
- Max routing length should be limited to 5inch for better signal integrity performance.
- No damping resistors should be added at TP3/TP4, in Figure 7-15, as that will impact signal integrity of RX signals.
- Figure 7-15 shows a RGMII interface requirements for RX* signals. MAC RGMII driver output impedance should be 50Ohm+/-20%.
- Signal Integrity at TP3 and TP4, in Figure 7-15, should be verified with IBIS model simulation and ensured conformance to following requirements:
  - At TP4, signal should meet rise/fall time of 1ns (20-80%) of signal amplitude.
  - Rise/fall time should be monotonic between VIH/VIL level at TP4.

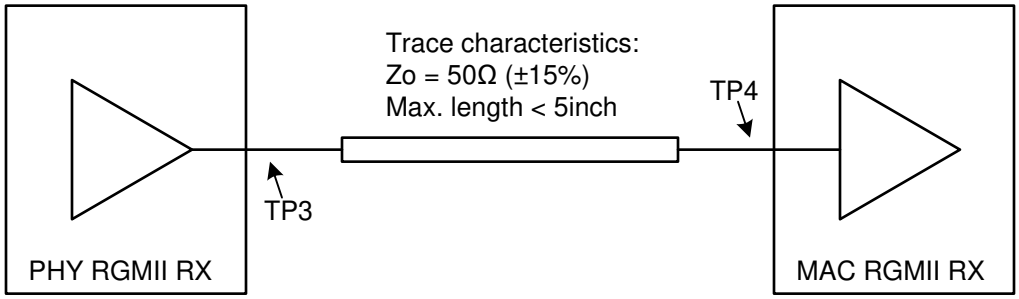

Figure 7-15. RGMII RX Requirements

Note

1. We recommend routing RGMII on buried traces to minimize EMC emissions.
2. Buried traces should be connected with via placement as close as possible to the PHY and MAC.

7.4.8.2 Serial Gigabit Media Independent Interface

The Serial Gigabit Media Independent Interface (SGMII) provides a means for data transfer between MAC and PHY with significantly less signal pins (4 pins) compared to RGMII (12 pins). SGMII uses low-voltage differential signaling (LVDS) to reduce emissions and improve signal quality.

The DP83TG720S-Q1 SGMII is capable of operating in 4-wire mode. In 4-wire operation, two differential pairs are used to transmit and receive data. Clock and data recovery are performed in the MAC and in the PHY in the case of the RX and TX directions, respectively.

SGMII Auto-Negotitation can be disabled by setting bit[0] = 0b0 in the SGMII Configuration Register (SGMIICTL, address 0x608).

The SGMII signals are summarized in Table 7-13.

Table 7-13. SGMII Signals

FUNCTION	PINS
Data Signals	TX_M, TX_P
	RX_M, RX_P

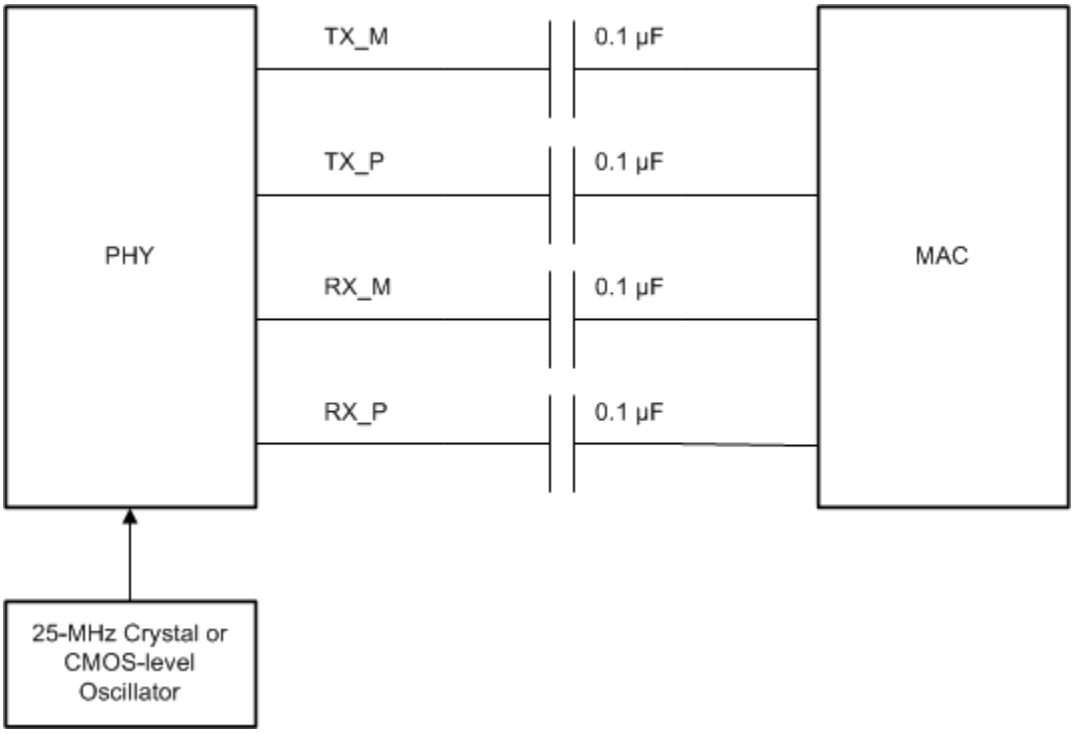

Figure 7-16. SGMII Connections

SGMII MAC Interface for Gigabit Ethernet has stringent signal integrity requirements to meet system level performance. It is advised to take the following requirements into consideration when designing PCB. It is also recommended to check board level signal integrity by using the DP83TG720 IBIS model.

SGMII Signals Guidelines

- Sgmii Tx and Rx signals should be routed on board with control differential impedance of 100ohms +/- 5%.
- Maximum routing length should be limited to 5inch for better signal integrity.
- Mismatch in routing length of p and n should be limited to 5mils.
- AC-coupling caps on rx lines should be placed close to rx_p and rx_m pins of PHY.
- AC-coupling caps on tx lines should be placed close to tx_p and tx_m pins of MAC.
- Signal integrity should be checked only at the pins of the receiver (PHY or MAC) using the high speed differential probe.

- At PHY's TX_M and TX_P following eye mask should be ensured :

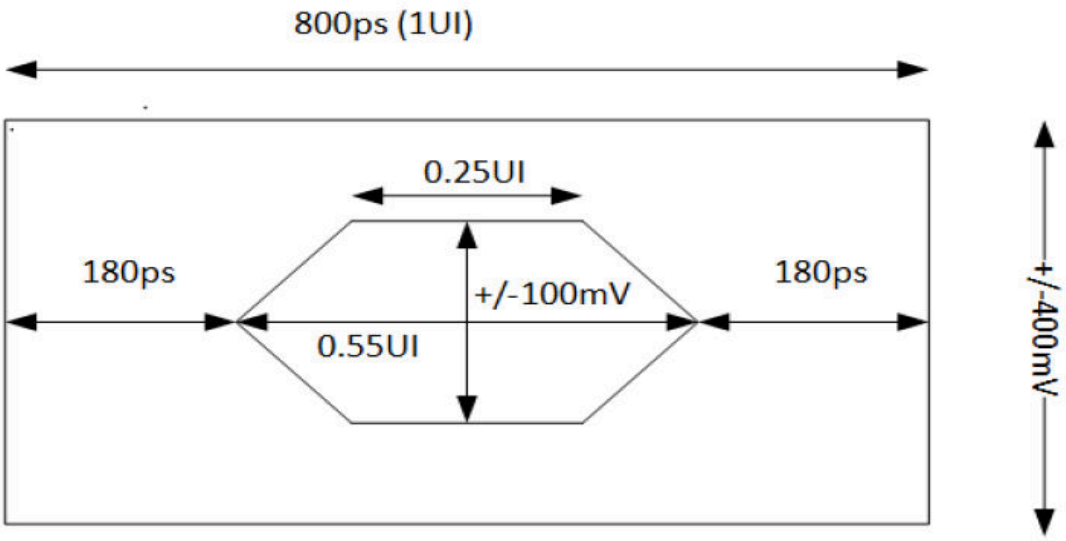

Figure 7-17. Sgmii PHY Receiver Mask Requirement

7.4.9 Serial Management Interface

The Serial Management Interface provides access to the DP83TG720S-Q1 internal register space for status information and configuration. The SMI is compatible with IEEE 802.3 clause 22. The implemented register set consists of the registers required by the IEEE 802.3 plus several others to provide additional visibility and controllability of the DP83TG720S-Q1.

The SMI includes the management clock (MDC) and the management input and output data pin (MDIO). MDC is sourced by the external management entity, also called Station (STA). MDC is not expected to be continuous, and can be turned off by the external management entity when the bus is idle.

MDIO is sourced by the external management entity and by the PHY. The data on the MDIO pin is latched on the rising edge of the MDC. MDIO pin requires a pullup resistor (2.2 KΩ), which pulls MDIO high during IDLE and turnaround.

Up to 9 DP83TG720S-Q1 PHYs can share a common SMI bus. To distinguish between the PHYs, a 3-bit address is used. During power-up-reset, the DP83TG720S-Q1 latches the PHY_AD configuration pins to determine its address.

The management entity must not start an SMI transaction in the first cycle after power-up-reset. To maintain valid operation, the SMI bus must remain inactive at least one MDC cycle after hard reset is deasserted. In normal MDIO transactions, the register address is taken directly from the management-frame reg_addr field, thus allowing direct access to 32 16-bit registers (including those defined in IEEE 802.3 and vendor specific). The data field is used for both reading and writing. The Start code is indicated by a <01> pattern. This pattern makes sure that the MDIO line transitions from the default idle line state. Turnaround is defined as an idle bit time inserted between the Register Address field and the Data field. To avoid contention during a read transaction, no device may actively drive the MDIO signal during the first bit of turnaround. The addressed DP83TG720S-Q1 drives the MDIO with a zero for the second bit of turnaround and follows this with the required data.

For write transactions, the station-management entity writes data to the addressed DP83TG720S-Q1, thus eliminating the requirement for MDIO Turnaround. The turnaround time is filled by the management entity by inserting <10>.

Table 7-14. SMI Protocol Structure

SMI PROTOCOL	<idle> <start> <op code> <device address> <reg address> <turnaround> <data> <idle>
Read Operation	<idle><01><10><AAAAA><RRRRR><Z0><XXXX XXXX XXXX XXXX><idle>
Write Operation	<idle><01><01><AAAAA><RRRRR><10><XXXX XXXX XXXX XXXX><idle>

7.4.10 Direct Register Access

Direct register access can be used for the first 31 registers (0x0h through 0x1Fh).

7.4.11 Extended Register Space Access

The DP83TG720S-Q1 SMI function supports read and write access to the extended register set using registers REGCR (0x000Dh) and ADDAR (0x000Eh) and the MDIO Manageable Device (MMD) indirect method defined in IEEE 802.3ah Draft for Clause 22 for accessing the Clause 45 extended register set.

REGCR (0x000Dh) is the MDIO Manageable MMD access control. In general, register REGCR[4:0] is the device address DEVAD that directs any accesses of ADDAR (0x000Eh) register to the appropriate MMD.

The DP83TG720S-Q1 supports 4 MMD device addresses. The 4 MMD register spaces are:

1. DEVAD[4:0] = 11111 (0x1F) is used for IEEE defined registers (0x00 to 0x1F) and vendor specific registers. This register space is called MMD1F
2. DEVAD[4:0] = 00001 (0x01) is used for 1000BASE-T1 PMA MMD register accesses. This register space is called MMD1.
3. DEVAD[4:0] = 00011 (0x03) is used for vendor specific registers. This register space is called MMD3
4. DEVAD[4:0] = 00111 (0x07) is used for vendor specific registers. This register space is called MMD7

Table 7-15. MMD Register Space Division

MMD Register Space	Register Address Range
MMD1F	0x000 - 0x0EFD
MMD1	0x1000 - 0x1904
MMD3	0x3000 - 0x390D
MMD7	0x7000 - 0x7200

Note

For MMD1/3/7, most significant nibble of the register address is used to denote the respective MMD space. This should be ignored during actual register access operation. For example to access register 0x1904 use 0x0904 as the register address and x01 as the MMD.

All accesses through register REGCR and ADDAR must use the correct DEVAD. Transactions with other DEVADs are ignored. REGCR[15:14] holds the access function: address (00), data with no post increment (01), data with post increment on read and writes (10) and data with post increment on writes only (11).

- ADDAR is the address and data MMD register. ADDAR is used in conjunction with REGCR to provide the access to the extended register set. If register REGCR[15:14] is (00), then ADDAR holds the address of the extended address space register. Otherwise, ADDAR holds the data as indicated by the contents of its address register. When REGCR[15:14] is set to (00), accesses to register ADDAR modify the extended register set address register. This address register must always be initialized in order to access any of the registers within the extended register set.
- When REGCR[15:14] is set to (01), accesses to register ADDAR access the register within the extended register set selected by the value in the address register.
- When REGCR[15:14] is set to (10), access to register ADDAR access the register within the extended register set selected by the value in the address register. After that access is complete, for both reads and writes, the value in the address register is incremented.
- When REGCR[15:14] is set to (11), access to register ADDAR access the register within the extended register set selected by the value in the address register. After that access is complete, for write access only, the value in the address register is incremented. For read accesses, the value of the address register remains unchanged.

The following sections describe how to perform operations on the extended register set using register REGCR and ADDAR.

7.4.12 Write Address Operation

To set the address register:

1. Write the value 0x001F (address function field = 00, DEVAD = '11111') to register REGCR.
2. Write the register address to register ADDAR.

Subsequent writes to register ADDAR (step 2) continue to write the address register.

7.4.12.1 Example - Write Address Operation

For writing register addresses within MMD1 field:

1. Write the value 0x0001 (address function field = 00, DEVAD = '00001') to register REGCR.
2. Write the register address to register ADDAR.

7.4.13 Read Address Operation

To read the address register:

1. Write the value 0x001F (address function field = 00, DEVAD = '11111') to register REGCR.
2. Read the register address from register ADDAR.

Subsequent reads to register ADDAR (step 2) continue to read the address register.

7.4.13.1 Example - Read Address Operation

For reading register addresses within MMD1 field:

1. Write the value 0x0001 (address function field = 00, DEVAD = '00001') to register REGCR.
2. Read the register address from register ADDAR.

7.4.14 Write Operation (No Post Increment)

To write a register in the extended register set:

1. Write the value 0x001F (address function field = 00, DEVAD = '11111') to register REGCR.
2. Write the desired register address to register ADDAR.
3. Write the value 0x401F (data, no post increment function field = 01, DEVAD = '11111') to register REGCR.
4. Write the content of the desired extended register set to register ADDAR.

Subsequent writes to register ADDAR (step 4) continue to rewrite the register selected by the value in the address register.

Note

Steps (1) and (2) can be skipped if the address register was previously configured.

7.4.14.1 Example - Write Operation (No Post Increment)

To write a register in the MMD1 extended register set:

1. Write the value 0x0001 (address function field = 00, DEVAD = '00001') to register REGCR.
2. Write the desired register address to register ADDAR.
3. Write the value 0x4001 (data, no post increment function field = 01, DEVAD = '00001') to register REGCR.
4. Write the content of the desired extended register set to register ADDAR.

7.4.15 Read Operation (No Post Increment)

To read a register in the extended register set:

1. Write the value 0x001F (address function field = 00, DEVAD = '11111') to register REGCR.
2. Write the desired register address to register ADDAR.
3. Write the value 0x401F (data, no post increment function field = 01, DEVAD = '11111') to register REGCR.
4. Read the content of the desired extended register set in register ADDAR.

Subsequent reads to register ADDAR (step 4) continue to reading the register selected by the value in the address register.

Note

Steps (1) and (2) can be skipped if the address register was previously configured.

7.4.15.1 Example - Read Operation (No Post Increment)

To read a register in the MMD1 extended register set:

1. Write the value 0x0001 (address function field = 00, DEVAD = '00001') to register REGCR.
2. Write the desired register address to register ADDAR.
3. Write the value 0x4001 (data, no post increment function field = 01, DEVAD = '00001') to register REGCR.
4. Read the content of the desired extended register set in register ADDAR.

7.4.16 Write Operation (Post Increment)

To write a register in the extended register set with post increment:

1. Write the value 0x001F (address function field = 00, DEVAD = '11111') to register REGCR.
2. Write the desired register address to register ADDAR.
3. Write the value 0x801F (data, post increment function field = 10, DEVAD = '11111') or the value 0xC01F (data, post increment on writes function field = 11, DEVAD = '11111') to register REGCR.
4. Write the content of the desired extended register set to register ADDAR.

Subsequent writes to register ADDAR (step 4) write the next higher addressed data register selected by the value of the address register; the address register is incremented after each access.

7.4.16.1 Example - Write Operation (Post Increment)

To write a register in the MMD1 extended register set with post increment:

1. Write the value 0x0001 (address function field = 00, DEVAD = '00001') to register REGCR.
2. Write the desired register address to register ADDAR.
3. Write the value 0x8001 (data, post increment function field = 10, DEVAD = '00001') or the value 0xC001 (data, post increment on writes function field = 11, DEVAD = '00001') to register REGCR.
4. Write the content of the desired extended register set to register ADDAR.

7.4.17 Read Operation (Post Increment)

To read a register in the extended register set and automatically increment the address register to the next higher value following the write operation:

1. Write the value 0x001F (address function field = 00, DEVAD = '11111') to register REGCR.
2. Write the desired register address to register ADDAR.
3. Write the value 0x801F (data, post increment function field = 10, DEVAD = '11111') to register REGCR.
4. Read the content of the desired extended register set in register ADDAR.

Subsequent reads to register ADDAR (step 4) read the next higher addressed data register selected by the value of the address register; the address register is incremented after each access.

7.4.17.1 Example - Read Operation (Post Increment)

To read a register in the MMD1 extended register set and automatically increment the address register to the next higher value following the write operation:

1. Write the value 0x0001 (address function field = 00, DEVAD = '00001') to register REGCR.
2. Write the desired register address to register ADDAR.
3. Write the value 0x8001 (data, post increment function field = 10, DEVAD = '00001') to register REGCR.
4. Read the content of the desired extended register set in register ADDAR.

7.5 Programming

7.5.1 Strap Configuration

The DP83TG720S-Q1 uses functional pins as strap options to place the device into specific modes of operation. The values of these pins are sampled at power up and hardware reset (through either the RESET_N pin or register access). The strap pins support 2-levels and 3-levels, which are described in greater detail below. Configuration of the device may be done through strapping or through serial management interface.

Note

- Because strap pins are functional pins after reset is deasserted, they should not be connected directly to VCC or GND.
- Pull up strap resistors are sufficient to enter different strap modes.
- Pull down strap resistor can have application for LED pin straps. Refer to LED Configuration section.

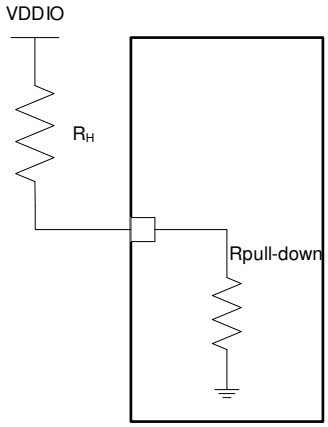

Figure 7-18. Strap Circuit

Table 7-16. Recommended 3-level Strap Resistor Ratios

MODE	IDEAL RH (kΩ)[1] for VDDIO = 3.3 V	IDEAL RH (kΩ)[2] for VDDIO = 2.5 V	IDEAL RH (kΩ)[1] for VDDIO = 1.8V
1	OPEN	OPEN	OPEN
2	13	12	4
3	4.5	2	0.8

1. 10% resistor accuracy
2. 1% resistor accuracy

Table 7-17. Recommended 2-level Strap Resistor

MODE	IDEAL RH (kΩ)[12]
1	OPEN
2	2.49

1. 10% resistor accuracy
2. To gain more margin in customer application for 1.8V VDDIO, either 2.1K+/-10% pull-up can be used or resistor accuracy of 2.49K resistor can be limited to 1%.

The following table describes the DP83TG720S-Q1 configuration bootstraps:

Table 7-18. 2-level Bootstraps

PIN NAME	PIN NO.	STRAP MODE	STRAP FUNCTION	DESCRIPTION
RX_D0	26	1 (default)	MAC[0] = 0	MAC Interface Selection [0]. Refer to Table 7-19 for full description.
		2	MAC[0] = 1	
RX_D1	25	1 (default)	MAC[1] = 0	MAC Interface Selection [1]. Refer to Table 7-19 for full description.
		2	MAC[1] = 1	
RX_D2	24	1 (default)	MAC[2] = 0	MAC Interface Selection [2]. Refer to Table 7-19 for full description.
		2	MAC[2] = 1	
LED_0	1	1 (default)	MS = 0	MDI Master Slave Select. MS = 0 Slave MS = 1 Master
		2	MS = 1	
LED_1	6	1 (default)	$\overline{\text{AUTO}}$ = 0	Autonomous Disable $\overline{\text{AUTO}}$ = 0 Autonomous $\overline{\text{AUTO}}$ = 1 Managed
		2	$\overline{\text{AUTO}}$ = 1	

Table 7-19. MAC Interface Selection Bootstraps

MAC[2]	MAC[1]	MAC[0]	DESCRIPTION
0	0	0	SGMII (4-wire)
0	0	1	RESERVED
0	1	0	RESERVED
0	1	1	RESERVED
1	0	0	RGMII (Align Mode)
1	0	1	RGMII (TX Shift Mode)
1	1	0	RGMII (TX and RX Shift Mode)
1	1	1	RGMII (RX Shift Mode)

Table 7-20. 3-Level Bootstrap: PHY Address

PHY_AD[3:0]	RX_CTRL STRAP MODE	STRP_1 STRAP MODE	DESCRIPTION
0000	1	1	PHY Address: 0x0000 (0)
0001	-	-	RESERVED
0010	-	-	RESERVED
0011	-	-	RESERVED
0100	2	1	PHY Address: 0x0004 (4)
0101	3	1	PHY Address: 0x0005 (5)
0110	-	-	RESERVED
0111	-	-	RESERVED
1000	1	2	PHY Address: 0x0008 (8)
1001	-	-	RESERVED
1010	1	3	PHY Address: 0x000A (10)
1011	-	-	RESERVED
1100	2	2	PHY Address: 0x000C (12)
1101	3	2	PHY Address: 0x000D (13)
1110	2	3	PHY Address: 0x000E (14)
1111	3	3	PHY Address: 0x000F (15)

7.5.2 LED Configuration

The DP83TG720S-Q1 supports up to three configurable Light Emitting Diode (LED) pins: LED_0, LED_1, and LED_2 (CLKOUT). Several functions can be multiplexed onto the LEDs for different modes of operation. LED operations are selected using registers 0x0450 and 0x0451.

Note

CLKOUT has 25MHz clock output as default. If required, it can be configured to LED2 using register 0x0453.

Because the LED output pins are also used as strap pins, external components required for strapping and the user must consider the LED usage to avoid contention. Specifically, when the LED outputs are used to drive LEDs directly, the active state of each output driver is dependent on the logic level sampled by the corresponding input upon power up or hardware reset.

Figure 7-19 shows the two proper ways of connecting LEDs directly to the DP83TG720S-Q1.

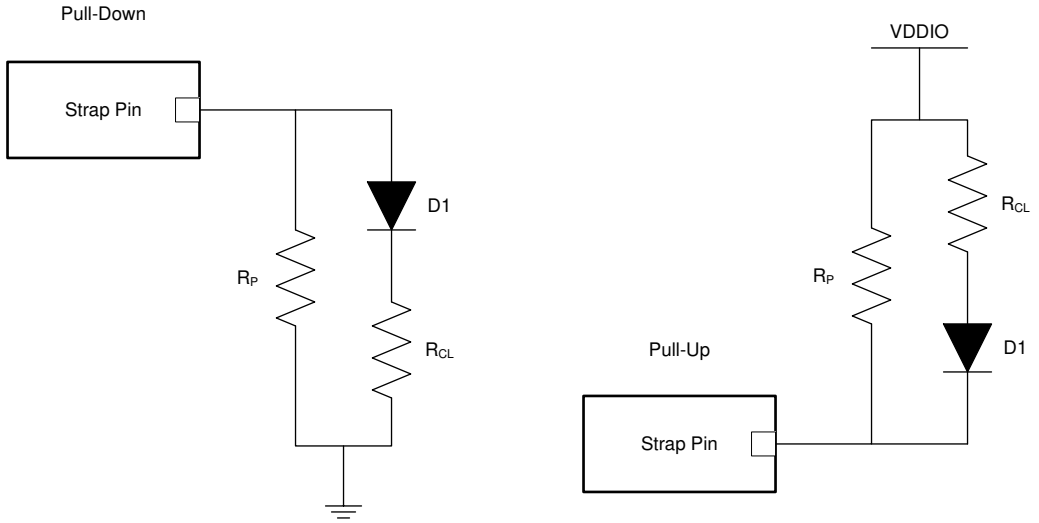

Figure 7-19. Example Strap Connections

7.5.3 PHY Address Configuration

The DP83TG720S-Q1 can be set to respond to any of 9 possible PHY addresses through bootstrap pins. The PHY address is latched into the device upon power-up or hardware reset. Each DP83TG720S-Q1 or port sharing PHY on the serial management bus in the system must have a unique PHY address. The DP83TG720S-Q1 supports PHY address as described in Table 7-20.

By default, the DP83TG720S-Q1 will latch to a PHY address of 0 ([0000]). This address can be changed by adding pullup resistors to bootstrap pins found in Table 7-18.

7.6 Register Maps

7.6.1 Register Access Summary

There are two different methods for accessing registers within the field. Direct register access method is only allowed for the first 31 registers (0x0h through 0x1Fh) of MMD1F register space. Registers beyond 0x1Fh must be accessed by use of the Indirect Method (Extended Register Space) described in *Section 7.4.11*.

Table 7-21. MMD Register Space Division

MMD REGISTER SPACE	REGISTER ADDRESS RANGE
MMD1F	0x000 - 0x0EFD
MMD1	0x1000 - 0x1904
MMD3	0x3000 - 0x390D
MMD7	0x7000 - 0x7200

Table 7-22. Register Access Summary

REGISTER FIELD	REGISTER ACCESS METHODS
0x0h through 0x1Fh	Direct Access
	Indirect Access, MMD1F = '11111' **Example:** to read register 0x17h in MMD1F field with no post increment Step 1) write 0x1Fh to register 0xDh Step 2) write 0x17h to register 0xEh Step 3) write 0x401Fh to register 0xDh Step 4) read register 0xEh
MMD1F Field 0x20h - 0xFFFh	Indirect Access, MMD1F = '11111' **Example:** to read register 0x462h in MMD1F field with no post increment Step 1) write 0x1Fh to register 0xDh Step 2) write 0x462h to register 0xEh Step 3) write 0x401Fh to register 0xDh Step 4) read register 0xEh
MMD1 Field 0x0000h - 0x0FFFh	Indirect Access, MMD1 = '00001' **Example:** to read register 0x7h in MMD1 field with no post increment Step 1) write 0x1h to register 0xDh Step 2) write 0x7h to register 0xEh Step 3) write 0x4001h to register 0xDh Step 4) read register 0xEh

7.6.2 DP83TG720 Registers

Table 7-23 lists the memory-mapped registers for the DP83TG720 registers. All register offset addresses not listed in Table 7-23 should be considered as reserved locations and the register contents should not be modified.

Table 7-23. DP83TG720 Registers

Offset	Acronym	Register Name	Section
0h	BMCR		Section 7.6.2.1
1h	BMSR		Section 7.6.2.2
2h	PHYID1		Section 7.6.2.3
3h	PHYID2		Section 7.6.2.4
Dh	REGCR		Section 7.6.2.5
Eh	ADDAR		Section 7.6.2.6
10h	MII_REG_10		Section 7.6.2.7
11h	MII_REG_11		Section 7.6.2.8
12h	MII_REG_12		Section 7.6.2.9
13h	MII_REG_13		Section 7.6.2.10
16h	MII_REG_16		Section 7.6.2.11
18h	MII_REG_18		Section 7.6.2.12
19h	MII_REG_19		Section 7.6.2.13
1Eh	MII_REG_1E		Section 7.6.2.14
1Fh	MII_REG_1F		Section 7.6.2.15
180h	LSR		Section 7.6.2.16
18Bh	LPS_CFG2		Section 7.6.2.17
18Ch	LPS_CFG3		Section 7.6.2.18
309h	TDR_STATUS0		Section 7.6.2.19
30Ah	TDR_STATUS1		Section 7.6.2.20
30Bh	TDR_STATUS2		Section 7.6.2.21
30Eh	TDR_STATUS5		Section 7.6.2.22
30Fh	TDR_TC12		Section 7.6.2.23
405h	A2D_REG_05		Section 7.6.2.24
41Eh	A2D_REG_30		Section 7.6.2.25
41Fh	A2D_REG_31		Section 7.6.2.26
428h	A2D_REG_40		Section 7.6.2.27
429h	A2D_REG_41		Section 7.6.2.28
42Bh	A2D_REG_43		Section 7.6.2.29
42Ch	A2D_REG_44		Section 7.6.2.30
42Eh	A2D_REG_46		Section 7.6.2.31
42Fh	A2D_REG_47		Section 7.6.2.32
430h	A2D_REG_48		Section 7.6.2.33
442h	A2D_REG_66		Section 7.6.2.34
450h	LEDS_CFG_1		Section 7.6.2.35
451h	LEDS_CFG_2		Section 7.6.2.36
452h	IO_MUX_CFG_1		Section 7.6.2.37
453h	IO_MUX_CFG_2		Section 7.6.2.38
454h	IO_CONTROL_1		Section 7.6.2.39
455h	IO_CONTROL_2		Section 7.6.2.40
456h	IO_CONTROL_3		Section 7.6.2.41
457h	IO_STATUS_1		Section 7.6.2.42

Table 7-23. DP83TG720 Registers (continued)

Offset	Acronym	Register Name	Section
458h	IO_STATUS_2		Section 7.6.2.43
459h	IO_CONTROL_4		Section 7.6.2.44
45Ah	IO_CONTROL_5		Section 7.6.2.45
45Dh	SOR_VECTOR_1		Section 7.6.2.46
45Eh	SOR_VECTOR_2		Section 7.6.2.47
467h	MONITOR_CTRL1		Section 7.6.2.48
468h	MONITOR_CTRL2		Section 7.6.2.49
46Ah	MONITOR_CTRL4		Section 7.6.2.50
47Bh	MONITOR_STAT1		Section 7.6.2.51
50Ah	BREAK_LINK_TIMER		Section 7.6.2.52
510h	RS_DECODER		Section 7.6.2.53
514h	LPS_CONTROL_1		Section 7.6.2.54
515h	LPS_CONTROL_2		Section 7.6.2.55
518h	MAXWAIT_TIMER		Section 7.6.2.56
519h	PHY_CTRL_1G		Section 7.6.2.57
531h	TEST_MODE		Section 7.6.2.58
543h	LINK_QUAL_1		Section 7.6.2.59
544h	LINK_QUAL_2		Section 7.6.2.60
545h	LINK_DOWN_LATCH_STAT		Section 7.6.2.61
547h	LINK_QUAL_3		Section 7.6.2.62
548h	LINK_QUAL_4		Section 7.6.2.63
552h	RS_DECODER_FRAME_STAT_2		Section 7.6.2.64
559h	PMA_WATCHDOG		Section 7.6.2.65
55Bh	SYMB_POL_CFG		Section 7.6.2.66
55Ch	OAM_CFG		Section 7.6.2.67
561h	TEST_MEM_CFG		Section 7.6.2.68
573h	FORCE_CTRL1		Section 7.6.2.69
600h	RGMII_CTRL		Section 7.6.2.70
601h	RGMII_FIFO_STATUS		Section 7.6.2.71
602h	RGMII_DELAY_CTRL		Section 7.6.2.72
608h	SGMII_CTRL_1		Section 7.6.2.73
60Ah	SGMII_STATUS		Section 7.6.2.74
60Ch	SGMII_CTRL_2		Section 7.6.2.75
60Dh	SGMII_FIFO_STATUS		Section 7.6.2.76
618h	PRBS_STATUS_1		Section 7.6.2.77
619h	PRBS_CTRL_1		Section 7.6.2.78
61Ah	PRBS_CTRL_2		Section 7.6.2.79
61Bh	PRBS_CTRL_3		Section 7.6.2.80
61Ch	PRBS_STATUS_2		Section 7.6.2.81
61Dh	PRBS_STATUS_3		Section 7.6.2.82
61Eh	PRBS_STATUS_4		Section 7.6.2.83
620h	PRBS_STATUS_6		Section 7.6.2.84
622h	PRBS_STATUS_8		Section 7.6.2.85
623h	PRBS_STATUS_9		Section 7.6.2.86
624h	PRBS_CTRL_4		Section 7.6.2.87

Table 7-23. DP83TG720 Registers (continued)

Offset	Acronym	Register Name	Section
625h	PRBS_CTRL_5		Section 7.6.2.88
626h	PRBS_CTRL_6		Section 7.6.2.89
627h	PRBS_CTRL_7		Section 7.6.2.90
628h	PRBS_CTRL_8		Section 7.6.2.91
629h	PRBS_CTRL_9		Section 7.6.2.92
62Ah	PRBS_CTRL_10		Section 7.6.2.93
638h	CRC_STATUS		Section 7.6.2.94
639h	PKT_STAT_1		Section 7.6.2.95
63Ah	PKT_STAT_2		Section 7.6.2.96
63Bh	PKT_STAT_3		Section 7.6.2.97
63Ch	PKT_STAT_4		Section 7.6.2.98
63Dh	PKT_STAT_5		Section 7.6.2.99
63Eh	PKT_STAT_6		Section 7.6.2.100
871h	SQI_REG_1		Section 7.6.2.101
875h	DSP_REG_75		Section 7.6.2.102
8ADh	SQI_1		Section 7.6.2.103
1000h	PMA_PMD_CONTROL_1	First nibble (0x1) in the register address is to indicated MMD register space. For register access, ignore the first nibble.	Section 7.6.2.104
1007h	PMA_PMD_CONTROL_2	First nibble (0x1) in the register address is to indicated MMD register space. For register access, ignore the first nibble.	Section 7.6.2.105
1009h	PMA_PMD_TRANSMIT_DISABLE	First nibble (0x1) in the register address is to indicated MMD register space. For register access, ignore the first nibble.	Section 7.6.2.106
100Bh	PMA_PMD_EXTENDED_ABILITY2	First nibble (0x1) in the register address is to indicated MMD register space. For register access, ignore the first nibble.	Section 7.6.2.107
1012h	PMA_PMD_EXTENDED_ABILITY	First nibble (0x1) in the register address is to indicated MMD register space. For register access, ignore the first nibble.	Section 7.6.2.108
1834h	PMA_PMD_CONTROL	First nibble (0x1) in the register address is to indicated MMD register space. For register access, ignore the first nibble.	Section 7.6.2.109
1900h	PMA_CONTROL	First nibble (0x1) in the register address is to indicated MMD register space. For register access, ignore the first nibble.	Section 7.6.2.110
1901h	PMA_STATUS	First nibble (0x1) in the register address is to indicated MMD register space. For register access, ignore the first nibble.	Section 7.6.2.111
1902h	TRAINING	First nibble (0x1) in the register address is to indicated MMD register space. For register access, ignore the first nibble.	Section 7.6.2.112
1903h	LP_TRAINING	First nibble (0x1) in the register address is to indicated MMD register space. For register access, ignore the first nibble.	Section 7.6.2.113
1904h	TEST_MODE_CONTROL	First nibble (0x1) in the register address is to indicated MMD register space. For register access, ignore the first nibble.	Section 7.6.2.114
3000h	PCS_CONTROL_COPY	First nibble (0x3) in the register address is to indicated MMD register space. For register access, ignore the first nibble.	Section 7.6.2.115

Table 7-23. DP83TG720 Registers (continued)

Offset	Acronym	Register Name	Section
3900h	PCS_CONTROL	First nibble (0x3) in the register address is to indicated MMD register space. For register access, ignore the first nibble.	Section 7.6.2.116
3901h	PCS_STATUS	First nibble (0x3) in the register address is to indicated MMD register space. For register access, ignore the first nibble.	Section 7.6.2.117
3902h	PCS_STATUS_2	First nibble (0x3) in the register address is to indicated MMD register space. For register access, ignore the first nibble.	Section 7.6.2.118
3904h	OAM_TRANSMIT	First nibble (0x3) in the register address is to indicated MMD register space. For register access, ignore the first nibble.	Section 7.6.2.119
3905h	OAM_TX_MESSAGE_1	First nibble (0x3) in the register address is to indicated MMD register space. For register access, ignore the first nibble.	Section 7.6.2.120
3906h	OAM_TX_MESSAGE_2	First nibble (0x3) in the register address is to indicated MMD register space. For register access, ignore the first nibble.	Section 7.6.2.121
3907h	OAM_TX_MESSAGE_3	First nibble (0x3) in the register address is to indicated MMD register space. For register access, ignore the first nibble.	Section 7.6.2.122
3908h	OAM_TX_MESSAGE_4	First nibble (0x3) in the register address is to indicated MMD register space. For register access, ignore the first nibble.	Section 7.6.2.123
3909h	OAM_RECEIVE	First nibble (0x3) in the register address is to indicated MMD register space. For register access, ignore the first nibble.	Section 7.6.2.124
390Ah	OAM_RX_MESSAGE_1	First nibble (0x3) in the register address is to indicated MMD register space. For register access, ignore the first nibble.	Section 7.6.2.125
390Bh	OAM_RX_MESSAGE_2	First nibble (0x3) in the register address is to indicated MMD register space. For register access, ignore the first nibble.	Section 7.6.2.126
390Ch	OAM_RX_MESSAGE_3	First nibble (0x3) in the register address is to indicated MMD register space. For register access, ignore the first nibble.	Section 7.6.2.127
390Dh	OAM_RX_MESSAGE_4	First nibble (0x3) in the register address is to indicated MMD register space. For register access, ignore the first nibble.	Section 7.6.2.128
7200h	AN_CFG	First nibble (0x7) in the register address is to indicated MMD register space. For register access, ignore the first nibble.	Section 7.6.2.129

7.6.2.1 BMCR Register (Offset = 0h) [Reset = 0140h]

BMCR is shown in Figure 7-20 and described in Table 7-24.

Return to the Table 7-23.

Figure 7-20. BMCR Register

15	14	13	12	11	10	9	8
mii_reset	loopback	RESERVED	RESERVED	power_down	isolate	RESERVED	RESERVED
R/WMC-0h	R/W-0h	R-0h	R-0h	R/W-0h	R/W-0h	R-0h	R-1h
7	6	5	4	3	2	1	0
RESERVED	speed_sel_msb	RESERVED	RESERVED				
R-0h	R-1h	R-0h	R-0h				

Table 7-24. BMCR Register Field Descriptions

Bit	Field	Type	Reset	Description
15	mii_reset	R/WMC	0h	1b = Digital in reset and all MII regs (0x0 - 0xF) reset to default 0b = No reset
14	loopback	R/W	0h	1b = MII loopback 0b = No MII loopback
13	RESERVED	R	0h	Reserved
12	RESERVED	R	0h	Reserved
11	power_down	R/W	0h	1b = Power down via register or pin 0b = Normal mode
10	isolate	R/W	0h	1b = MAC isolate mode (No output to MAC from the PHY) 0b = Normal Mode
9	RESERVED	R	0h	Reserved
8	RESERVED	R	1h	Reserved
7	RESERVED	R	0h	Reserved
6	speed_sel_msb	R	1h	0b= Reserved 1b= 1000 Mb/s
5	RESERVED	R	0h	Reserved
4-0	RESERVED	R	0h	Reserved

7.6.2.2 BMSR Register (Offset = 1h) [Reset = 0141h]

BMSR is shown in Figure 7-21 and described in Table 7-25.

Return to the Table 7-23.

Figure 7-21. BMSR Register

15	14	13	12	11	10	9	8
RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	extended_status
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-1h
7	6	5	4	3	2	1	0
unidirectional_ability	preamble_supression	aneg_complete	remote_fault	aneg_ability	link_status	jabber_detect	extended_capability
R-0h	R-1h	R-0h	R/W0C-0h	R-0h	R/W0S-0h	R/W0C-0h	R-1h

Table 7-25. BMSR Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	Reserved
14	RESERVED	R	0h	Reserved
13	RESERVED	R	0h	Reserved
12	RESERVED	R	0h	Reserved
11	RESERVED	R	0h	Reserved
10	RESERVED	R	0h	Reserved
9	RESERVED	R	0h	Reserved
8	extended_status	R	1h	1b = Extended status information in Register 15 0b = No extended status information in Register 15
7	unidirectional_ability	R	0h	Reserved
6	preamble_supression	R	1h	1b = PHY will accept management frames with preamble suppressed. 0b = PHY will not accept management frames with preamble suppressed
5	aneg_complete	R	0h	Reserved
4	remote_fault	R/W0C	0h	Reserved
3	aneg_ability	R	0h	Reserved
2	link_status	R/W0S	0h	1b = link is up 0b = link down
1	jabber_detect	R/W0C	0h	Reserved
0	extended_capability	R	1h	1b = extended register capabilities 0b = basic register set capabilities only

7.6.2.3 PHYID1 Register (Offset = 2h) [Reset = 2000h]

PHYID1 is shown in Figure 7-22 and described in Table 7-26.

Return to the Table 7-23.

Figure 7-22. PHYID1 Register

15	14	13	12	11	10	9	8
oui_21_16							
R-2000h							
7	6	5	4	3	2	1	0
oui_21_16							
R-2000h							

Table 7-26. PHYID1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	oui_21_16	R	2000h	Unique identifier for the part

7.6.2.4 PHYID2 Register (Offset = 3h) [Reset = A284h]

PHYID2 is shown in Figure 7-23 and described in Table 7-27.

Return to the Table 7-23.

Figure 7-23. PHYID2 Register

15	14	13	12	11	10	9	8
oui_5_0						model_number	
R-28h						R-28h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
model_number				rev_number			
R-28h				R-4h			

Table 7-27. PHYID2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-10	oui_5_0	R	28h	Unique identifier for the part
9-4	model_number	R	28h	Unique identifier for the part
3-0	rev_number	R	4h	Unique identifier for the part

7.6.2.5 REGCR Register (Offset = Dh) [Reset = 0000h]

REGCR is shown in Figure 7-24 and described in Table 7-28.

Return to the Table 7-23.

Figure 7-24. REGCR Register

15	14	13	12	11	10	9	8
Extended Register Command		RESERVED					
R/W-0h		R/W-0h					
7	6	5	4	3	2	1	0
RESERVED			DEVAD				
R/W-0h			R/W-0h				

Table 7-28. REGCR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	Extended Register Command	R/W	0h	00b = Address 01b = Data, no post increment 10b = Data, post increment on read and write 11b = Data, post increment on write only
13-5	RESERVED	R/W	0h	Reserved
4-0	DEVAD	R/W	0h	RESERVED

7.6.2.6 ADDAR Register (Offset = Eh) [Reset = 0000h]

ADDAR is shown in Figure 7-25 and described in Table 7-29.

Return to the Table 7-23.

Figure 7-25. ADDAR Register

15	14	13	12	11	10	9	8
Address/Data							
R/W-0h							
7	6	5	4	3	2	1	0
Address/Data							
R/W-0h							

Table 7-29. ADDAR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	Address/Data	R/W	0h	

7.6.2.7 MII_REG_10 Register (Offset = 10h) [Reset = 0004h]

MII_REG_10 is shown in Figure 7-26 and described in Table 7-30.

Return to the Table 7-23.

Figure 7-26. MII_REG_10 Register

15	14	13	12	11	10	9	8
RESERVED					signal_detect	descr_lock_bit	RESERVED
R-0h					R/W0S-0h	R/W0S-0h	R-0h
7	6	5	4	3	2	1	0
mii_int_bit	RESERVED			mii_loopback	duplex_mode_env	RESERVED	link_status_bit
0h	R-0h			R-0h	R-1h	R-0h	R-0h

Table 7-30. MII_REG_10 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-11	RESERVED	R	0h	Reserved
10	signal_detect	R/W0S	0h	1b = Channel ok is set 0b = Channel ok had been reset
9	descr_lock_bit	R/W0S	0h	1b = Descrambler is locked 0b = Descrmabler had been locked
8	RESERVED	R	0h	Reserved
7	mii_int_bit		0h	1b = Interrupt pin had been set 0b = Interrupts pin not set
6-4	RESERVED	R	0h	Reserved
3	mii_loopback	R	0h	1b = MII loopback 0b = No MII loopback
2	duplex_mode_env	R	1h	1b = Full duplex 0b = Half duplex
1	RESERVED	R	0h	Reserved
0	link_status_bit	R	0h	1b = link is up 0b = link had been down

7.6.2.8 MII_REG_11 Register (Offset = 11h) [Reset = 000Bh]

MII_REG_11 is shown in Figure 7-27 and described in Table 7-31.

Return to the Table 7-23.

Figure 7-27. MII_REG_11 Register

15	14	13	12	11	10	9	8
RESERVED	RESERVED	RESERVED		RESERVED	RESERVED	RESERVED	RESERVED
R/W-0h	R/W-0h	R/W-0h		R/WSC-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED		int_polarity	force_interrupt	int_en	RESERVED
R-0h	R/W-0h	R/W-0h		R/W-1h	R/W-0h	R/W-1h	R/W-1h

Table 7-31. MII_REG_11 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R/W	0h	Reserved
14	RESERVED	R/W	0h	Reserved
13-12	RESERVED	R/W	0h	Reserved
11	RESERVED	R/WSC	0h	Reserved
10	RESERVED	R/W	0h	Reserved
9	RESERVED	R/W	0h	Reserved
8	RESERVED	R/W	0h	Reserved
7	RESERVED	R	0h	Reserved
6	RESERVED	R/W	0h	Reserved
5-4	RESERVED	R/W	0h	Reserved
3	int_polarity	R/W	1h	1b = Active low 0b = Active high
2	force_interrupt	R/W	0h	1b = Force interrupt pin 0b = Do not force interrupt pin
1	int_en	R/W	1h	1b = Enable interrupts 0b = Disable interrupts
0	RESERVED	R/W	1h	Reserved

7.6.2.9 MII_REG_12 Register (Offset = 12h) [Reset = 0000h]

MII_REG_12 is shown in Figure 7-28 and described in Table 7-32.

Return to the Table 7-23.

Figure 7-28. MII_REG_12 Register

15	14	13	12	11	10	9	8
link_qual_int	energy_det_int	link_int	RESERVED	esd_int	ms_train_done_int	RESERVED	RESERVED
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h
7	6	5	4	3	2	1	0
link_qual_int_en	energy_det_int_en	link_int_en	unused_int_3	esd_int_en	ms_train_done_int_en	unused_int_2	unused_int_1
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 7-32. MII_REG_12 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	link_qual_int	R	0h	Link quality bad interrupt status
14	energy_det_int	R	0h	Energy det change interrupt status
13	link_int	R	0h	Link status change interrupt status
12	RESERVED	R	0h	Reserved
11	esd_int	R	0h	ESD fault detected interrupt status
10	ms_train_done_int	R	0h	Training done interrupt status
9	RESERVED	R	0h	Reserved
8	RESERVED	R	0h	Reserved
7	link_qual_int_en	R/W	0h	Link quality bad interrupt enable
6	energy_det_int_en	R/W	0h	Energy det change interrupt enable
5	link_int_en	R/W	0h	Link status change interrupt enable
4	unused_int_3	R/W	0h	Reserved
3	esd_int_en	R/W	0h	ESD fault detected interrupt enable
2	ms_train_done_int_en	R/W	0h	Training done interrupt enable
1	unused_int_2	R/W	0h	Reserved
0	unused_int_1	R/W	0h	Reserved

7.6.2.10 MII_REG_13 Register (Offset = 13h) [Reset = 0000h]

MII_REG_13 is shown in Figure 7-29 and described in Table 7-33.

Return to the Table 7-23.

Figure 7-29. MII_REG_13 Register

15	14	13	12	11	10	9	8
under_volt_int	over_volt_int	RESERVED	RESERVED	over_temp_int	sleep_int	pol_change_int	not_one_hot_int
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h
7	6	5	4	3	2	1	0
under_volt_int_en	over_volt_int_en	unused_int_6	unused_int_5	over_temp_int_en	sleep_int_en	pol_change_int_en	not_one_hot_int_en
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 7-33. MII_REG_13 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	under_volt_int	R	0h	Under volt interrupt status
14	over_volt_int	R	0h	Over volt interrupt status
13	RESERVED	R	0h	Reserved
12	RESERVED	R	0h	Reserved
11	over_temp_int	R	0h	Over temp interrupt status
10	sleep_int	R	0h	Sleep mode change interrupt status
9	pol_change_int	R	0h	Data polarity change interrupt status
8	not_one_hot_int	R	0h	Not one hot interrupt status
7	under_volt_int_en	R/W	0h	Under volt interrupt enable
6	over_volt_int_en	R/W	0h	Over volt interrupt enable
5	unused_int_6	R/W	0h	Reserved
4	unused_int_5	R/W	0h	Reserved
3	over_temp_int_en	R/W	0h	Over temp interrupt enable
2	sleep_int_en	R/W	0h	Sleep mode change interrupt enable
1	pol_change_int_en	R/W	0h	Data Polarity change interrupt enable
0	not_one_hot_int_en	R/W	0h	Not one hot interrupt enable

7.6.2.11 MII_REG_16 Register (Offset = 16h) [Reset = 0000h]

MII_REG_16 is shown in Figure 7-30 and described in Table 7-34.

Return to the Table 7-23.

Figure 7-30. MII_REG_16 Register

15	14	13	12	11	10	9	8
RESERVED					prbs_sync_loss	RESERVED	core_pwr_mode
R-0h					R/W0C-0h	R-0h	R-0h
7	6	5	4	3	2	1	0
cfg_dig_pcs_loopback	loopback_mode						
R/W-0h	R/W-0h						

Table 7-34. MII_REG_16 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-11	RESERVED	R	0h	Reserved
10	prbs_sync_loss	R/W0C	0h	1b = Prbs lock had been lost 0b = Prbs lock never lost
9	RESERVED	R	0h	Reserved
8	core_pwr_mode	R	0h	1b = Core is is normal power mode 0b = Core is in power down or sleep mode
7	cfg_dig_pcs_loopback	R/W	0h	PCS digital loopback
6-0	loopback_mode	R/W	0h	000001b = PCS loop 000010b = RS loop 000100b = Digital loop 001000B = Analog loop 010000b = Reverse loop

7.6.2.12 MII_REG_18 Register (Offset = 18h) [Reset = 0008h]

MII_REG_18 is shown in Figure 7-31 and described in Table 7-35.

Return to the Table 7-23.

Figure 7-31. MII_REG_18 Register

15	14	13	12	11	10	9	8
ack_received_int	tx_valid_clr_int	RESERVED	RESERVED	por_done_int	no_frame_int	wake_req_int	lps_int
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h
7	6	5	4	3	2	1	0
ack_received_int_en	tx_valid_clr_int_en	RESERVED	RESERVED	por_done_int_en	no_frame_int_en	wake_req_int_en	lps_int_en
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h

Table 7-35. MII_REG_18 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	ack_received_int	R	0h	Ack received interrupt status (OAM)
14	tx_valid_clr_int	R	0h	mr_tx_valid clear interrupt status (OAM)
13	RESERVED	R	0h	Reserved
12	RESERVED	R	0h	Reserved
11	por_done_int	R	0h	POR done interrupt status
10	no_frame_int	R	0h	No frame detect interrupt status
9	wake_req_int	R	0h	Wake request interrupt status
8	lps_int	R	0h	LPS interrupt status
7	ack_received_int_en	R/W	0h	Ack received interrupt enable (OAM)
6	tx_valid_clr_int_en	R/W	0h	mr_tx_valid clear interrupt enable (OAM)
5	RESERVED	R/W	0h	Reserved
4	RESERVED	R/W	0h	Reserved
3	por_done_int_en	R/W	1h	POR done interrupt enable
2	no_frame_int_en	R/W	0h	No frame detect interrupt enable
1	wake_req_int_en	R/W	0h	Wake request interrupt enable
0	lps_int_en	R/W	0h	LPS interrupt enable

7.6.2.13 MII_REG_19 Register (Offset = 19h) [Reset = X]

MII_REG_19 is shown in Figure 7-32 and described in Table 7-36.

Return to the Table 7-23.

Figure 7-32. MII_REG_19 Register

15	14	13	12	11	10	9	8
RESERVED					RESERVED	RESERVED	
R-0h					R-0h	R-0h	
7	6	5	4	3	2	1	0
RESERVED			SOR_PHYADDR				
R-0h			R-X				

Table 7-36. MII_REG_19 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-11	RESERVED	R	0h	Reserved
10	RESERVED	R	0h	Reserved
9-5	RESERVED	R	0h	Reserved
4-0	SOR_PHYADDR	R	X	PHY ADDRESS latched from strap

7.6.2.14 MII_REG_1E Register (Offset = 1Eh) [Reset = 0000h]

MII_REG_1E is shown in Figure 7-33 and described in Table 7-37.

Return to the Table 7-23.

Figure 7-33. MII_REG_1E Register

15	14	13	12	11	10	9	8
tdr_start	cfg_tdr_auto_run	RESERVED					
R/WMC-0h	R/W-0h	R-0h					
7	6	5	4	3	2	1	0
RESERVED						tdr_done	tdr_fail
R-0h						R-0h	R-0h

Table 7-37. MII_REG_1E Register Field Descriptions

Bit	Field	Type	Reset	Description
15	tdr_start	R/WMC	0h	1b = TDR start 0b = No TDR
14	cfg_tdr_auto_run	R/W	0h	1b = TDR start automatically on link down 0b = TDR start manually
13-2	RESERVED	R	0h	Reserved
1	tdr_done	R	0h	TDR done status
0	tdr_fail	R	0h	TDR fail status

7.6.2.15 MII_REG_1F Register (Offset = 1Fh) [Reset = 0000h]

MII_REG_1F is shown in Figure 7-34 and described in Table 7-38.

Return to the Table 7-23.

Figure 7-34. MII_REG_1F Register

15	14	13	12	11	10	9	8
sw_global_reset	digital_reset	RESERVED	RESERVED				
R/WMC-0h	R/WMC-0h	R/W-0h	R/W-0h				
7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	RESERVED				
R/W-0h	R/W-0h	R-0h	R/W-0h				

Table 7-38. MII_REG_1F Register Field Descriptions

Bit	Field	Type	Reset	Description
15	sw_global_reset	R/WMC	0h	Hardware reset - Reset digital + register file
14	digital_reset	R/WMC	0h	Soft reset - Reset only digital core
13	RESERVED	R/W	0h	Reserved
12-8	RESERVED	R/W	0h	Reserved
7	RESERVED	R/W	0h	Reserved
6	RESERVED	R/W	0h	Reserved
5	RESERVED	R	0h	Reserved
4-0	RESERVED	R/W	0h	Reserved

7.6.2.16 LSR Register (Offset = 180h) [Reset = 0000h]

LSR is shown in Figure 7-35 and described in Table 7-39.

Return to the Table 7-23.

Figure 7-35. LSR Register

15	14	13	12	11	10	9	8
link_up	link_down	phy_ctrl_send_data	link_status	RESERVED			
R-0h	R-0h	R-0h	R-0h	R-0h			
7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	descr_sync	loc_rcvr_status	rem_rcvr_status
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

Table 7-39. LSR Register Field Descriptions

Bit	Field	Type	Reset	Description
15	link_up	R	0h	Link up defined by CnS
14	link_down	R	0h	Link down as defined by CnS
13	phy_ctrl_send_data	R	0h	Phy control in send data status
12	link_status	R	0h	Link status
11-8	RESERVED	R	0h	Reserved
7	RESERVED	R	0h	Reserved
6	RESERVED	R	0h	Reserved
5	RESERVED	R	0h	Reserved
4	RESERVED	R	0h	Reserved
3	RESERVED	R	0h	Reserved
2	descr_sync	R	0h	Descrambler lock status
1	loc_rcvr_status	R	0h	Local receiver status
0	rem_rcvr_status	R	0h	Remote receiver status

7.6.2.17 LPS_CFG2 Register (Offset = 18Bh) [Reset = 0000h]

LPS_CFG2 is shown in Figure 7-36 and described in Table 7-40.

Return to the Table 7-23.

Figure 7-36. LPS_CFG2 Register

15	14	13	12	11	10	9	8
RESERVED							ed_en
R-0h							R/W-0h
7	6	5	4	3	2	1	0
sleep_en	cfg_auto_mode_en_strap	cfg_lps_mon_en_strap	cfg_lps_sleep_auto	cfg_lps_slp_confirm	cfg_lps_auto_pwrdn	cfg_lps_sleep_en	cfg_lps_sm_en
R/W-0h	R/WMC,1-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 7-40. LPS_CFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	RESERVED	R	0h	Reserved
8	ed_en	R/W	0h	1b = Enable energy detection on MDI 0b = Disable energy detection on MDI
7	sleep_en	R/W	0h	1b = Allow PHY to enter sleep 0b = Do not allow PHY to enter sleep
6	cfg_auto_mode_en_strap	R/WMC,1	0h	LPS autonomous mode enable 1b = PHY enters normal mode on power up 0b = PHY enters standby mode on power up
5	cfg_lps_mon_en_strap	R/W	0h	
4	cfg_lps_sleep_auto	R/W	0h	Reserved
3	cfg_lps_slp_confirm	R/W	0h	Reserved
2	cfg_lps_auto_pwrdn	R/W	0h	Reserved
1	cfg_lps_sleep_en	R/W	0h	Reserved
0	cfg_lps_sm_en	R/W	0h	Reserved

7.6.2.18 LPS_CFG3 Register (Offset = 18Ch) [Reset = 0000h]

LPS_CFG3 is shown in Figure 7-37 and described in Table 7-41.

Return to the Table 7-23.

Figure 7-37. LPS_CFG3 Register

15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
cfg_lps_pwr_mode_7	cfg_lps_pwr_mode_6	cfg_lps_pwr_mode_5	cfg_lps_pwr_mode_4	cfg_lps_pwr_mode_3	cfg_lps_pwr_mode_2	cfg_lps_pwr_mode_1	cfg_lps_pwr_mode_0
R/WMC,0-0h	R/WMC,0-0h	R/WMC,0-0h	R/WMC,0-0h	R/WMC,0-0h	R/WMC,0-0h	R/WMC,0-0h	R/WMC,0-0h

Table 7-41. LPS_CFG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R	0h	Reserved
7	cfg_lps_pwr_mode_7	R/WMC,0	0h	Reserved
6	cfg_lps_pwr_mode_6	R/WMC,0	0h	Reserved
5	cfg_lps_pwr_mode_5	R/WMC,0	0h	Reserved
4	cfg_lps_pwr_mode_4	R/WMC,0	0h	Set to enter standby mode
3	cfg_lps_pwr_mode_3	R/WMC,0	0h	Reserved
2	cfg_lps_pwr_mode_2	R/WMC,0	0h	Reserved
1	cfg_lps_pwr_mode_1	R/WMC,0	0h	Reserved
0	cfg_lps_pwr_mode_0	R/WMC,0	0h	Set to enter normal mode

7.6.2.19 TDR_STATUS0 Register (Offset = 309h) [Reset = 0000h]

TDR_STATUS0 is shown in Figure 7-38 and described in Table 7-42.

Return to the Table 7-23.

Figure 7-38. TDR_STATUS0 Register

15	14	13	12	11	10	9	8
peak1_loc							
R-0h							
7	6	5	4	3	2	1	0
peak0_loc							
R-0h							

Table 7-42. TDR_STATUS0 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	peak1_loc	R	0h	Peak 1 location in tap index
7-0	peak0_loc	R	0h	Peak 0 location in tap index

7.6.2.20 TDR_STATUS1 Register (Offset = 30Ah) [Reset = 0000h]

TDR_STATUS1 is shown in Figure 7-39 and described in Table 7-43.

Return to the Table 7-23.

Figure 7-39. TDR_STATUS1 Register

15	14	13	12	11	10	9	8
peak3_loc							
R-0h							
7	6	5	4	3	2	1	0
peak2_loc							
R-0h							

Table 7-43. TDR_STATUS1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	peak3_loc	R	0h	Peak 3 location in tap index
7-0	peak2_loc	R	0h	Peak 2 location in tap index

7.6.2.21 TDR_STATUS2 Register (Offset = 30Bh) [Reset = 0000h]

TDR_STATUS2 is shown in Figure 7-40 and described in Table 7-44.

Return to the Table 7-23.

Figure 7-40. TDR_STATUS2 Register

15	14	13	12	11	10	9	8
peak0_amp							
R-0h							
7	6	5	4	3	2	1	0
peak4_loc							
R-0h							

Table 7-44. TDR_STATUS2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	peak0_amp	R	0h	Peak 0 amplitude in echo coeff
7-0	peak4_loc	R	0h	Peak 4 location in tap index

7.6.2.22 TDR_STATUS5 Register (Offset = 30Eh) [Reset = 0000h]

TDR_STATUS5 is shown in Figure 7-41 and described in Table 7-45.

Return to the Table 7-23.

Figure 7-41. TDR_STATUS5 Register

15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED			peak4_sign	peak3_sign	peak2_sign	peak1_sign	peak0_sign
R-0h			R-0h	R-0h	R-0h	R-0h	R-0h

Table 7-45. TDR_STATUS5 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-5	RESERVED	R	0h	Reserved
4	peak4_sign	R	0h	Peak 4 sign
3	peak3_sign	R	0h	Peak 3 sign
2	peak2_sign	R	0h	Peak 2 sign
1	peak1_sign	R	0h	Peak 1 sign
0	peak0_sign	R	0h	Peak 0 sign

7.6.2.23 TDR_TC12 Register (Offset = 30Fh) [Reset = 0000h]

TDR_TC12 is shown in Figure 7-42 and described in Table 7-46.

Return to the Table 7-23.

Figure 7-42. TDR_TC12 Register

15	14	13	12	11	10	9	8
RESERVED		fault_loc					
R-0h		R-0h					
7	6	5	4	3	2	1	0
tdr_state				RESERVED		tdr_activation	
R-0h				R-0h		R-0h	

Table 7-46. TDR_TC12 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	RESERVED	R	0h	Reserved
13-8	fault_loc	R	0h	See TC12
7-4	tdr_state	R	0h	See TC12
3-2	RESERVED	R	0h	Reserved
1-0	tdr_activation	R	0h	See TC12

7.6.2.24 A2D_REG_05 Register (Offset = 405h) [Reset = 6400h]

A2D_REG_05 is shown in Figure 7-43 and described in Table 7-47.

Return to the Table 7-23.

Figure 7-43. A2D_REG_05 Register

15	14	13	12	11	10	9	8
ld_bias_1p0v_sl						RESERVED	
R/W-19h						R/W-0h	
7	6	5	4	3	2	1	0
RESERVED							
R/W-0h							

Table 7-47. A2D_REG_05 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-10	ld_bias_1p0v_sl	R/W	19h	Bits to control the DAC current of LD and hence the swing. 001010b = 400 mV 001011b = 440 mV 001100b = 480 mV 001101b = 520 mV 001110b = 560 mV 001111b = 600 mV 010000b = 640 mV 010001b = 680 mV 010010b = 720 mV 010011b = 760 mV 010100b = 800 mV 010101b = 840 mV 010110b = 880 mV 010111b = 920 mV 011000b = 960 mV 011001b = 1000 mV 011010b = 1040 mV 011011b = 1080 mV 011100b = 1120 mV 011101b = 1160 mV 011110b = 1200 mV
9-0	RESERVED	R/W	0h	Reserved

7.6.2.25 A2D_REG_30 Register (Offset = 41Eh) [Reset = 0000h]

A2D_REG_30 is shown in Figure 7-44 and described in Table 7-48.

Return to the Table 7-23.

Figure 7-44. A2D_REG_30 Register

15	14	13	12	11	10	9	8
RESERVED							spare_in_2_fromdig_sl_force_en
R-0h							R/W-0h
7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	RESERVED	RESERVED			
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h			

Table 7-48. A2D_REG_30 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	RESERVED	R	0h	Reserved
8	spare_in_2_fromdig_sl_force_en	R/W	0h	Force control enable for Reg0x042F
7	RESERVED	R/W	0h	Reserved
6	RESERVED	R/W	0h	Reserved
5	RESERVED	R/W	0h	Reserved
4	RESERVED	R/W	0h	Reserved
3-0	RESERVED	R/W	0h	Reserved

7.6.2.26 A2D_REG_31 Register (Offset = 41Fh) [Reset = 0000h]

A2D_REG_31 is shown in Figure 7-45 and described in Table 7-49.

Return to the Table 7-23.

Figure 7-45. A2D_REG_31 Register

15	14	13	12	11	10	9	8
RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED		
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h		
7	6	5	4	3	2	1	0
RESERVED	RESERVED				RESERVED	RESERVED	RESERVED
R/W-0h	R/W-0h				R/W-0h	R/W-0h	R/W-0h

Table 7-49. A2D_REG_31 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R/W	0h	Reserved
14	RESERVED	R/W	0h	Reserved
13	RESERVED	R/W	0h	Reserved
12	RESERVED	R/W	0h	Reserved
11	RESERVED	R/W	0h	Reserved
10-7	RESERVED	R/W	0h	Reserved
6-3	RESERVED	R/W	0h	Reserved
2	RESERVED	R/W	0h	Reserved
1	RESERVED	R/W	0h	Reserved
0	RESERVED	R/W	0h	Reserved

7.6.2.27 A2D_REG_40 Register (Offset = 428h) [Reset = 6002h]

A2D_REG_40 is shown in Figure 7-46 and described in Table 7-50.

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Figure 7-46. A2D_REG_40 Register

15	14	13	12	11	10	9	8
RESERVED	SGMII_TESTMODE		RESERVED	SGMII_SOP_SON_SLEW_CTRL	RESERVED	RESERVED	
R/W-0h	R/W-3h		R/W-0h	R/W-0h	R/W-0h	R/W-0h	
7	6	5	4	3	2	1	0
RESERVED	RESERVED						RESERVED
R/W-0h	R/W-1h						R/W-0h

Table 7-50. A2D_REG_40 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R/W	0h	Reserved
14-13	SGMII_TESTMODE	R/W	3h	00b = 1000mV Sgmii output swing 01b = 1260mV Sgmii output swing 10b = 900mV Sgmii output swing 11b = 720mV Sgmii output swing
12	RESERVED	R/W	0h	Reserved
11	SGMII_SOP_SON_SLEW_CTRL	R/W	0h	0b =Default output rise/fall time 1b = Slow output rise/fall time
10	RESERVED	R/W	0h	Reserved
9-8	RESERVED	R/W	0h	Reserved
7	RESERVED	R/W	0h	Reserved
6-1	RESERVED	R/W	1h	Reserved
0	RESERVED	R/W	0h	Reserved

7.6.2.28 A2D_REG_41 Register (Offset = 429h) [Reset = 0030h]

A2D_REG_41 is shown in Figure 7-47 and described in Table 7-51.

Return to the Table 7-23.

Figure 7-47. A2D_REG_41 Register

15	14	13	12	11	10	9	8
RESERVED					RESERVED	RESERVED	RESERVED
R/W-0h					R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
RESERVED						SGMII_IO_LOOPBACK_EN	RESERVED
R/W-Ch						R/W-0h	R/W-0h

Table 7-51. A2D_REG_41 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-11	RESERVED	R/W	0h	Reserved
10	RESERVED	R/W	0h	Reserved
9	RESERVED	R/W	0h	Reserved
8	RESERVED	R/W	0h	Reserved
7-2	RESERVED	R/W	Ch	Reserved
1	SGMII_IO_LOOPBACK_EN	R/W	0h	1b = Connects RX and TX signals internally to provide internal loopback option without external components.
0	RESERVED	R/W	0h	Reserved

7.6.2.29 A2D_REG_43 Register (Offset = 42Bh) [Reset = 0000h]

A2D_REG_43 is shown in Figure 7-48 and described in Table 7-52.

Return to the Table 7-23.

Figure 7-48. A2D_REG_43 Register

15	14	13	12	11	10	9	8
SGMII_CDR_TESTMODE_1							
R/W-0h							
7	6	5	4	3	2	1	0
SGMII_CDR_TESTMODE_1							
R/W-0h							

Table 7-52. A2D_REG_43 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	SGMII_CDR_TESTMODE_1	R/W	0h	SGMII RX CDR test mode

7.6.2.30 A2D_REG_44 Register (Offset = 42Ch) [Reset = 0000h]

A2D_REG_44 is shown in Figure 7-49 and described in Table 7-53.

Return to the Table 7-23.

Figure 7-49. A2D_REG_44 Register

15	14	13	12	11	10	9	8
RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	SGMII_DIG_LOOPBACK_EN	RESERVED			RESERVED
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h			R/W-0h

Table 7-53. A2D_REG_44 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R/W	0h	Reserved
14	RESERVED	R/W	0h	Reserved
13	RESERVED	R/W	0h	Reserved
12	RESERVED	R/W	0h	Reserved
11	RESERVED	R/W	0h	Reserved
10	RESERVED	R/W	0h	Reserved
9	RESERVED	R/W	0h	Reserved
8	RESERVED	R/W	0h	Reserved
7	RESERVED	R/W	0h	Reserved
6	RESERVED	R/W	0h	Reserved
5	RESERVED	R/W	0h	Reserved
4	SGMII_DIG_LOOPBACK_EN	R/W	0h	1b = Loops back TX data to RX before the IO
3-1	RESERVED	R/W	0h	Reserved
0	RESERVED	R/W	0h	Reserved

7.6.2.31 A2D_REG_46 Register (Offset = 42Eh) [Reset = 0000h]

A2D_REG_46 is shown in Figure 7-50 and described in Table 7-54.

Return to the Table 7-23.

Figure 7-50. A2D_REG_46 Register

15	14	13	12	11	10	9	8
RESERVED				sgmii_calib_watchdog_dis	sgmii_calib_watchdog_val		sgmii_calib_avg
R-0h				R/W-0h	R/W-0h		R/W-0h
7	6	5	4	3	2	1	0
sgmii_calib_avg	sgmii_do_calib	SGMII_CDR_LOCK_SL	SGMII_MODE_force_en	SGMII_INPUT_TERM_EN_force_en	SGMII_OUTPUT_EN_force_en	SGMII_COMP_OFFSET_TUNE_force_en	SGMII_DATA_SYNC_SL
R/W-0h	R/WSC-0h	R-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R-0h

Table 7-54. A2D_REG_46 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	RESERVED	R	0h	Reserved
11	sgmii_calib_watchdog_dis	R/W	0h	By default, SGMII calibration process has a watchdog timer. If calibration is not ended till timer expires, then it is dsabled and default value is taken. If this bit is set, then the calibration watchdog timer is disabled.
10-9	sgmii_calib_watchdog_val	R/W	0h	Watchdog timer configuration for SGMII calibration sequence: 00 - If not ended, calibration stops after 32us 01 - If not ended, calibration stops after 48us 10 - If not ended, calibration stops after 64us 11 - If not ended, calibration stops after 128us
8-7	sgmii_calib_avg	R/W	0h	Number of repetitions of COMP_OFFSET_TUNE calibration (the repetitions are for averaging): 00 - a single repetition 01 - 2 repetitions 10 - 4 repetitions 11 - 8 repetitions
6	sgmii_do_calib	R/WSC	0h	SGMII start calibration command (mainly for debug) Please notice: This register is WSC (write-self-clear) and not read-only!
5	SGMII_CDR_LOCK_SL	R	0h	Indicates Sgmiis CDR lock status
4	SGMII_MODE_force_en	R/W	0h	
3	SGMII_INPUT_TERM_EN_force_en	R/W	0h	
2	SGMII_OUTPUT_EN_force_en	R/W	0h	
1	SGMII_COMP_OFFSET_TUNE_force_en	R/W	0h	
0	SGMII_DATA_SYNC_SL	R	0h	

7.6.2.32 A2D_REG_47 Register (Offset = 42Fh) [Reset = 0000h]

A2D_REG_47 is shown in Figure 7-51 and described in Table 7-55.

Return to the Table 7-23.

Figure 7-51. A2D_REG_47 Register

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED				RESERVED	spare_in_2_fromdig_sl_2	spare_in_2_fromdig_sl_1	spare_in_2_fromdig_sl_0
R/W-0h				R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 7-55. A2D_REG_47 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-4	RESERVED	R/W	0h	Reserved
3	RESERVED	R/W	0h	Reserved
2	spare_in_2_fromdig_sl_2	R/W	0h	energy lost indication force control value
1	spare_in_2_fromdig_sl_1	R/W	0h	energy lost detector enable force control value
0	spare_in_2_fromdig_sl_0	R/W	0h	[0] - sleep enable force control value Force control enable is controlled by reg0x041E[8]

7.6.2.33 A2D_REG_48 Register (Offset = 430h) [Reset = 0960h]

A2D_REG_48 is shown in Figure 7-52 and described in Table 7-56.

Return to the Table 7-23.

Figure 7-52. A2D_REG_48 Register

15	14	13	12	11	10	9	8
RESERVED	RESERVED	RESERVED	DLL_EN	DLL_TX_DELAY_CTRL_SL			
R-0h	R/W-0h	R/W-0h	R/W-0h	R/W-9h			
7	6	5	4	3	2	1	0
DLL_RX_DELAY_CTRL_SL				RESERVED			
R/W-6h				R/W-0h			

Table 7-56. A2D_REG_48 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	Reserved
14	RESERVED	R/W	0h	Reserved
13	RESERVED	R/W	0h	Reserved
12	DLL_EN	R/W	0h	
11-8	DLL_TX_DELAY_CTRL_SL	R/W	9h	Refer to electrical specification for delay vs code information.
7-4	DLL_RX_DELAY_CTRL_SL	R/W	6h	Refer to electrical specification for delay vs code information.
3-0	RESERVED	R/W	0h	Reserved

7.6.2.34 A2D_REG_66 Register (Offset = 442h) [Reset = 0000h]

A2D_REG_66 is shown in Figure 7-53 and described in Table 7-57.

Return to the Table 7-23.

Figure 7-53. A2D_REG_66 Register

15	14	13	12	11	10	9	8
RESERVED	esd_event_count						RESERVED
R/W-0h	R-0h						R/W-0h
7	6	5	4	3	2	1	0
RESERVED			RESERVED	RESERVED			
R/W-0h			R/W-0h	R/W-0h			

Table 7-57. A2D_REG_66 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R/W	0h	Reserved
14-9	esd_event_count	R	0h	Number gives the number of esd events on the copper channel
8	RESERVED	R/W	0h	Reserved
7-5	RESERVED	R/W	0h	Reserved
4	RESERVED	R/W	0h	Reserved
3-0	RESERVED	R/W	0h	Reserved

7.6.2.35 LEDS_CFG_1 Register (Offset = 450h) [Reset = 2610h]

LEDS_CFG_1 is shown in Figure 7-54 and described in Table 7-58.

Return to the Table 7-23.

Figure 7-54. LEDS_CFG_1 Register

15	14	13	12	11	10	9	8
RESERVED	leds_bypass_stretching	leds_blink_rate		led_2_option			
R-0h	R/W-0h	R/W-2h		R/W-6h			
7	6	5	4	3	2	1	0
led_1_option				led_0_option			
R/W-1h				R/W-0h			

Table 7-58. LEDS_CFG_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	
14	leds_bypass_stretching	R/W	0h	LED Signal Stretch
13-12	leds_blink_rate	R/W	2h	Blink Rate for the LED - 00b = 20Hz (50mSec) 01b = 10Hz (100mSec) 10b = 5Hz (200mSec) 11b = 2Hz (500mSec)
11-8	led_2_option	R/W	6h	0000b = link OK 0001b = link OK + blink on TX/RX activity 0010b = link OK + blink on TX activity 0011b = link OK + blink on RX activity 0100b = link OK + 100Base-T1 Master 0101b = link OK + 100Base-T1 Slave 0110b = TX/RX activity with stretch option 0111b = Reserved 1000b = Reserved 1001b = Link lost (remains on until register 0x1 is read) 1010b = PRBS error latch until cleared by 0x620(1) 1011b = XMII TX/RX Error with stretch option
7-4	led_1_option	R/W	1h	0000b = link OK 0001b = link OK + blink on TX/RX activity 0010b = link OK + blink on TX activity 0011b = link OK + blink on RX activity 0100b = link OK + 100Base-T1 Master 0101b = link OK + 100Base-T1 Slave 0110b = TX/RX activity with stretch option 0111b = Reserved 1000b = Reserved 1001b = Link lost (remains on until register 0x1 is read) 1010b = PRBS error (latch until cleared by 0x620(1) 1011b = XMII TX/RX Error with stretch option
3-0	led_0_option	R/W	0h	0000b = link OK 0001b = link OK + blink on TX/RX activity 0010b = link OK + blink on TX activity 0011b = link OK + blink on RX activity 0100b = link OK + 100Base-T1 Master 0101b = link OK + 100Base-T1 Slave 0110b = TX/RX activity with stretch option 0111b = Reserved 1000b = Reserved 1001b = Link lost (remains on until register 0x1 is read) 1010b = PRBS error (latch until cleared by 0x620(1) 1011b = XMII TX/RX Error with stretch option

7.6.2.36 LEDS_CFG_2 Register (Offset = 451h) [Reset = 0000h]

LEDS_CFG_2 is shown in Figure 7-55 and described in Table 7-59.

Return to the Table 7-23.

Figure 7-55. LEDS_CFG_2 Register

15	14	13	12	11	10	9	8
RESERVED		RESERVED				XXXX	led_2_drv_en
R-0h		R-0h					R/W-0h
7	6	5	4	3	2	1	0
led_2_drv_val	led_2_polarity	led_1_drv_en	led_1_drv_val	led_1_polarity	led_0_drv_en	led_0_drv_val	led_0_polarity
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 7-59. LEDS_CFG_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	RESERVED	R	0h	Reserved
13-10	RESERVED	R	0h	Reserved
11-9	cfg_ieee_compl_sel	R/W	0h	Observe IEEE Compliance signals in LED_0_GPIO_0, when LED_0_GPIO_CTRL= 'h5 as follows - 000b = loc_rcvr_status 001b = rem_rcvr_status 010b = loc_snr_margin 011b = rem_phy_ready 100b = pma_watchdog_status 101b = link_sync_link_control
8	led_2_drv_en	R/W	0h	LED_2 Drive Enable, When set, drives the value as per LED_2_DRV_VAL
7	led_2_drv_val	R/W	0h	LED_2 Drive Value, when LED_2_DRV_EN is set
6	led_2_polarity	R/W	0h	LED_2 polarity
5	led_1_drv_en	R/W	0h	LED_1 Drive Enable, When set, drives the value as per LED_1_DRV_VAL
4	led_1_drv_val	R/W	0h	LED_1 Drive Value, when LED_1_DRV_EN is set
3	led_1_polarity	R/W	0h	LED_1 polarity
2	led_0_drv_en	R/W	0h	LED_0 Drive Enable, When set, drives the value as per LED_0_DRV_VAL
1	led_0_drv_val	R/W	0h	LED_0 Drive Value, when LED_0_DRV_EN is set
0	led_0_polarity	R/W	0h	LED_0 polarity

7.6.2.37 IO_MUX_CFG_1 Register (Offset = 452h) [Reset = 0000h]

IO_MUX_CFG_1 is shown in Figure 7-56 and described in Table 7-60.

Return to the Table 7-23.

Figure 7-56. IO_MUX_CFG_1 Register

15	14	13	12	11	10	9	8
RESERVED		RESERVED			led_1_gpio_ctrl		
R-0h		R/W-0h			R/W-0h		
7	6	5	4	3	2	1	0
RESERVED		RESERVED			led_0_gpio_ctrl		
R-0h		R/W-0h			R/W-0h		

Table 7-60. IO_MUX_CFG_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	RESERVED	R	0h	Reserved
13-11	RESERVED	R/W	0h	Reserved
10-8	led_1_gpio_ctrl	R/W	0h	Controls the output of LED_1 IO - 000b = LED_1 (default: link OK + blink on TX/RX activity) 001b = Reserved 010b = RGMII data match indication 011b = Under-Voltage indication 100b = Interrupt 101b = IEEE compliance signals 110b = constant 0 111b = constant 1
7-6	RESERVED	R	0h	Reserved
5-3	RESERVED	R/W	0h	Reserved
2-0	led_0_gpio_ctrl	R/W	0h	Controls the output of LED_0 IO: 000b = LED_0 (default: LINK) 001b = Reserved 010b = RGMII data match indication 011b = Under-Voltage indication 100b = Interrupt 101b = IEEE compliance signals (see 0x451[11:9]) 110b = constant 0 111b = constant 1

7.6.2.38 IO_MUX_CFG_2 Register (Offset = 453h) [Reset = 0001h]

IO_MUX_CFG_2 is shown in Figure 7-57 and described in Table 7-61.

Return to the Table 7-23.

Figure 7-57. IO_MUX_CFG_2 Register

15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED		clk_o_clk_source			clk_o_gpio_ctrl		
R-0h		R/W-0h			R/W-1h		

Table 7-61. IO_MUX_CFG_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-6	RESERVED	R	0h	Reserved
5-3	clk_o_clk_source	R/W	0h	Clock Observable in CLK_O pin - 000b = xi_osc_25m_1p0v_dl (25MHz crystal output - from analog) 001b = Reserved 010b = Reserved 011b = 125MHz clock 100b = 125MHz clock 101b = Reserved 110b = Reserved 111b = Reserved
2-0	clk_o_gpio_ctrl	R/W	1h	Controls the output of CLK_O IO - 000b = LED_2 (default: TX/RX activity with stretch option(LED_2_OPTION=0x6) 001b = Clock out (see 0x453[5:3]) 010b = RGMII data match indication 011b = Under-Voltage indication 100b = constant 0 101b = constant 0 110b = constant 0 111b = constant 1

7.6.2.39 IO_CONTROL_1 Register (Offset = 454h) [Reset = 0000h]

IO_CONTROL_1 is shown in Figure 7-58 and described in Table 7-62.

Return to the Table 7-23.

Figure 7-58. IO_CONTROL_1 Register

15	14	13	12	11	10	9	8
io_control_1							
R/W-0h							
7	6	5	4	3	2	1	0
io_control_1							
R/W-0h							

Table 7-62. IO_CONTROL_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	io_control_1	R/W	0h	IO_CONTROL_1 : IO reflects the value written on this register when enabled IO_OE_N_FORCE_CTRL=1 and IO_OE_N_VALUE=0 If 0 is written, IO will be forced to ouput LOW. If 1 is written, IO will be forced to ouput HIGH. The following is the bit position for pads. 0=LED_0_GPIO_0; 1=LED_1_GPIO_1; 2=CLKOUT_GPIO_2; 3=INT_N; 4=RESERVED; 5=RESERVED; 6=INH; 7=TX_CLK; 8=TX_CTRL; 9=TX_D0; 10=TX_D1; 11=TX_D2; 12=TX_D3; 13=RX_CLK; 14=RX_CTRL; 15=RX_D0;

7.6.2.40 IO_CONTROL_2 Register (Offset = 455h) [Reset = 0000h]

IO_CONTROL_2 is shown in Figure 7-59 and described in Table 7-63.

Return to the Table 7-23.

Figure 7-59. IO_CONTROL_2 Register

15	14	13	12	11	10	9	8
RESERVED		cfg_other_impedance					pupd_value
R-0h		R/W-0h					R/W-0h
7	6	5	4	3	2	1	0
pupd_value	pupd_force_cntl	io_oe_n_value	io_oe_n_force_ctrl	io_control_2			
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h			

Table 7-63. IO_CONTROL_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	RESERVED	R	0h	Reserved
13-9	cfg_other_impedance	R/W	0h	Slew Rate Control for CLKOUT - 00000b = Default rise/fall time 00001b = Slower rise/fall time 00010b = Faster rise/fall time
8-7	pupd_value	R/W	0h	IO Test mode - pullup/pull down : 00b = No pull (HiZ) 01b = PullUP 10b = PullDown 11b = PullUp/PullDown (Both Enabled)
6	pupd_force_cntl	R/W	0h	IO Test mode pull up/down override functional pull.
5	io_oe_n_value	R/W	0h	IO Test mode direction, related to IO_OE_N_FORCE_CTRL
4	io_oe_n_force_ctrl	R/W	0h	IO Test mode (alternate to BSR). The IO direction is set by IO_OE_N_VALUE and value is set by IO_CONTROL_1/2
3-0	io_control_2	R/W	0h	IO_CONTROL_2 : IO reflects the value written on this register when enabled IO_OE_N_FORCE_CTRL=1 and IO_OE_N_VALUE=0 If 0 is written, IO will be forced to ouput LOW. If 1 is written, IO will be forced to ouput HIGH. The following is the bit position for pads. 0=RX_D1; 1=RX_D2; 2=RX_D3; 3=STRP_1;

7.6.2.41 IO_CONTROL_3 Register (Offset = 456h) [Reset = 0108h]

IO_CONTROL_3 is shown in Figure 7-60 and described in Table 7-64.

Return to the Table 7-23.

Figure 7-60. IO_CONTROL_3 Register

15	14	13	12	11	10	9	8
RESERVED						cfg_mac_rx_impedance	
R-0h						R/W-8h	
7	6	5	4	3	2	1	0
cfg_mac_rx_impedance			RESERVED				
R/W-8h			R/W-8h				

Table 7-64. IO_CONTROL_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-10	RESERVED	R	0h	Reserved
9-5	cfg_mac_rx_impedance	R/W	8h	Slew Rate Control for RGMII pads - 01010b = Medium Slew (OA tr/tf compliant, max tr/tf = 1ns) 01011b = Slowest Slew (For low emissions, max tr/tf = 1.2ns) 01000b = Default mode (rgmii tr/tf compliant, max tr/tf=750ps)
4-0	RESERVED	R/W	8h	Reserved

7.6.2.42 IO_STATUS_1 Register (Offset = 457h) [Reset = 0000h]

IO_STATUS_1 is shown in Figure 7-61 and described in Table 7-65.

Return to the Table 7-23.

Figure 7-61. IO_STATUS_1 Register

15	14	13	12	11	10	9	8
io_status_1							
R-0h							
7	6	5	4	3	2	1	0
io_status_1							
R-0h							

Table 7-65. IO_STATUS_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	io_status_1	R	0h	IO_STATUS_1 : Register reflects the IO value, when enabled IO_OE_N_FORCE_CTRL=1 and IO_OE_N_VALUE=1 If 0 is read, IO is connected LOW at pin. If 1 is read, IO is connected HIGH at pin. The following is the bit position for each pad. 0=LED_0_GPIO_0; 1=LED_1_GPIO_1; 2=CLKOUT_GPIO_2; 3=INT_N; 4=RESERVED; 5=RESERVED; 6=INH; 7=TX_CLK; 8=TX_CTRL; 9=TX_D0; 10=TX_D1; 11=TX_D2; 12=TX_D3; 13=RX_CLK; 14=RX_CTRL; 15=RX_D0;

7.6.2.43 IO_STATUS_2 Register (Offset = 458h) [Reset = 0000h]

IO_STATUS_2 is shown in Figure 7-62 and described in Table 7-66.

Return to the Table 7-23.

Figure 7-62. IO_STATUS_2 Register

15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED				io_status_2			
R-0h				R-0h			

Table 7-66. IO_STATUS_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-4	RESERVED	R	0h	
3-0	io_status_2	R	0h	IO_STATUS_2 : Register reflects the IO value, when enabled IO_OE_N_FORCE_CTRL=1 and IO_OE_N_VALUE=1 If 0 is read, IO is connected LOW at pin. If 1 is read, IO is connected HIGH at pin. The following is the bit position for each pad. 0=RX_D1; 1=RX_D2; 2=RX_D3; 3=STRP_1;

7.6.2.44 IO_CONTROL_4 Register (Offset = 459h) [Reset = 0000h]

IO_CONTROL_4 is shown in Figure 7-63 and described in Table 7-67.

Return to the Table 7-23.

Figure 7-63. IO_CONTROL_4 Register

15	14	13	12	11	10	9	8
io_input_mode							
R/W-0h							
7	6	5	4	3	2	1	0
io_input_mode							
R/W-0h							

Table 7-67. IO_CONTROL_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	io_input_mode	R/W	0h	Each bit configures one pin into input mode as per mapping below - 0=LED_0_GPIO_0; 1=LED_1_GPIO_1; 2=CLKOUT_GPIO_2; 3=INT_N; 4=TX_CLK; 5=TX_CTRL; 6=TX_D0; 7=TX_D1; 8=TX_D2; 9=TX_D3; 10=RX_CLK; 11=RX_CTRL; 12=RX_D0; 13=RX_D1; 14=RX_D2; 15=RX_D3

7.6.2.45 IO_CONTROL_5 Register (Offset = 45Ah) [Reset = 0000h]

IO_CONTROL_5 is shown in Figure 7-64 and described in Table 7-68.

Return to the Table 7-23.

Figure 7-64. IO_CONTROL_5 Register

15	14	13	12	11	10	9	8
io_output_mode							
R/W-0h							
7	6	5	4	3	2	1	0
io_output_mode							
R/W-0h							

Table 7-68. IO_CONTROL_5 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	io_output_mode	R/W	0h	Each bit configures one pin into output mode as per mapping below - 0=LED_0_GPIO_0; 1=LED_1_GPIO_1; 2=CLKOUT_GPIO_2; 3=INT_N; 4=TX_CLK; 5=TX_CTRL; 6=TX_D0; 7=TX_D1; 8=TX_D2; 9=TX_D3; 10=RX_CLK; 11=RX_CTRL; 12=RX_D0; 13=RX_D1; 14=RX_D2; 15=RX_D3

7.6.2.46 SOR_VECTOR_1 Register (Offset = 45Dh) [Reset = 0000h]

SOR_VECTOR_1 is shown in Figure 7-65 and described in Table 7-69.

Return to the Table 7-23.

Figure 7-65. SOR_VECTOR_1 Register

15	14	13	12	11	10	9	8
RGMII_TX_SHIFT	RGMII_RX_SHIFT	SGMII_EN	RGMII_EN	TEST_MODE			MAC_MODE
R-0h	R-0h	R-0h	R-0h	R-0h			R-0h
7	6	5	4	3	2	1	0
MAC_MODE		MAS/SLV	PHY_AD				
R-0h		R-0h	R-0h				

Table 7-69. SOR_VECTOR_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RGMII_TX_SHIFT	R	0h	0x0 = TX shift disbaled 0x1 = TX shift enabled
14	RGMII_RX_SHIFT	R	0h	0x0 = RX shift disabled 0x1 = RX shift enabled
13	SGMII_EN	R	0h	0x0 = SGMII disabled 0x1 = SGMII enabled
12	RGMII_EN	R	0h	0x0 = RGMII disabled 0x1 = RGMII enabled
11-9	TEST_MODE	R	0h	
8-6	MAC_MODE	R	0h	0x0 = SGMII 0x1 = Reserved 0x2 = Reserved 0x3 = Reserved 0x4 = RGMII align 0x5 = RGMII TX shift 0x6 = RGMII TX and RX shift 0x7 = RGMII RX shift
5	MAS/SLV	R	0h	0x0 = Slave 0x1 = Master
4-0	PHY_AD	R	0h	0x0 = PHY address 0 0x4 = PHY address 4 0x5 = PHY address 5 0x8 = PHY address 8 0xA = PHY address A 0xC = PHY address C 0xD = PHY address D 0xE = PHY address E 0xF = PHY address F

7.6.2.47 SOR_VECTOR_2 Register (Offset = 45Eh) [Reset = 0000h]

SOR_VECTOR_2 is shown in Figure 7-66 and described in Table 7-70.

Return to the Table 7-23.

Figure 7-66. SOR_VECTOR_2 Register

15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							AUTO/ MANAGED
R-0h							R-0h

Table 7-70. SOR_VECTOR_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-1	RESERVED	R	0h	Reserved
0	AUTO/MANAGED	R	0h	0x0 = Autonomous mode enabled 0x1 = Managed mode enabled

7.6.2.48 MONITOR_CTRL1 Register (Offset = 467h) [Reset = 0012h]

MONITOR_CTRL1 is shown in Figure 7-67 and described in Table 7-71.

Return to the Table 7-23.

Figure 7-67. MONITOR_CTRL1 Register

15	14	13	12	11	10	9	8
cfg_dc_offset_2c							
R/W-0h							
7	6	5	4	3	2	1	0
cfg_cic_gain12_arith		cfg_cic_gain2			cfg_cic_gain1		
R/W-0h		R/W-2h			R/W-2h		

Table 7-71. MONITOR_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	cfg_dc_offset_2c	R/W	0h	Analog control
7-6	cfg_cic_gain12_arith	R/W	0h	Analog control
5-3	cfg_cic_gain2	R/W	2h	Analog control
2-0	cfg_cic_gain1	R/W	2h	Analog control

7.6.2.49 MONITOR_CTRL2 Register (Offset = 468h) [Reset = 0920h]

MONITOR_CTRL2 is shown in Figure 7-68 and described in Table 7-72.

Return to the Table 7-23.

Figure 7-68. MONITOR_CTRL2 Register

15	14	13	12	11	10	9	8
cfg_bypass_reset_sensor_val	cfg_rd_data			cfg_dec_factor_sensors			cfg_dec_factor_gain_calib
R/W-0h	R/W-0h			R/W-4h			R/W-4h
7	6	5	4	3	2	1	0
cfg_dec_factor_gain_calib		cfg_dec_factor_dc_calib			cfg_bypass_sel_num		
R/W-4h		R/W-4h			R/W-0h		

Table 7-72. MONITOR_CTRL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	cfg_bypass_reset_sensor_val	R/W	0h	When cfg_bypass_fsm is 1, use this register to keep sensor in reset
14-12	cfg_rd_data	R/W	0h	To read out monitor adc output through MDIO for debug
11-9	cfg_dec_factor_sensors	R/W	4h	Analog control
8-6	cfg_dec_factor_gain_calib	R/W	4h	Analog control
5-3	cfg_dec_factor_dc_calib	R/W	4h	Analog control
2-0	cfg_bypass_sel_num	R/W	0h	When cfg_bypass_fsm is 1, use this register to select the sensor

7.6.2.50 MONITOR_CTRL4 Register (Offset = 46Ah) [Reset = 0094h]

MONITOR_CTRL4 is shown in Figure 7-69 and described in Table 7-73.

Return to the Table 7-23.

Figure 7-69. MONITOR_CTRL4 Register

15	14	13	12	11	10	9	8
RESERVED							cfg_hist_clr
R-0h							R/W-0h
7	6	5	4	3	2	1	0
cfg_discard_sample_num	cfg_avg_sample_num	cfg_adc_clk_div		cfg_force_start	cfg_reset	periodic	start
R/W-1h	R/W-0h	R/W-1h		R/W-0h	R/W-1h	R/W-0h	R/WSC-0h

Table 7-73. MONITOR_CTRL4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	RESERVED	R	0h	RESERVED
8	cfg_hist_clr	R/W	0h	CFG_HIST_CLR
7	cfg_discard_sample_num	R/W	1h	Number of samples to be discarded before starting averaging - 0b = 2 samples 1b = 4 samples
6	cfg_avg_sample_num	R/W	0h	Number of samples for calculating the average before storing in history - 0b = 2 samples 1b = 4 samples
5-4	cfg_adc_clk_div	R/W	1h	Config options to select frequency of monitor adc clock - 00b = 12.5MHz 01b = 6.25MHz 10b = 3.125MHz 11b = Reserved
3	cfg_force_start	R/W	0h	Set to force start sensor monitor FSM even if link is not established
2	cfg_reset	R/W	1h	0b = Enable the monitor 1b = Monitor is held in reset state At any point of time, if the signal is changed to 1, the module abruptly goes to reset state
1	periodic	R/W	0h	0b = Monitor is enabled only when start is set for one iteration 1b = Monitor is enabled for periodic iteration
0	start	R/WSC	0h	Start indication for sensor monitor FSM, self clearing

7.6.2.51 MONITOR_STAT1 Register (Offset = 47Bh) [Reset = 0000h]

MONITOR_STAT1 is shown in Figure 7-70 and described in Table 7-74.

Return to the Table 7-23.

Figure 7-70. MONITOR_STAT1 Register

15	14	13	12	11	10	9	8
stat_rd_data							
R-0h							
7	6	5	4	3	2	1	0
stat_rd_data							
R-0h							

Table 7-74. MONITOR_STAT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	stat_rd_data	R	0h	STAT_RD_DATA

7.6.2.52 BREAK_LINK_TIMER Register (Offset = 50Ah) [Reset = 112Eh]

BREAK_LINK_TIMER is shown in Figure 7-71 and described in Table 7-75.

Return to the Table 7-23.

Figure 7-71. BREAK_LINK_TIMER Register

15	14	13	12	11	10	9	8
RESERVED		RESERVED	cfg_fifo_reset_in_break_link	cfg_slave_send_s_32_mode	RESERVED		
R/W-0h		R/W-0h	R/W-1h	R/W-0h	R/W-12Eh		
7	6	5	4	3	2	1	0
RESERVED							
R/W-12Eh							

Table 7-75. BREAK_LINK_TIMER Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	RESERVED	R/W	0h	Reserved
13	RESERVED	R/W	0h	Reserved
12	cfg_fifo_reset_in_break_link	R/W	1h	Allow ADC FIFO to be in reset during break link timer
11	cfg_slave_send_s_32_mode	R/W	0h	Enable mode where Slave PHY sends SEND_S signalling for a fixed 32 times once it has detected SEND_S Note : Should be enabled only if 0x509[10] is not set 0h = Follow IEEE state machine 1h = Enable slave to send SEND_S 32 times
10-0	RESERVED	R/W	12Eh	Reserved

7.6.2.53 RS_DECODER Register (Offset = 510h) [Reset = 2D50h]

RS_DECODER is shown in Figure 7-72 and described in Table 7-76.

Return to the Table 7-23.

Figure 7-72. RS_DECODER Register

15	14	13	12	11	10	9	8
cfg_rs_decoder_bypass	RESERVED	RESERVED					
R/W-0h	R/W-0h	R/W-2Dh					
7	6	5	4	3	2	1	0
RESERVED							RESERVED
R/W-28h							R/W-0h

Table 7-76. RS_DECODER Register Field Descriptions

Bit	Field	Type	Reset	Description
15	cfg_rs_decoder_bypass	R/W	0h	Bypass RS decoder 0h = RS decoder in use 1h = Bypass RS decoder
14	RESERVED	R/W	0h	Reserved
13-8	RESERVED	R/W	2Dh	Reserved
7-1	RESERVED	R/W	28h	Reserved
0	RESERVED	R/W	0h	Reserved

7.6.2.54 LPS_CONTROL_1 Register (Offset = 514h) [Reset = 08E3h]

LPS_CONTROL_1 is shown in Figure 7-73 and described in Table 7-77.

Return to the Table 7-23.

Figure 7-73. LPS_CONTROL_1 Register

15	14	13	12	11	10	9	8
RESERVED				cfg_tx_wake_cg			cfg_tx_sleep_cg
R-0h				R/W-4h			R/W-3h
7	6	5	4	3	2	1	0
cfg_tx_sleep_cg		cfg_rx_wake_cg			cfg_rx_sleep_cg		
R/W-3h		R/W-4h			R/W-3h		

Table 7-77. LPS_CONTROL_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	RESERVED	R	0h	Reserved
11-9	cfg_tx_wake_cg	R/W	4h	Control code to send on Tx for wake indication
8-6	cfg_tx_sleep_cg	R/W	3h	Control code to send on Tx for sleep indication
5-3	cfg_rx_wake_cg	R/W	4h	Control code to expect on Rx for wake indication
2-0	cfg_rx_sleep_cg	R/W	3h	Control code to expect on Rx for sleep indication

7.6.2.55 LPS_CONTROL_2 Register (Offset = 515h) [Reset = 0808h]

LPS_CONTROL_2 is shown in Figure 7-74 and described in Table 7-78.

Return to the Table 7-23.

Figure 7-74. LPS_CONTROL_2 Register

15	14	13	12	11	10	9	8
RESERVED	cfg_wake_cg_cnt_th						
R-0h	R/W-8h						
7	6	5	4	3	2	1	0
RESERVED	cfg_sleep_cg_cnt_th						
R-0h	R/W-8h						

Table 7-78. LPS_CONTROL_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	Reserved
14-8	cfg_wake_cg_cnt_th	R/W	8h	Number of continuous expected wake code groups required to acknowledge and set LPS wake command received.
7	RESERVED	R	0h	Reserved
6-0	cfg_sleep_cg_cnt_th	R/W	8h	Number of continuous expected sleep code groups required to acknowledge and set LPS sleep command received.

7.6.2.56 MAXWAIT_TIMER Register (Offset = 518h) [Reset = 17CEh]

MAXWAIT_TIMER is shown in Figure 7-75 and described in Table 7-79.

Return to the Table 7-23.

Figure 7-75. MAXWAIT_TIMER Register

15	14	13	12	11	10	9	8
cfg_maxwait_timer_init							
R/W-17CEh							
7	6	5	4	3	2	1	0
cfg_maxwait_timer_init							
R/W-17CEh							

Table 7-79. MAXWAIT_TIMER Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	cfg_maxwait_timer_init	R/W	17CEh	Maxwait timer (used during link-up) : value in us = decimal value multipled by 16

7.6.2.57 PHY_CTRL_1G Register (Offset = 519h) [Reset = 003Dh]

PHY_CTRL_1G is shown in Figure 7-76 and described in Table 7-80.

Return to the Table 7-23.

Figure 7-76. PHY_CTRL_1G Register

15	14	13	12	11	10	9	8
RESERVED	RESERVED	RESERVED	RESERVED	cfg_force_link_stat_val	cfg_force_link_stat	RESERVED	RESERVED
R-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
cfg_minwait_timer_init							
R/W-3Dh							

Table 7-80. PHY_CTRL_1G Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	Reserved
14	RESERVED	R/W	0h	Reserved
13	RESERVED	R/W	0h	Reserved
12	RESERVED	R/W	0h	Reserved
11	cfg_force_link_stat_val	R/W	0h	Forced link status value Valid only if 0x519[10] is set
10	cfg_force_link_stat	R/W	0h	Enable forcing link status value
9	RESERVED	R/W	0h	Reserved
8	RESERVED	R/W	0h	Reserved
7-0	cfg_minwait_timer_init	R/W	3Dh	Minwait timer (used during link-up) : value in us = decimal value multipled by 16

7.6.2.58 TEST_MODE Register (Offset = 531h) [Reset = 0000h]

TEST_MODE is shown in Figure 7-77 and described in Table 7-81.

Return to the Table 7-23.

Figure 7-77. TEST_MODE Register

15	14	13	12	11	10	9	8
RESERVED							cfg_test_mode4_tx_order
R-0h							R/W-0h
7	6	5	4	3	2	1	0
cfg_test_mode_7_data							
R/W-0h							

Table 7-81. TEST_MODE Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	RESERVED	R	0h	Reserved
8	cfg_test_mode4_tx_order	R/W	0h	Order of symbols to be transmitted in Test mode 4 0h = T1 followed by T2 1h = T2 followed by T1
7-0	cfg_test_mode_7_data	R/W	0h	GMII data to transmit in Test mode 7

7.6.2.59 LINK_QUAL_1 Register (Offset = 543h) [Reset = 0000h]

LINK_QUAL_1 is shown in Figure 7-78 and described in Table 7-82.

Return to the Table 7-23.

Figure 7-78. LINK_QUAL_1 Register

15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
link_training_time							
R-0h							

Table 7-82. LINK_QUAL_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R	0h	Reserved
7-0	link_training_time	R	0h	Link training time in ms (TC12)

7.6.2.60 LINK_QUAL_2 Register (Offset = 544h) [Reset = 0000h]

LINK_QUAL_2 is shown in Figure 7-79 and described in Table 7-83.

Return to the Table 7-23.

Figure 7-79. LINK_QUAL_2 Register

15	14	13	12	11	10	9	8
remote_receiver_time							
R-0h							
7	6	5	4	3	2	1	0
local_receiver_time							
R-0h							

Table 7-83. LINK_QUAL_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	remote_receiver_time	R	0h	Remote receiver time in ms (TC12)
7-0	local_receiver_time	R	0h	Local receiver time in ms (TC12)

7.6.2.61 LINK_DOWN_LATCH_STAT Register (Offset = 545h) [Reset = 0000h]

LINK_DOWN_LATCH_STAT is shown in Figure 7-80 and described in Table 7-84.

Return to the Table 7-23.

Figure 7-80. LINK_DOWN_LATCH_STAT Register

15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED		channel_ok_ll	link_fail_inhibit_lh	send_s_sigdet_lh	hi_rfer_lh	block_lock_ll	pma_watchdog_ll
R-0h		R/W0C-0h	R/W0C-0h	R/W0C-0h	R/W0C-0h	R/W0S-0h	R/W0S-0h

Table 7-84. LINK_DOWN_LATCH_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
15-6	RESERVED	R	0h	Reserved
5	channel_ok_ll	R/W0C	0h	1b = Channel ok was never de-asserted 0b = Channel ok was de-asserted
4	link_fail_inhibit_lh	R/W0C	0h	1b = Link fail inhibit assertion was reported 0b = Link fail inhibit assertion was never reported
3	send_s_sigdet_lh	R/W0C	0h	1b = Send s sigdet assertion was reported 0b = Send s sigdet assertion was never reported
2	hi_rfer_lh	R/W0C	0h	1b = High ri rfer assertion was reported 0b = High ri rfer assertion was never reported
1	block_lock_ll	R/W0S	0h	1b = Block lock de-assertion was never reported 0b = Block lock de-assertion was never reported
0	pma_watchdog_ll	R/W0S	0h	1b = Low pma watchdog was never reported 0b = Low pma watchdof was reported

7.6.2.62 LINK_QUAL_3 Register (Offset = 547h) [Reset = 0000h]

LINK_QUAL_3 is shown in Figure 7-81 and described in Table 7-85.

Return to the Table 7-23.

Figure 7-81. LINK_QUAL_3 Register

15	14	13	12	11	10	9	8
link_loss_cnt						link_fail_cnt	
R-0h						R-0h	
7	6	5	4	3	2	1	0
link_fail_cnt							
R-0h							

Table 7-85. LINK_QUAL_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-10	link_loss_cnt	R	0h	Link loss count since last power cycle (TC12)
9-0	link_fail_cnt	R	0h	Link fail without link loss count since last power cycle (TC12)

7.6.2.63 LINK_QUAL_4 Register (Offset = 548h) [Reset = 0000h]

LINK_QUAL_4 is shown in Figure 7-82 and described in Table 7-86.

Return to the Table 7-23.

Figure 7-82. LINK_QUAL_4 Register

15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							comm_ready
R-0h							R-0h

Table 7-86. LINK_QUAL_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-1	RESERVED	R	0h	Reserved
0	comm_ready	R	0h	Communication ready status (TC12)

7.6.2.64 RS_DECODER_FRAME_STAT_2 Register (Offset = 552h) [Reset = 0000h]

RS_DECODER_FRAME_STAT_2 is shown in Figure 7-83 and described in Table 7-87.

Return to the Table 7-23.

Figure 7-83. RS_DECODER_FRAME_STAT_2 Register

15	14	13	12	11	10	9	8
rs_dec_uncorr_frame_cnt							
0h							
7	6	5	4	3	2	1	0
rs_dec_uncorr_frame_cnt							
0h							

Table 7-87. RS_DECODER_FRAME_STAT_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	rs_dec_uncorr_frame_cnt		0h	No of uncorrectable RS frames received at RS decoder, clear on read, saturates

7.6.2.65 PMA_WATCHDOG Register (Offset = 559h) [Reset = 0051h]

PMA_WATCHDOG is shown in Figure 7-84 and described in Table 7-88.

Return to the Table 7-23.

Figure 7-84. PMA_WATCHDOG Register

15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED	cfg_pma_watchdog_force_val	cfg_pma_watchdog_force_en	cfg_ieee_watchdog_en	cfg_watchdog_cnt_clr_th			
R-0h	R/W-1h	R/W-0h	R/W-1h	R/W-1h			

Table 7-88. PMA_WATCHDOG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-7	RESERVED	R	0h	Reserved
6	cfg_pma_watchdog_force_val	R/W	1h	Force value for pma watchdog
5	cfg_pma_watchdog_force_en	R/W	0h	Enable forcing pma watchdog
4	cfg_ieee_watchdog_en	R/W	1h	1 : watchdog counters are started after link up 0: TBD
3-0	cfg_watchdog_cnt_clr_th	R/W	1h	Number of 0, +1, -1 symbols to be seen in their respective watchdog counter window to prevent them for asserting pma_watchdog_status

7.6.2.66 SYMB_POL_CFG Register (Offset = 55Bh) [Reset = 0000h]

SYMB_POL_CFG is shown in Figure 7-85 and described in Table 7-89.

Return to the Table 7-23.

Figure 7-85. SYMB_POL_CFG Register

15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED			cfg_slave_auto_pol_correction_en	cfg_rx_symb_order_inv	cfg_rx_symb_pol_inv	cfg_tx_symb_order_inv	cfg_tx_symb_pol_inv
R-0h			R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 7-89. SYMB_POL_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-5	RESERVED	R	0h	Reserved
4	cfg_slave_auto_pol_correction_en	R/W	0h	Correct tx polarity for slave based on received polarity 0h = Slave tx polarity independent of slave rx polarity 1h = Slave tx polarity to match received polarity
3	cfg_rx_symb_order_inv	R/W	0h	Order of received symbols S0 to S6 reversed to S6 to S0 Valid only if LPs 0x55B[1] is set (TI-TI link) 0h = Order of received symbols S0 to S6 unchanged 1h = Order of received symbols S0 to S6 reversed to S6 to S0
2	cfg_rx_symb_pol_inv	R/W	0h	Invert polarity of received symbols 0h = Unchanged polarity of received symbols 1h = Invert polarity of received symbols
1	cfg_tx_symb_order_inv	R/W	0h	Order of transmit symbols S0 to S6 reversed to S6 to S0 Valid only if LPs 0x55B[3] is set (TI-TI link) 0h = Order of transmit symbols S0 to S6 unchanged 1h = Order of transmit symbols S0 to S6 reversed to S6 to S0
0	cfg_tx_symb_pol_inv	R/W	0h	Invert polarity of transmit symbols 0h = Unchanged polarity of transmit symbols 1h = Invert polarity of transmit symbols

7.6.2.67 OAM_CFG Register (Offset = 55Ch) [Reset = 0000h]

OAM_CFG is shown in Figure 7-86 and described in Table 7-90.

Return to the Table 7-23.

Figure 7-86. OAM_CFG Register

15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED						cfg_rx_oam_crc_data_in_order	cfg_tx_oam_crc_data_in_order
R-0h						R/W-0h	R/W-0h

Table 7-90. OAM_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-2	RESERVED	R	0h	Reserved
1	cfg_rx_oam_crc_data_in_order	R/W	0h	Reverse order of data input to CRC checker in rx oam to MSB first 0h = Order of data input to CRC checker in rx oam is LSB first 1h = Order of data input to CRC checker in rx oam is MSB first
0	cfg_tx_oam_crc_data_in_order	R/W	0h	Reverse order of data input to CRC calculator in tx oam to MSB first 0h = Order of data input to CRC calculator in tx oam is LSB first 1h = Order of data input to CRC calculator in tx oam is MSB first

7.6.2.68 TEST_MEM_CFG Register (Offset = 561h) [Reset = 17A0h]

TEST_MEM_CFG is shown in Figure 7-87 and described in Table 7-91.

Return to the Table 7-23.

Figure 7-87. TEST_MEM_CFG Register

15	14	13	12	11	10	9	8
RESERVED			cfg_wait_time_xcorr_wen				
R-0h			R/W-5Eh				
7	6	5	4	3	2	1	0
cfg_wait_time_xcorr_wen		cfg_xcorr_dbg_sel	cfg_send_s_infinite_loop	cfg_xcorr_dbg_test_mem	cfg_ecc_en	cfg_test_mem_sigdet_debug	cfg_pcs_test_mem_mode
R/W-5Eh		R/W-1h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 7-91. TEST_MEM_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-13	RESERVED	R	0h	Reserved
12-6	cfg_wait_time_xcorr_wen	R/W	5Eh	Wait timer after TX_SEND_S after which testmem is written on energy fall Note : Valid only if 0x561[3] is set
5	cfg_xcorr_dbg_sel	R/W	1h	0b = Select xcorr from aligned detector to write to test mem 1b = Select xcorr from shifted detector to write to test mem Note : Valid only if 0x561[3] is set
4	cfg_send_s_infinite_loop	R/W	0h	enable transmitting infinite send_s sequence. For send_s debug. Valid only in master and when 0x56A[15] is set. 0h = disable infinte send_s mode 1h = enable infinite send_s mode
3	cfg_xcorr_dbg_test_mem	R/W	0h	enabled xcorr debug for send_s. Valid only if 0x561[0] is 1b0 0h = Normal send_s debug. Refer to 0x561[1] 1h = Enabled xcorr debug
2	cfg_ecc_en	R/W	0h	Enable ECC logic for RS decoder memory 0h = ECC encoding/decoding is disabled 1h = ECC encoding/decoding is enabled
1	cfg_test_mem_sigdet_debug	R/W	0h	Enable sidget debug mode in test mem send s mode Valid only if 0x561[0] is 1b0 0h = Test mem written in send s mode only on state transition 1h = Enable sigdet debug mode in test mem send s mode
0	cfg_pcs_test_mem_mode	R/W	0h	Choose send s or train rx test mem mode 0h = Send s info on test mem 1h = Train rx info on test mem

7.6.2.69 FORCE_CTRL1 Register (Offset = 573h) [Reset = 0000h]

FORCE_CTRL1 is shown in Figure 7-88 and described in Table 7-92.

Return to the Table 7-23.

Figure 7-88. FORCE_CTRL1 Register

15	14	13	12	11	10	9	8
RESERVED							cfg_force_link_sync_state_en
R-0h							R/W-0h
7	6	5	4	3	2	1	0
cfg_force_link_sync_state_val							
R/W-0h							

Table 7-92. FORCE_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	RESERVED	R	0h	Reserved
8	cfg_force_link_sync_state_en	R/W	0h	Force link sync state enable
7-0	cfg_force_link_sync_state_val	R/W	0h	Force link sync state value

7.6.2.70 RGMII_CTRL Register (Offset = 600h) [Reset = 0120h]

RGMII_CTRL is shown in Figure 7-89 and described in Table 7-93.

Return to the Table 7-23.

Figure 7-89. RGMII_CTRL Register

15	14	13	12	11	10	9	8
RESERVED						rgmii_rx_half_full_th	
R-0h						R/W-2h	
7	6	5	4	3	2	1	0
rgmii_rx_half_full_th	rgmii_tx_half_full_th			rgmii_tx_if_en	invert_rgmii_txd	invert_rgmii_rxd	sup_tx_err_fd
R/W-2h	R/W-2h			R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 7-93. RGMII_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
15-10	RESERVED	R	0h	Reserved
9-7	rgmii_rx_half_full_th	R/W	2h	RGMII RX sync FIFO half full threshold
6-4	rgmii_tx_half_full_th	R/W	2h	RGMII TX sync FIFO half full threshold
3	rgmii_tx_if_en	R/W	0h	RGMII enable bit Default from strap 0h = RGMII disable 1h = RGMII enable
2	invert_rgmii_txd	R/W	0h	Invert RGMII Tx wire order - full swap [3:0] to [0:3] 0h = Keep RGMII Tx wire order same - [3: 1h = Invert RGMII Tx wire order - [3:
1	invert_rgmii_rxd	R/W	0h	Invert RGMII Rx wire order - full swap [3:0] to [0:3] 0h = Keep RGMII Rx wire order same - [3: 1h = Invert RGMII Rx wire order - [3:
0	sup_tx_err_fd	R/W	0h	1: suppress tx_err in full duplex mode when tx_en set to zero 0: allow tx_err assertion to PHY when tx_en set to zero (this bit can disable the TX_ERR indication input)

7.6.2.71 RGMII_FIFO_STATUS Register (Offset = 601h) [Reset = 0000h]

RGMII_FIFO_STATUS is shown in Figure 7-90 and described in Table 7-94.

Return to the Table 7-23.

Figure 7-90. RGMII_FIFO_STATUS Register

15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED				rgmii_rx_af_full_err	rgmii_rx_af_empty_err	rgmii_tx_af_full_err	rgmii_tx_af_empty_err
R-0h				R/W0C-0h	R/W0C-0h	R/W0C-0h	R/W0C-0h

Table 7-94. RGMII_FIFO_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15-4	RESERVED	R	0h	Reserved
3	rgmii_rx_af_full_err	R/W0C	0h	RGMII RX fifo full error 0h = No empty fifo error 1h = RGMII TX full error has been indicated
2	rgmii_rx_af_empty_err	R/W0C	0h	RGMII RX fifo empty error 0h = No empty fifo error 1h = RGMII RX empty error has been indicated
1	rgmii_tx_af_full_err	R/W0C	0h	RGMII TX fifo full error 0h = No empty fifo error 1h = RGMII TX full error has been indicated
0	rgmii_tx_af_empty_err	R/W0C	0h	RGMII TX fifo empty error 0h = No empty fifo error 1h = RGMII TX empty error has been indicated

7.6.2.72 RGMII_DELAY_CTRL Register (Offset = 602h) [Reset = 0000h]

RGMII_DELAY_CTRL is shown in Figure 7-91 and described in Table 7-95.

Return to the Table 7-23.

Figure 7-91. RGMII_DELAY_CTRL Register

15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED						rx_clk_sel	tx_clk_sel
R-0h						R/W-0h	R/W-0h

Table 7-95. RGMII_DELAY_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
15-2	RESERVED	R	0h	Reserved
1	rx_clk_sel	R/W	0h	In RGMII mode, Enable or disable the internal delay for RXD wrt RX_CLK (use this mode when RGMII_RX_CLK and RGMII_RXD are aligned). The delay magnitude can be configured by programming register 0x430[7:4] 0h = clock and data are aligned 1h = clock on PIN is delayed by 90 degrees relative to RGMII_RX data
0	tx_clk_sel	R/W	0h	In RGMII mode, Enable or disable the internal delay for TXD wrt TX_CLK (use this mode when RGMII_TX_CLK and RGMII_TXD are aligned). The delay magnitude can be configured by programming register 0x430[11:8] 0h = clock and data are aligned 1h = clock is internally delayed by 90 degrees

7.6.2.73 SGMII_CTRL_1 Register (Offset = 608h) [Reset = 007Bh]

SGMII_CTRL_1 is shown in Figure 7-92 and described in Table 7-96.

Return to the Table 7-23.

Figure 7-92. SGMII_CTRL_1 Register

15	14	13	12	11	10	9	8
sgmii_tx_err_dis	cfg_align_idx_force	cfg_align_idx_value				cfg_sgmii_en	cfg_sgmii_rx_pol_invert
R/W-0h	R/W-0h	R/W-0h				R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
cfg_sgmii_tx_pol_invert	RESERVED		RESERVED	RESERVED	sgmii_autoneg_timer		mr_an_enable
R/W-0h	R/W-3h		R/W-1h	R/W-1h	R/W-1h		R/W-1h

Table 7-96. SGMII_CTRL_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	sgmii_tx_err_dis	R/W	0h	1 = Disable SGMII TX Error indication 0 = Enable SGMII TX Error indication
14	cfg_align_idx_force	R/W	0h	Force word boundray index selection
13-10	cfg_align_idx_value	R/W	0h	when cfg_align_idx_force = 1 This value set the iword boundray index
9	cfg_sgmii_en	R/W	0h	SGMII enable bit Default from strap 0h = SGMII disable 1h = SGMII enable
8	cfg_sgmii_rx_pol_invert	R/W	0h	SGMII RX bus invert polarity 0h = Polarity not inverted 1h = SGMII RX bus invert polarity
7	cfg_sgmii_tx_pol_invert	R/W	0h	SGMII TX bus invert polarity 0h = Polarity not inverted 1h = SGMII TX bus invert polarity
6-5	RESERVED	R/W	3h	Reserved
4	RESERVED	R/W	1h	Reserved
3	RESERVED	R/W	1h	Reserved
2-1	sgmii_autoneg_timer	R/W	1h	Selects duration of SGMII Auto-Negotiation timer: 00: 1.6ms 01: 2us 10: 800us 11: 11ms
0	mr_an_enable	R/W	1h	1 = Enable SGMII Auto-Negotaition 0 = Disable SGMII Auto-Negotiation

7.6.2.74 SGMII_STATUS Register (Offset = 60Ah) [Reset = 0000h]

SGMII_STATUS is shown in Figure 7-93 and described in Table 7-97.

Return to the Table 7-23.

Figure 7-93. SGMII_STATUS Register

15	14	13	12	11	10	9	8
RESERVED			sgmii_page_received	link_status_1000bx	mr_an_complete	cfg_align_en	cfg_sync_status
R-0h			R-0h	R-0h	R-0h	R-0h	R-0h
7	6	5	4	3	2	1	0
cfg_align_idx				cfg_state			
R-0h				R-0h			

Table 7-97. SGMII_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15-13	RESERVED	R	0h	Reserved
12	sgmii_page_received	R	0h	Indicates that a new auto neg page was received 0h = No new auto neg page received 1h = A new auto neg page received
11	link_status_1000bx	R	0h	sgmii link status 0h = SGMII link down 1h = SGMII link up
10	mr_an_complete	R	0h	sgmii autoneg complete indication 0h = SGMII autoneg not completed 1h = SGMII autoneg completed
9	cfg_align_en	R	0h	word boundary FSM - align indication
8	cfg_sync_status	R	0h	word boundary FSM - sync status indication 0h = sync not achieved 1h = sync achieved
7-4	cfg_align_idx	R	0h	word boundary index selection
3-0	cfg_state	R	0h	word boundary FSM state

7.6.2.75 SGMII_CTRL_2 Register (Offset = 60Ch) [Reset = 001Bh]

SGMII_CTRL_2 is shown in Figure 7-94 and described in Table 7-98.

Return to the Table 7-23.

Figure 7-94. SGMII_CTRL_2 Register

15	14	13	12	11	10	9	8
RESERVED							sgmii_signal_detect_force_val
R-0h							R/W-0h
7	6	5	4	3	2	1	0
sgmii_signal_detect_force_en	mr_restart_an	tx_half_full_th			rx_half_full_th		
R/W-0h	R/WSC,0-0h	R/W-3h			R/W-3h		

Table 7-98. SGMII_CTRL_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	RESERVED	R	0h	Reserved
8	sgmii_signal_detect_force_val	R/W	0h	SGMII cdr lock force value
7	sgmii_signal_detect_force_en	R/W	0h	SGMII cdr lock force enable
6	mr_restart_an	R/WSC,0	0h	Restart sgmii autonegotiation
5-3	tx_half_full_th	R/W	3h	SGMII TX sync FIFO half full threshold
2-0	rx_half_full_th	R/W	3h	SGMII RX sync FIFO half full threshold

7.6.2.76 SGMII_FIFO_STATUS Register (Offset = 60Dh) [Reset = 0000h]

SGMII_FIFO_STATUS is shown in Figure 7-95 and described in Table 7-99.

Return to the Table 7-23.

Figure 7-95. SGMII_FIFO_STATUS Register

15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED				sgmii_rx_af_full_err	sgmii_rx_af_empty_err	sgmii_tx_af_full_err	sgmii_tx_af_empty_err
R-0h				R/W0C-0h	R/W0C-0h	R/W0C-0h	R/W0C-0h

Table 7-99. SGMII_FIFO_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15-4	RESERVED	R	0h	Reserved
3	sgmii_rx_af_full_err	R/W0C	0h	SGMII RX fifo full error 0h = No error indication 1h = SGMII RX fifo full error has been indicated
2	sgmii_rx_af_empty_err	R/W0C	0h	SGMII RX fifo empty error 0h = No error indication 1h = SGMII RX fifo empty error has been indicated
1	sgmii_tx_af_full_err	R/W0C	0h	SGMII TX fifo full error 0h = No error indication 1h = SGMII TX fifo full error has been indicated
0	sgmii_tx_af_empty_err	R/W0C	0h	SGMII TX fifo empty error 0h = No error indication 1h = SGMII TX fifo empty error has been indicated

7.6.2.77 PRBS_STATUS_1 Register (Offset = 618h) [Reset = 0000h]

PRBS_STATUS_1 is shown in Figure 7-96 and described in Table 7-100.

Return to the Table 7-23.

Figure 7-96. PRBS_STATUS_1 Register

15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
prbs_err_ov_cnt							
R-0h							

Table 7-100. PRBS_STATUS_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R	0h	Reserved
7-0	prbs_err_ov_cnt	R	0h	Holds number of error counter overflow that received by the PRBS checker. Value in this register is locked when write is done to register prbs_status_6 bit[0] or bit[1]. Counter stops on 0xFF. Note: when PRBS counters work in single mode, overflow counter is not active

7.6.2.78 PRBS_CTRL_1 Register (Offset = 619h) [Reset = 0574h]

PRBS_CTRL_1 is shown in Figure 7-97 and described in Table 7-101.

Return to the Table 7-23.

Figure 7-97. PRBS_CTRL_1 Register

15	14	13	12	11	10	9	8
RESERVED		cfg_pkt_gen_64	send_pkt	RESERVED	cfg_prbs_chk_sel		
R-0h		R/W-0h	R/WMC,0-0h	R-0h	R/W-5h		
7	6	5	4	3	2	1	0
RESERVED	cfg_prbs_gen_sel			cfg_prbs_cnt_mode	cfg_prbs_chk_enable	cfg_pkt_gen_prbs	pkt_gen_en
R-0h	R/W-7h			R/W-0h	R/W-1h	R/W-0h	R/W-0h

Table 7-101. PRBS_CTRL_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	RESERVED	R	0h	Reserved
13	cfg_pkt_gen_64	R/W	0h	Reserved
12	send_pkt	R/WMC,0	0h	Enables generating MAC packet with fix/incremental data w CRC (pkt_gen_en has to be set and cfg_pkt_gen_prbs has to be clear) Cleared automatically when pkt_done is set 0h = Stop MAC packet 1h = Transmit MAC packet w CRC
11	RESERVED	R	0h	Reserved
10-8	cfg_prbs_chk_sel	R/W	5h	000 : Checker receives from RGMII TX 001 : Checker receives SGMII TX 101 : Checker receives from Cu RX
7	RESERVED	R	0h	Reserved
6-4	cfg_prbs_gen_sel	R/W	7h	000 : PRBS transmits to RGMII RX 001 : PRBS transmits to SGMII RX 101 : PRBS transmits to Cu TX
3	cfg_prbs_cnt_mode	R/W	0h	1 = Continuous mode, when one of the PRBS counters reaches max value, pulse is generated and counter starts counting from zero again 0 = Single mode, When one of the PRBS counters reaches max value, PRBS checker stops counting.
2	cfg_prbs_chk_enable	R/W	1h	Enable PRBS checker xbar (to receive data) To be enabled for counters in 0x63C, 0x63D, 0x63E to work 0h = Disable PRBS checker 1h = Enable PRBS checker
1	cfg_pkt_gen_prbs	R/W	0h	If set: (1) When pkt_gen_en is set, PRBS packets are generated continuously (3) When pkt_gen_en is cleared, PRBS RX checker is still enabled If cleared: (1) When pkt_gen_en is set, non - PRBS packet is generated (3) When pkt_gen_en is cleared, PRBS RX checker is disabled as well 0h = Stop PRBS packet 1h = Transmit PRBS packet
0	pkt_gen_en	R/W	0h	1 = Enable packet/PRBS generator 0 = Disable packet/PRBS generator

7.6.2.79 PRBS_CTRL_2 Register (Offset = 61Ah) [Reset = 05DCh]

PRBS_CTRL_2 is shown in Figure 7-98 and described in Table 7-102.

Return to the Table 7-23.

Figure 7-98. PRBS_CTRL_2 Register

15	14	13	12	11	10	9	8
cfg_pkt_len_prbs							
R/W-5DCh							
7	6	5	4	3	2	1	0
cfg_pkt_len_prbs							
R/W-5DCh							

Table 7-102. PRBS_CTRL_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	cfg_pkt_len_prbs	R/W	5DCh	Length (in bytes) of PRBS packets and MAC packets w CRC

7.6.2.80 PRBS_CTRL_3 Register (Offset = 61Bh) [Reset = 007Dh]

PRBS_CTRL_3 is shown in Figure 7-99 and described in Table 7-103.

Return to the Table 7-23.

Figure 7-99. PRBS_CTRL_3 Register

15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
cfg_ipg_len							
R/W-7Dh							

Table 7-103. PRBS_CTRL_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R	0h	Reserved
7-0	cfg_ipg_len	R/W	7Dh	Inter-packet gap (in bytes) between packets

7.6.2.81 PRBS_STATUS_2 Register (Offset = 61Ch) [Reset = 0000h]

PRBS_STATUS_2 is shown in Figure 7-100 and described in Table 7-104.

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Figure 7-100. PRBS_STATUS_2 Register

15	14	13	12	11	10	9	8
prbs_byte_cnt							
R-0h							
7	6	5	4	3	2	1	0
prbs_byte_cnt							
R-0h							

Table 7-104. PRBS_STATUS_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	prbs_byte_cnt	R	0h	Holds number of total bytes that received by the PRBS checker. Value in this register is locked when write is done to register prbs_status_6 bit[0] or bit[1]. When PRBS Count Mode set to zero, count stops on 0xFFFF

7.6.2.82 PRBS_STATUS_3 Register (Offset = 61Dh) [Reset = 0000h]

PRBS_STATUS_3 is shown in Figure 7-101 and described in Table 7-105.

Return to the Table 7-23.

Figure 7-101. PRBS_STATUS_3 Register

15	14	13	12	11	10	9	8
prbs_pkt_cnt_15_0							
R-0h							
7	6	5	4	3	2	1	0
prbs_pkt_cnt_15_0							
R-0h							

Table 7-105. PRBS_STATUS_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	prbs_pkt_cnt_15_0	R	0h	Bits [15:0] of number of total packets received by the PRBS checker Value in this register is locked when write is done to register prbs_status_6 bit[0] or bit[1]. When PRBS Count Mode set to zero, count stops on 0xFFFFFFFF

7.6.2.83 PRBS_STATUS_4 Register (Offset = 61Eh) [Reset = 0000h]

PRBS_STATUS_4 is shown in Figure 7-102 and described in Table 7-106.

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Figure 7-102. PRBS_STATUS_4 Register

15	14	13	12	11	10	9	8
prbs_pkt_cnt_31_16							
R-0h							
7	6	5	4	3	2	1	0
prbs_pkt_cnt_31_16							
R-0h							

Table 7-106. PRBS_STATUS_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	prbs_pkt_cnt_31_16	R	0h	Bits [31:16] of number of total packets received by the PRBS checker Value in this register is locked when write is done to register prbs_status_6 bit[0] or bit[1]. When PRBS Count Mode set to zero, count stops on 0xFFFFFFFF

7.6.2.84 PRBS_STATUS_6 Register (Offset = 620h) [Reset = 0000h]

PRBS_STATUS_6 is shown in Figure 7-103 and described in Table 7-107.

Return to the Table 7-23.

Figure 7-103. PRBS_STATUS_6 Register

15	14	13	12	11	10	9	8
RESERVED			pkt_done	pkt_gen_busy	prbs_pkt_ov	prbs_byte_ov	prbs_lock
R-0h			R-0h	R-0h	R-0h	R-0h	R-0h
7	6	5	4	3	2	1	0
prbs_err_cnt							
R-0h							

Table 7-107. PRBS_STATUS_6 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-13	RESERVED	R	0h	Reserved
12	pkt_done	R	0h	Set when all MAC packets w CRC are transmitted 0h = MAC packet transmission in progress 1h = MAC packets transmission completed
11	pkt_gen_busy	R	0h	1 = Packet generator is in process 0 = Packet generator is not in process
10	prbs_pkt_ov	R	0h	If set, packet counter reached overflow Overflow is cleared when PRBS counters are cleared - done by setting bit #1 of prbs_status_6 0h = No overflow 1h = Packet counter overflow
9	prbs_byte_ov	R	0h	If set, bytes counter reached overflow Overflow is cleared when PRBS counters are cleared - done by setting bit #1of prbs_status_6 0h = No overflow 1h = byte counter overflow
8	prbs_lock	R	0h	1 = PRBS checker is locked sync) on received byte stream 0 = PRBS checker is not locked 0h = PRBS checker is not locked 1h = PRBS checker is locked sync) on received byte stream
7-0	prbs_err_cnt	R	0h	Holds number of errored bits received by the PRBS checker Value in this register is locked when write is done to bit[0] or bit[1] When PRBS Count Mode set to zero, count stops on 0xFF Notes: Writing bit 0 generates a lock signal for the PRBS counters. Writing bit 1 generates a lock and clear signal for the PRBS counters

7.6.2.85 PRBS_STATUS_8 Register (Offset = 622h) [Reset = 0000h]

PRBS_STATUS_8 is shown in Figure 7-104 and described in Table 7-108.

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Figure 7-104. PRBS_STATUS_8 Register

15	14	13	12	11	10	9	8
pkt_err_cnt_15_0							
R-0h							
7	6	5	4	3	2	1	0
pkt_err_cnt_15_0							
R-0h							

Table 7-108. PRBS_STATUS_8 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	pkt_err_cnt_15_0	R	0h	Bits [15:0] of number of total packets with error received by the PRBS checker Value in this register is locked when write is done to register prbs_status_6 bit[0] or bit[1]. When PRBS Count Mode set to zero, count stops on 0xFFFFFFFF

7.6.2.86 PRBS_STATUS_9 Register (Offset = 623h) [Reset = 0000h]

PRBS_STATUS_9 is shown in Figure 7-105 and described in Table 7-109.

Return to the Table 7-23.

Figure 7-105. PRBS_STATUS_9 Register

15	14	13	12	11	10	9	8
pkt_err_cnt_31_16							
R-0h							
7	6	5	4	3	2	1	0
pkt_err_cnt_31_16							
R-0h							

Table 7-109. PRBS_STATUS_9 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	pkt_err_cnt_31_16	R	0h	Bits [31:16] of number of total packets with error received by the PRBS checker Value in this register is locked when write is done to register prbs_status_6 bit[0] or bit[1]. When PRBS Count Mode set to zero, count stops on 0xFFFFFFFF

7.6.2.87 PRBS_CTRL_4 Register (Offset = 624h) [Reset = 5511h]

PRBS_CTRL_4 is shown in Figure 7-106 and described in Table 7-110.

Return to the Table 7-23.

Figure 7-106. PRBS_CTRL_4 Register

15	14	13	12	11	10	9	8
cfg_pkt_data							
R/W-55h							
7	6	5	4	3	2	1	0
cfg_pkt_mode		cfg_pattern_vld_bytes			cfg_pkt_cnt		
R/W-0h		R/W-2h			R/W-1h		

Table 7-110. PRBS_CTRL_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	cfg_pkt_data	R/W	55h	Fixed data to be sent in Fix data mode
7-6	cfg_pkt_mode	R/W	0h	2b00 - Incremental 2b01 - Fixed 2b1x - PRBS 0h = Incremental 1h = Fixed
5-3	cfg_pattern_vld_bytes	R/W	2h	Number of bytes of valid pattern in packet (Max - 6) 0h = 0 bytes 1h = 1 bytes 2h = 2 bytes 3h = 3 bytes 4h = 4 bytes 5h = 5 bytes 6h = 6 bytes 7h = 6 bytes
2-0	cfg_pkt_cnt	R/W	1h	000b = 1 packet 001b = 10 packets 010b = 100 packets 011b = 1000 packets 100b = 10000 packets 101b = 100000 packets 110b = 1000000 packets 111b = Continuous packets 0h = 1 packet 1h = 10 packets 2h = 100 packets 3h = 1000 packets 4h = 10000 packets 5h = 100000 packets 6h = 1000000 packets 7h = Continuous packets

7.6.2.88 PRBS_CTRL_5 Register (Offset = 625h) [Reset = 0000h]

PRBS_CTRL_5 is shown in Figure 7-107 and described in Table 7-111.

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Figure 7-107. PRBS_CTRL_5 Register

15	14	13	12	11	10	9	8
pattern_15_0							
R/W-0h							
7	6	5	4	3	2	1	0
pattern_15_0							
R/W-0h							

Table 7-111. PRBS_CTRL_5 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	pattern_15_0	R/W	0h	Bits 15:0 of pattern

7.6.2.89 PRBS_CTRL_6 Register (Offset = 626h) [Reset = 0000h]

PRBS_CTRL_6 is shown in Figure 7-108 and described in Table 7-112.

Return to the Table 7-23.

Figure 7-108. PRBS_CTRL_6 Register

15	14	13	12	11	10	9	8
pattern_31_16							
R/W-0h							
7	6	5	4	3	2	1	0
pattern_31_16							
R/W-0h							

Table 7-112. PRBS_CTRL_6 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	pattern_31_16	R/W	0h	Bits 31:16 of pattern

7.6.2.90 PRBS_CTRL_7 Register (Offset = 627h) [Reset = 0000h]

PRBS_CTRL_7 is shown in Figure 7-109 and described in Table 7-113.

Return to the Table 7-23.

Figure 7-109. PRBS_CTRL_7 Register

15	14	13	12	11	10	9	8
pattern_47_32							
R/W-0h							
7	6	5	4	3	2	1	0
pattern_47_32							
R/W-0h							

Table 7-113. PRBS_CTRL_7 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	pattern_47_32	R/W	0h	Bits 47:32 of pattern

7.6.2.91 PRBS_CTRL_8 Register (Offset = 628h) [Reset = 0000h]

PRBS_CTRL_8 is shown in Figure 7-110 and described in Table 7-114.

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Figure 7-110. PRBS_CTRL_8 Register

15	14	13	12	11	10	9	8
pmatch_data_15_0							
R/W-0h							
7	6	5	4	3	2	1	0
pmatch_data_15_0							
R/W-0h							

Table 7-114. PRBS_CTRL_8 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	pmatch_data_15_0	R/W	0h	Bits 15:0 of Perfect Match Data - used for DA (destination address) match

7.6.2.92 PRBS_CTRL_9 Register (Offset = 629h) [Reset = 0000h]

PRBS_CTRL_9 is shown in Figure 7-111 and described in Table 7-115.

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Figure 7-111. PRBS_CTRL_9 Register

15	14	13	12	11	10	9	8
pmatch_data_31_16							
R/W-0h							
7	6	5	4	3	2	1	0
pmatch_data_31_16							
R/W-0h							

Table 7-115. PRBS_CTRL_9 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	pmatch_data_31_16	R/W	0h	Bits 31:16 of Perfect Match Data - used for DA (destination address) match

7.6.2.93 PRBS_CTRL_10 Register (Offset = 62Ah) [Reset = 0000h]

PRBS_CTRL_10 is shown in Figure 7-112 and described in Table 7-116.

Return to the Table 7-23.

Figure 7-112. PRBS_CTRL_10 Register

15	14	13	12	11	10	9	8
pmatch_data_47_32							
R/W-0h							
7	6	5	4	3	2	1	0
pmatch_data_47_32							
R/W-0h							

Table 7-116. PRBS_CTRL_10 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	pmatch_data_47_32	R/W	0h	Bits 47:32 of Perfect Match Data - used for DA (destination address) match

7.6.2.94 CRC_STATUS Register (Offset = 638h) [Reset = 0000h]

CRC_STATUS is shown in Figure 7-113 and described in Table 7-117.

Return to the Table 7-23.

Figure 7-113. CRC_STATUS Register

15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED						rx_bad_crc	tx_bad_crc
R-0h						R-0h	R-0h

Table 7-117. CRC_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15-2	RESERVED	R	0h	Reserved
1	rx_bad_crc	R	0h	CRC error indication in packet received on Cu RX 0h = No CRC error 1h = CRC error
0	tx_bad_crc	R	0h	CRC error indication in packet transmitted on Cu TX 0h = No CRC error 1h = CRC error

7.6.2.95 PKT_STAT_1 Register (Offset = 639h) [Reset = 0000h]

PKT_STAT_1 is shown in Figure 7-114 and described in Table 7-118.

Return to the Table 7-23.

Figure 7-114. PKT_STAT_1 Register

15	14	13	12	11	10	9	8
tx_pkt_cnt_15_0							
0h							
7	6	5	4	3	2	1	0
tx_pkt_cnt_15_0							
0h							

Table 7-118. PKT_STAT_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	tx_pkt_cnt_15_0		0h	Lower 16 bits of Tx packet counter Note : Register is cleared when 0x39, 0x3A, 0x3B are read in sequence

7.6.2.96 PKT_STAT_2 Register (Offset = 63Ah) [Reset = 0000h]

PKT_STAT_2 is shown in Figure 7-115 and described in Table 7-119.

Return to the Table 7-23.

Figure 7-115. PKT_STAT_2 Register

15	14	13	12	11	10	9	8
tx_pkt_cnt_31_16							
0h							
7	6	5	4	3	2	1	0
tx_pkt_cnt_31_16							
0h							

Table 7-119. PKT_STAT_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	tx_pkt_cnt_31_16		0h	Upper 16 bits of Tx packet counter Note : Register is cleared when 0x39, 0x3A, 0x3B are read in sequence

7.6.2.97 PKT_STAT_3 Register (Offset = 63Bh) [Reset = 0000h]

PKT_STAT_3 is shown in Figure 7-116 and described in Table 7-120.

Return to the Table 7-23.

Figure 7-116. PKT_STAT_3 Register

15	14	13	12	11	10	9	8
tx_err_pkt_cnt							
0h							
7	6	5	4	3	2	1	0
tx_err_pkt_cnt							
0h							

Table 7-120. PKT_STAT_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	tx_err_pkt_cnt		0h	Tx packet w error (CRC error) counter Note : Register is cleared when 0x39, 0x3A, 0x3B are read in sequence

7.6.2.98 PKT_STAT_4 Register (Offset = 63Ch) [Reset = 0000h]

PKT_STAT_4 is shown in Figure 7-117 and described in Table 7-121.

Return to the Table 7-23.

Figure 7-117. PKT_STAT_4 Register

15	14	13	12	11	10	9	8
rx_pkt_cnt_15_0							
0h							
7	6	5	4	3	2	1	0
rx_pkt_cnt_15_0							
0h							

Table 7-121. PKT_STAT_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	rx_pkt_cnt_15_0		0h	Lower 16 bits of Rx packet counter Note : Register is cleared when 0x3C, 0x3D, 0x3E are read in sequence

7.6.2.99 PKT_STAT_5 Register (Offset = 63Dh) [Reset = 0000h]

PKT_STAT_5 is shown in Figure 7-118 and described in Table 7-122.

Return to the Table 7-23.

Figure 7-118. PKT_STAT_5 Register

15	14	13	12	11	10	9	8
rx_pkt_cnt_31_16							
0h							
7	6	5	4	3	2	1	0
rx_pkt_cnt_31_16							
0h							

Table 7-122. PKT_STAT_5 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	rx_pkt_cnt_31_16		0h	Upper 16 bits of Rx packet counter Note : Register is cleared when 0x3C, 0x3D, 0x3E are read in sequence

7.6.2.100 PKT_STAT_6 Register (Offset = 63Eh) [Reset = 0000h]

PKT_STAT_6 is shown in Figure 7-119 and described in Table 7-123.

Return to the Table 7-23.

Figure 7-119. PKT_STAT_6 Register

15	14	13	12	11	10	9	8
rx_err_pkt_cnt							
0h							
7	6	5	4	3	2	1	0
rx_err_pkt_cnt							
0h							

Table 7-123. PKT_STAT_6 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	rx_err_pkt_cnt		0h	Rx packet w error (CRC error) counter Note : Register is cleared when 0x3C, 0x3D, 0x3E are read in sequence

7.6.2.101 SQI_REG_1 Register (Offset = 871h) [Reset = 0000h]

SQI_REG_1 is shown in Figure 7-120 and described in Table 7-124.

Return to the Table 7-23.

Figure 7-120. SQI_REG_1 Register

15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
worst_sqi_out			RESERVED	sqi_out			RESERVED
0h			R-0h	R-0h			R-0h

Table 7-124. SQI_REG_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R	0h	Reserved
7-5	worst_sqi_out		0h	3 bit Worst SQI since last read (see SQI mapping above)
4	RESERVED	R	0h	Reserved
3-1	sqi_out	R	0h	3 bit SQI - (mse here refers to Mean Square Error 0x875[9:0]) 0b000 = MSE > 102 0b001 = 81 < MSE ≤102 0b010 = 65 < MSE ≤ 81 0b011 = 51 < MSE ≤ 65 0b100 = 41 < MSE ≤ 51 0b101 = 32 < MSE ≤ 41 0b110 = 25 < MSE ≤ 32 0b111 = MSE ≤ 25
0	RESERVED	R	0h	Reserved

7.6.2.102 DSP_REG_75 Register (Offset = 875h) [Reset = 0000h]

DSP_REG_75 is shown in Figure 7-121 and described in Table 7-125.

Return to the Table 7-23.

Figure 7-121. DSP_REG_75 Register

15	14	13	12	11	10	9	8
RESERVED				RESERVED		mse_lock	
R-0h				R-0h		R-0h	
7	6	5	4	3	2	1	0
mse_lock							
R-0h							

Table 7-125. DSP_REG_75 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	RESERVED	R	0h	Reserved
11-10	RESERVED	R	0h	Reserved
9-0	mse_lock	R	0h	10 bit mse used for SQI mapping. (mse = mean square error at the receiver)

7.6.2.103 SQI_1 Register (Offset = 8ADh) [Reset = 3051h]

SQI_1 is shown in Figure 7-122 and described in Table 7-126.

Return to the Table 7-23.

Figure 7-122. SQI_1 Register

15	14	13	12	11	10	9	8
cfg_hist_1_2				cfg_acc_window_sel		cfg_sqi_th_1_2	
R/W-3h				R/W-0h		R/W-51h	
7	6	5	4	3	2	1	0
cfg_sqi_th_1_2							
R/W-51h							

Table 7-126. SQI_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	cfg_hist_1_2	R/W	3h	Hysteresis between SQI value 1 and 2
11-10	cfg_acc_window_sel	R/W	0h	Accumulator window select - 00b = 90us 01b = 180us 10b = 360us 11b = 720us
9-0	cfg_sqi_th_1_2	R/W	51h	Threshold between SQI value 1 and 2

7.6.2.104 PMA_PMD_CONTROL_1 Register (Offset = 1000h) [Reset = 0000h]

PMA_PMD_CONTROL_1 is shown in Figure 7-123 and described in Table 7-127.

Return to the Table 7-23.

First nibble (0x1) in the register address is to indicated MMD register space. For register access, ignore the first nibble.

Figure 7-123. PMA_PMD_CONTROL_1 Register

15	14	13	12	11	10	9	8
pma_reset_2	RESERVED			cfg_low_power_2	RESERVED		
R-0h	R-0h			R-0h	R-0h		
7	6	5	4	3	2	1	0
RESERVED							
R-0h							

Table 7-127. PMA_PMD_CONTROL_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	pma_reset_2	R	0h	1 = PMA/PMD reset 0 = Normal operation Note - RW bit, self clearing
14-12	RESERVED	R	0h	Reserved
11	cfg_low_power_2	R	0h	1 = Low-power mode 0 = Normal operation Note - RW bit
10-0	RESERVED	R	0h	Reserved

7.6.2.105 PMA_PMD_CONTROL_2 Register (Offset = 1007h) [Reset = 003Dh]

PMA_PMD_CONTROL_2 is shown in Figure 7-124 and described in Table 7-128.

Return to the Table 7-23.

First nibble (0x1) in the register address is to indicated MMD register space. For register access, ignore the first nibble.

Figure 7-124. PMA_PMD_CONTROL_2 Register

15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED		cfg_pma_type_selection					
R-0h		R/W-3Dh					

Table 7-128. PMA_PMD_CONTROL_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-6	RESERVED	R	0h	Reserved
5-0	cfg_pma_type_selection	R/W	3Dh	BASE-T1 type selection for device 3Dh = BASE-T1 type selection for device

7.6.2.106 PMA_PMD_TRANSMIT_DISABLE Register (Offset = 1009h) [Reset = 0000h]

PMA_PMD_TRANSMIT_DISABLE is shown in Figure 7-125 and described in Table 7-129.

Return to the Table 7-23.

First nibble (0x1) in the register address is to indicated MMD register space. For register access, ignore the first nibble.

Figure 7-125. PMA_PMD_TRANSMIT_DISABLE Register

15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							cfg_transmit_disable_2
R-0h							R-0h

Table 7-129. PMA_PMD_TRANSMIT_DISABLE Register Field Descriptions

Bit	Field	Type	Reset	Description
15-1	RESERVED	R	0h	Reserved
0	cfg_transmit_disable_2	R	0h	1 = Transmit disable 0 = Normal operation Note - RW bit

7.6.2.107 PMA_PMD_EXTENDED_ABILITY2 Register (Offset = 100Bh) [Reset = 0800h]

PMA_PMD_EXTENDED_ABILITY2 is shown in Figure 7-126 and described in Table 7-130.

Return to the Table 7-23.

First nibble (0x1) in the register address is to indicated MMD register space. For register access, ignore the first nibble.

Figure 7-126. PMA_PMD_EXTENDED_ABILITY2 Register

15	14	13	12	11	10	9	8
RESERVED				base_t1_extended_abilities	RESERVED		
R-0h				R-1h	R-0h		
7	6	5	4	3	2	1	0
RESERVED							
R-0h							

Table 7-130. PMA_PMD_EXTENDED_ABILITY2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	RESERVED	R	0h	Reserved
11	base_t1_extended_abilities	R	1h	1 = PMA/PMD has BASE-T1 extended abilities listed in register 1.18 0 = PMA/PMD does not have BASE-T1 extended abilities
10-0	RESERVED	R	0h	Reserved

7.6.2.108 PMA_PMD_EXTENDED_ABILITY Register (Offset = 1012h) [Reset = 0002h]

PMA_PMD_EXTENDED_ABILITY is shown in Figure 7-127 and described in Table 7-131.

Return to the Table 7-23.

First nibble (0x1) in the register address is to indicated MMD register space. For register access, ignore the first nibble.

Figure 7-127. PMA_PMD_EXTENDED_ABILITY Register

15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED						mr_1000_base_t1_ability	mr_100_base_t1_ability
R-0h						R-1h	R-0h

Table 7-131. PMA_PMD_EXTENDED_ABILITY Register Field Descriptions

Bit	Field	Type	Reset	Description
15-2	RESERVED	R	0h	Reserved
1	mr_1000_base_t1_ability	R	1h	1 = PMA/PMD is able to perform 1000BASE-T1 0 = PMA/PMD is not able to perform 1000BASE-T1
0	mr_100_base_t1_ability	R	0h	1 = PMA/PMD is able to perform 100BASE-T1 0 = PMA/PMD is not able to perform 100BASE-T1

7.6.2.109 PMA_PMD_CONTROL Register (Offset = 1834h) [Reset = 8001h]

PMA_PMD_CONTROL is shown in Figure 7-128 and described in Table 7-132.

Return to the Table 7-23.

First nibble (0x1) in the register address is to indicated MMD register space. For register access, ignore the first nibble.

Figure 7-128. PMA_PMD_CONTROL Register

15	14	13	12	11	10	9	8
RESERVED	cfg_master_slave_val	RESERVED					
R-1h	R/W-0h	R-0h					
7	6	5	4	3	2	1	0
RESERVED				RESERVED			
R-0h				R/W-1h			

Table 7-132. PMA_PMD_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	1h	Reserved
14	cfg_master_slave_val	R/W	0h	1 = Configure PHY as MASTER 0 = Configure PHY as SLAVE
13-4	RESERVED	R	0h	Reserved
3-0	RESERVED	R/W	1h	Reserved

7.6.2.110 PMA_CONTROL Register (Offset = 1900h) [Reset = 0000h]

PMA_CONTROL is shown in Figure 7-129 and described in Table 7-133.

Return to the Table 7-23.

First nibble (0x1) in the register address is to indicated MMD register space. For register access, ignore the first nibble.

Figure 7-129. PMA_CONTROL Register

15	14	13	12	11	10	9	8
pma_reset	cfg_transmit_disable	RESERVED		cfg_low_power	RESERVED		
R-0h	R-0h	R-0h		R-0h	R-0h		
7	6	5	4	3	2	1	0
RESERVED							
R-0h							

Table 7-133. PMA_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	pma_reset	R	0h	1 = PMA/PMD reset 0 = Normal operation Note - RW bit, self clearing
14	cfg_transmit_disable	R	0h	1 = Transmit disable 0 = Normal operation Note - RW bit
13-12	RESERVED	R	0h	Reserved
11	cfg_low_power	R	0h	1 = Low-power mode 0 = Normal operation Note - RW bit
10-0	RESERVED	R	0h	Reserved

7.6.2.111 PMA_STATUS Register (Offset = 1901h) [Reset = 0900h]

PMA_STATUS is shown in Figure 7-130 and described in Table 7-134.

Return to the Table 7-23.

First nibble (0x1) in the register address is to indicated MMD register space. For register access, ignore the first nibble.

Figure 7-130. PMA_STATUS Register

15	14	13	12	11	10	9	8
RESERVED				oam_ability	eee_ability	receive_fault_ability	low_power_ability
R-0h				R-1h	R-0h	R-0h	R-1h
7	6	5	4	3	2	1	0
RESERVED					receive_polarity	receive_fault	pma_receive_link_status_ll
R-0h					R-0h	R-0h	R/W0S-0h

Table 7-134. PMA_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	RESERVED	R	0h	Reserved
11	oam_ability	R	1h	1 = PHY has 1000BASE-T1 OAM ability 0 = PHY does not have 1000BASE-T1 OAM ability
10	eee_ability	R	0h	1 = PHY has EEE ability 0 = PHY does not have EEE ability
9	receive_fault_ability	R	0h	1 = PMA/PMD has the ability to detect a fault condition on the receive path 0 = PMA/PMD does not have the ability to detect a fault condition on the receive path
8	low_power_ability	R	1h	1 = PMA/PMD has low-power ability 0 = PMA/PMD does not have low-power ability
7-3	RESERVED	R	0h	Reserved
2	receive_polarity	R	0h	1 = Receive polarity is reversed 0 = Receive polarity is not reversed
1	receive_fault	R	0h	1 = Fault condition detected 0 = Fault condition not detected
0	pma_receive_link_status_ll	R/W0S	0h	1 = PMA/PMD receive link up 0 = PMA/PMD receive link down

7.6.2.112 TRAINING Register (Offset = 1902h) [Reset = 0002h]

TRAINING is shown in Figure 7-131 and described in Table 7-135.

Return to the Table 7-23.

First nibble (0x1) in the register address is to indicated MMD register space. For register access, ignore the first nibble.

Figure 7-131. TRAINING Register

15	14	13	12	11	10	9	8
RESERVED						cfg_training_user_fld	
R-0h						R/W-0h	
7	6	5	4	3	2	1	0
cfg_training_user_fld				RESERVED		cfg_oam_en	cfg_eee_en
R/W-0h				R-0h		R/W-1h	R/W-0h

Table 7-135. TRAINING Register Field Descriptions

Bit	Field	Type	Reset	Description
15-11	RESERVED	R	0h	Reserved
10-4	cfg_training_user_fld	R/W	0h	7-bit user defined field to send to the link partner
3-2	RESERVED	R	0h	Reserved
1	cfg_oam_en	R/W	1h	1 = 1000BASE-T1 OAM ability advertised to link partner 0 = 1000BASE-T1 OAM ability not advertised to link partner
0	cfg_eee_en	R/W	0h	1 = EEE ability advertised to link partner 0 = EEE ability not advertised to link partner

7.6.2.113 LP_TRAINING Register (Offset = 1903h) [Reset = 0000h]

LP_TRAINING is shown in Figure 7-132 and described in Table 7-136.

Return to the Table 7-23.

First nibble (0x1) in the register address is to indicated MMD register space. For register access, ignore the first nibble.

Figure 7-132. LP_TRAINING Register

15	14	13	12	11	10	9	8
RESERVED						lp_training_user_fld	
R-0h						R-0h	
7	6	5	4	3	2	1	0
lp_training_user_fld				RESERVED		lp_oam_adv	lp_eee_adv
R-0h				R-0h		R-0h	R-0h

Table 7-136. LP_TRAINING Register Field Descriptions

Bit	Field	Type	Reset	Description
15-11	RESERVED	R	0h	Reserved
10-4	lp_training_user_fld	R	0h	7-bit user defined field received from the link partner
3-2	RESERVED	R	0h	Reserved
1	lp_oam_adv	R	0h	1 = Link partner has 1000BASE-T1 OAM ability 0 = Link partner does not have 1000BASE-T1 OAM ability
0	lp_eee_adv	R	0h	1 = Link partner has EEE ability 0 = Link partner does not have EEE ability

7.6.2.114 TEST_MODE_CONTROL Register (Offset = 1904h) [Reset = 0000h]

TEST_MODE_CONTROL is shown in Figure 7-133 and described in Table 7-137.

Return to the Table 7-23.

First nibble (0x1) in the register address is to indicated MMD register space. For register access, ignore the first nibble.

Figure 7-133. TEST_MODE_CONTROL Register

15	14	13	12	11	10	9	8
cfg_test_mode			RESERVED				
R/W-0h			R-0h				
7	6	5	4	3	2	1	0
RESERVED							
R-0h							

Table 7-137. TEST_MODE_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
15-13	cfg_test_mode	R/W	0h	111 = Test mode 7 110 = Test mode 6 101 = Test mode 5 100 = Test mode 4 011 = Reserved 010 = Test mode 2 001 = Test mode 1 000 = Normal (non-test) operation
12-0	RESERVED	R	0h	Reserved

7.6.2.115 PCS_CONTROL_COPY Register (Offset = 3000h) [Reset = 0000h]

PCS_CONTROL_COPY is shown in Figure 7-134 and described in Table 7-138.

Return to the Table 7-23.

First nibble (0x3) in the register address is to indicated MMD register space. For register access, ignore the first nibble.

Figure 7-134. PCS_CONTROL_COPY Register

15	14	13	12	11	10	9	8
pcs_reset_2	mmd3_loopback_2	RESERVED					
R-0h	R-0h	R-0h					
7	6	5	4	3	2	1	0
RESERVED							
R-0h							

Table 7-138. PCS_CONTROL_COPY Register Field Descriptions

Bit	Field	Type	Reset	Description
15	pcs_reset_2	R	0h	Note - RW bit, self clear bit 0h = Normal operation 1h = PCS reset
14	mmd3_loopback_2	R	0h	Note - RW bit 0h = Disable loopback mode 1h = Enable loopback mode
13-0	RESERVED	R	0h	Reserved

7.6.2.116 PCS_CONTROL Register (Offset = 3900h) [Reset = 0000h]

PCS_CONTROL is shown in Figure 7-135 and described in Table 7-139.

Return to the Table 7-23.

First nibble (0x3) in the register address is to indicated MMD register space. For register access, ignore the first nibble.

Figure 7-135. PCS_CONTROL Register

15	14	13	12	11	10	9	8
pcs_reset	mmd3_loopback	RESERVED					
R-0h	R-0h	R-0h					
7	6	5	4	3	2	1	0
RESERVED							
R-0h							

Table 7-139. PCS_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	pcs_reset	R	0h	Note - RW bit, self clear bit 0h = Normal operation 1h = PCS reset
14	mmd3_loopback	R	0h	Note - RW bit 0h = Disable loopback mode 1h = Enable loopback mode
13-0	RESERVED	R	0h	Reserved

7.6.2.117 PCS_STATUS Register (Offset = 3901h) [Reset = 0000h]

PCS_STATUS is shown in Figure 7-136 and described in Table 7-140.

Return to the Table 7-23.

First nibble (0x3) in the register address is to indicated MMD register space. For register access, ignore the first nibble.

Figure 7-136. PCS_STATUS Register

15	14	13	12	11	10	9	8
RESERVED				tx_lpi_received_lh	rx_lpi_received_lh	tx_lpi_indication	rx_lpi_indication
R-0h				R/W0C-0h	R/W0C-0h	R-0h	R-0h
7	6	5	4	3	2	1	0
pcs_fault	RESERVED				pcs_receive_link_status_ll	RESERVED	
R-0h	R-0h				R/W0S-0h	R-0h	

Table 7-140. PCS_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	RESERVED	R	0h	Reserved
11	tx_lpi_received_lh	R/W0C	0h	0h = LPI not received 1h = Tx PCS has received LPI
10	rx_lpi_received_lh	R/W0C	0h	0h = LPI not received 1h = Rx PCS has received LPI
9	tx_lpi_indication	R	0h	0h = PCS is not currently receiving LPI 1h = Tx PCS is currently receiving LPI
8	rx_lpi_indication	R	0h	0h = PCS is not currently receiving LPI 1h = Rx PCS is currently receiving LPI
7	pcs_fault	R	0h	0h = No fault condition detected 1h = Fault condition detected
6-3	RESERVED	R	0h	Reserved
2	pcs_receive_link_status_ll	R/W0S	0h	0h = PCS receive link down 1h = PCS receive link up
1-0	RESERVED	R	0h	Reserved

7.6.2.118 PCS_STATUS_2 Register (Offset = 3902h) [Reset = 0000h]

PCS_STATUS_2 is shown in Figure 7-137 and described in Table 7-141.

Return to the Table 7-23.

First nibble (0x3) in the register address is to indicated MMD register space. For register access, ignore the first nibble.

Figure 7-137. PCS_STATUS_2 Register

15	14	13	12	11	10	9	8
RESERVED					pcs_receive_link_status	hi_rfer	block_lock
R-0h					R-0h	R-0h	R-0h
7	6	5	4	3	2	1	0
hi_rfer_lh	block_lock_ll	RESERVED					
R/W0C-0h	R/W0S-0h	R-0h					

Table 7-141. PCS_STATUS_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-11	RESERVED	R	0h	Reserved
10	pcs_receive_link_status	R	0h	0h = PCS receive link down 1h = PCS receive link up
9	hi_rfer	R	0h	0h = PCS not reporting a high BER 1h = PCS reporting a high BER
8	block_lock	R	0h	0h = PCS not locked to received blocks 1h = PCS locked to received blocks
7	hi_rfer_lh	R/W0C	0h	0h = PCS has not reported a high BER 1h = PCS has reported a high BER
6	block_lock_ll	R/W0S	0h	0h = PCS does not have block lock 1h = PCS has block lock
5-0	RESERVED	R	0h	Reserved

7.6.2.119 OAM_TRANSMIT Register (Offset = 3904h) [Reset = 0000h]

OAM_TRANSMIT is shown in Figure 7-138 and described in Table 7-142.

Return to the Table 7-23.

First nibble (0x3) in the register address is to indicated MMD register space. For register access, ignore the first nibble.

Figure 7-138. OAM_TRANSMIT Register

15	14	13	12	11	10	9	8
mr_tx_valid	mr_tx_toggle	mr_tx_received	mr_tx_received_toggle	mr_tx_message_num			
R/WMC,0-0h	R-0h	0h	R-0h	R/W-0h			
7	6	5	4	3	2	1	0
RESERVED				mr_rx_ping	mr_tx_ping	mr_tx_snr	
R-0h				R-0h	R/W-0h	R-0h	

Table 7-142. OAM_TRANSMIT Register Field Descriptions

Bit	Field	Type	Reset	Description
15	mr_tx_valid	R/WMC,0	0h	This bit is used to indicate message data in registers 3.2308.11:8, 3.2309, 3.2310, 3.2311, and 3.2312 are valid and ready to be loaded. This bit shall self-clear when registers are loaded by the state machine. 1 = Message data in registers are valid 0 = Message data in registers are not valid
14	mr_tx_toggle	R	0h	Toggle value to be transmitted with message. This bit is set by the state machine and cannot be overridden by the user.
13	mr_tx_received		0h	This bit shall self clear on read. 1 = 1000BASE-T1 OAM message received by link partner 0 = 1000BASE-T1 OAM message not received by link partner
12	mr_tx_received_toggle	R	0h	Toggle value of message that was received by link partner
11-8	mr_tx_message_num	R/W	0h	User-defined message number to send
7-4	RESERVED	R	0h	Reserved
3	mr_rx_ping	R	0h	Received PingTx value from latest good 1000BASE-T1 OAM frame received
2	mr_tx_ping	R/W	0h	Ping value to send to link partner
1-0	mr_tx_snr	R	0h	00 = PHY link is failing and will drop link and relink within 2 ms to 4 ms after the end of the current 1000BASE-T1 OAM frame. 01 = LPI refresh is insufficient to maintain PHY SNR. Request link partner to exit LPI and send idles (used only when EEE is enabled). 10 = PHY SNR is marginal. 11 = PHY SNR is good.

7.6.2.120 OAM_TX_MESSAGE_1 Register (Offset = 3905h) [Reset = 0000h]

OAM_TX_MESSAGE_1 is shown in Figure 7-139 and described in Table 7-143.

Return to the Table 7-23.

First nibble (0x3) in the register address is to indicated MMD register space. For register access, ignore the first nibble.

Figure 7-139. OAM_TX_MESSAGE_1 Register

15	14	13	12	11	10	9	8
mr_tx_message_15_0							
R/W-0h							
7	6	5	4	3	2	1	0
mr_tx_message_15_0							
R/W-0h							

Table 7-143. OAM_TX_MESSAGE_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	mr_tx_message_15_0	R/W	0h	Message octet 1/0. LSB transmitted first.

7.6.2.121 OAM_TX_MESSAGE_2 Register (Offset = 3906h) [Reset = 0000h]

OAM_TX_MESSAGE_2 is shown in Figure 7-140 and described in Table 7-144.

Return to the Table 7-23.

First nibble (0x3) in the register address is to indicated MMD register space. For register access, ignore the first nibble.

Figure 7-140. OAM_TX_MESSAGE_2 Register

15	14	13	12	11	10	9	8
mr_tx_message_31_16							
R/W-0h							
7	6	5	4	3	2	1	0
mr_tx_message_31_16							
R/W-0h							

Table 7-144. OAM_TX_MESSAGE_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	mr_tx_message_31_16	R/W	0h	Message octet 3/2. LSB transmitted first.

7.6.2.122 OAM_TX_MESSAGE_3 Register (Offset = 3907h) [Reset = 0000h]

OAM_TX_MESSAGE_3 is shown in Figure 7-141 and described in Table 7-145.

Return to the Table 7-23.

First nibble (0x3) in the register address is to indicated MMD register space. For register access, ignore the first nibble.

Figure 7-141. OAM_TX_MESSAGE_3 Register

15	14	13	12	11	10	9	8
mr_tx_message_47_32							
R/W-0h							
7	6	5	4	3	2	1	0
mr_tx_message_47_32							
R/W-0h							

Table 7-145. OAM_TX_MESSAGE_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	mr_tx_message_47_32	R/W	0h	Message octet 5/4. LSB transmitted first.

7.6.2.123 OAM_TX_MESSAGE_4 Register (Offset = 3908h) [Reset = 0000h]

OAM_TX_MESSAGE_4 is shown in Figure 7-142 and described in Table 7-146.

Return to the Table 7-23.

First nibble (0x3) in the register address is to indicated MMD register space. For register access, ignore the first nibble.

Figure 7-142. OAM_TX_MESSAGE_4 Register

15	14	13	12	11	10	9	8
mr_tx_message_63_48							
R/W-0h							
7	6	5	4	3	2	1	0
mr_tx_message_63_48							
R/W-0h							

Table 7-146. OAM_TX_MESSAGE_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	mr_tx_message_63_48	R/W	0h	Message octet 7/6. LSB transmitted first.

7.6.2.124 OAM_RECEIVE Register (Offset = 3909h) [Reset = 0000h]

OAM_RECEIVE is shown in Figure 7-143 and described in Table 7-147.

Return to the Table 7-23.

First nibble (0x3) in the register address is to indicated MMD register space. For register access, ignore the first nibble.

Figure 7-143. OAM_RECEIVE Register

15	14	13	12	11	10	9	8
mr_rx_lp_valid	mr_rx_lp_toggle	RESERVED		mr_rx_lp_message_num			
R-0h	R-0h	R-0h		R-0h			
7	6	5	4	3	2	1	0
RESERVED						mr_rx_lp_SNR	
R-0h						R-0h	

Table 7-147. OAM_RECEIVE Register Field Descriptions

Bit	Field	Type	Reset	Description
15	mr_rx_lp_valid	R	0h	This bit is used to indicate message data in registers 3.2313.11:8, 3.2314, 3.2315, 3.2316, and 3.2317 are stored and ready to be read. This bit shall self clear when register 3.2317 is read. 0h = Message data in registers are not valid 1h = Message data in registers are valid
14	mr_rx_lp_toggle	R	0h	Toggle value received with message Note - 0x3 added in [15:12] to differentiate
13-12	RESERVED	R	0h	Reserved
11-8	mr_rx_lp_message_num	R	0h	Message number from link partner Note - 0x3 added in [15:12] to differentiate
7-2	RESERVED	R	0h	Reserved
1-0	mr_rx_lp_SNR	R	0h	00 = Link partner link is failing and will drop link and relink within 2 ms to 4 ms after the end of the current 1000BASE-T1 OAM frame. 01 = LPI refresh is insufficient to maintain link partner SNR. Link partner requests local device to exit LPI and send idles (used only when EEE is enabled). 10 = Link partner SNR is marginal. 11 = Link partner SNR is good

7.6.2.125 OAM_RX_MESSAGE_1 Register (Offset = 390Ah) [Reset = 0000h]

OAM_RX_MESSAGE_1 is shown in Figure 7-144 and described in Table 7-148.

Return to the Table 7-23.

First nibble (0x3) in the register address is to indicated MMD register space. For register access, ignore the first nibble.

Figure 7-144. OAM_RX_MESSAGE_1 Register

15	14	13	12	11	10	9	8
mr_rx_lp_message_15_0							
R-0h							
7	6	5	4	3	2	1	0
mr_rx_lp_message_15_0							
R-0h							

Table 7-148. OAM_RX_MESSAGE_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	mr_rx_lp_message_15_0	R	0h	Message octet 1/0. LSB transmitted first.

7.6.2.126 OAM_RX_MESSAGE_2 Register (Offset = 390Bh) [Reset = 0000h]

OAM_RX_MESSAGE_2 is shown in Figure 7-145 and described in Table 7-149.

Return to the Table 7-23.

First nibble (0x3) in the register address is to indicated MMD register space. For register access, ignore the first nibble.

Figure 7-145. OAM_RX_MESSAGE_2 Register

15	14	13	12	11	10	9	8
mr_rx_lp_message_31_16							
R-0h							
7	6	5	4	3	2	1	0
mr_rx_lp_message_31_16							
R-0h							

Table 7-149. OAM_RX_MESSAGE_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	mr_rx_lp_message_31_16	R	0h	Message octet 3/2. LSB transmitted first.

7.6.2.127 OAM_RX_MESSAGE_3 Register (Offset = 390Ch) [Reset = 0000h]

OAM_RX_MESSAGE_3 is shown in Figure 7-146 and described in Table 7-150.

Return to the Table 7-23.

First nibble (0x3) in the register address is to indicated MMD register space. For register access, ignore the first nibble.

Figure 7-146. OAM_RX_MESSAGE_3 Register

15	14	13	12	11	10	9	8
mr_rx_lp_message_47_32							
R-0h							
7	6	5	4	3	2	1	0
mr_rx_lp_message_47_32							
R-0h							

Table 7-150. OAM_RX_MESSAGE_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	mr_rx_lp_message_47_32	R	0h	Message octet 5/4. LSB transmitted first.

7.6.2.128 OAM_RX_MESSAGE_4 Register (Offset = 390Dh) [Reset = 0000h]

OAM_RX_MESSAGE_4 is shown in Figure 7-147 and described in Table 7-151.

Return to the Table 7-23.

First nibble (0x3) in the register address is to indicated MMD register space. For register access, ignore the first nibble.

Figure 7-147. OAM_RX_MESSAGE_4 Register

15	14	13	12	11	10	9	8
mr_rx_lp_message_63_48							
0h							
7	6	5	4	3	2	1	0
mr_rx_lp_message_63_48							
0h							

Table 7-151. OAM_RX_MESSAGE_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	mr_rx_lp_message_63_48		0h	Message octet 7/6. LSB transmitted first.

7.6.2.129 AN_CFG Register (Offset = 7200h) [Reset = 0000h]

AN_CFG is shown in Figure 7-148 and described in Table 7-152.

Return to the Table 7-23.

First nibble (0x7) in the register address is to indicated MMD register space. For register access, ignore the first nibble.

Figure 7-148. AN_CFG Register

15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							mr_main_reset
R-0h							R/WSC-0h

Table 7-152. AN_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-1	RESERVED	R	0h	Reserved
0	mr_main_reset	R/WSC	0h	1 = Reset link sync/autoneg Note - RW bit Note - Added 7 to [15:12] to differentiate

7.6.2.1 Base Registers

BASE Registers lists the Base registers. All register offset addresses not listed in BASE Registers should be considered as reserved locations and the register contents should not be modified.

IEEE defined base register set as per 802.3 clause 22. These registers provide basic status, control, and identification functions.

Table 7-153. BASE Registers

Offset	Acronym	Register Name	Section
0x0	Basic_Mode_Control_		Go
0x1	Basic_Mode_Status_		Go
0x2	PHY_Identification__1		Go
0x3	PHY_Identification__2		Go
0xD	Extended__Control_Register		Go
0xE	Address_or_Data_		Go
0x10	PHY_Control_		Go
0x11	PHY_Configuration_		Go
0x12	Interrupt_Status__1		Go
0x13	Interrupt_Status__2		Go
0x16	Loopback_Control_		Go
0x18	Interrupt_Status__3		Go
0x1E	TDR_Control_		Go
0x1F	PHY_Reset_		Go
0x180	Receiver_Status_		Go

Complex bit access types are encoded to fit into small table cells. Table 7-154 shows the codes that are used for access types in this section.

Table 7-154. Base Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
W0C	W0C	Write 0 to clear
W0S	W0S	Write 0 to set
WMC	W	Write with manual clear to default (refer to register description to know about the clearing event)
WMC,0	W	Write with manual clear to 0 (refer to register description to know about the clearing event)
WMC,1	W	Write with manual clear to 1 (refer to register description to know about the clearing event)
WSC	W	Write
WSC,0	W	Write with self clear to 0
Reset or Default Value		
-n		Value after reset or the default value

7.6.2.1.1 Basic_Mode_Control_ Register (Offset = 0x0) [reset = 0x140]

Basic_Mode_Control_ is shown in Table 7-155.

Return to the Summary Table.

Table 7-155. Basic_Mode_Control_ Register Field Descriptions

Bit	Field	Type	Reset	Description
15	MII Reset	R/WMC	0x0	MII Reset 0x0 = No reset 0x1 = Digital in reset and all MII regs (0x0 - 0xF) reset to default
14	MII Loopback Enable	R/W	0x0	MII loopback enable 0x0 = No MII loopback 0x1 = MII loopback
13	Speed Selection LSB	R	0x0	Speed selection LSB 0x2 = 1000 Mb/s
12	RESERVED	R	0x0	Reserved
11	Power Down Mode Enable	R/W	0x0	Power down mode enable 0x0 = Normal mode 0x1 = Power down via register or pin
10	Isolate Mode Enable	R/W	0x0	Isolate mode enable 0x0 = Normal mode 0x1 = Isolate mode

Table 7-155. Basic_Mode_Control_ Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	RESERVED	R	0x0	Reserved
8	Duplex Mode	R	0x1	Duplex mode 0x0 = Half duplex 0x1 = Full duplex
7	RESERVED	R	0x0	Reserved
6	Speed Selection MSB	R	0x1	Speed selection MSB 0x2 = 1000 Mb/s
5	RESERVED	R	0x0	Reserved
4-0	RESERVED	R	0x0	Reserved

7.6.2.1.2 Basic_Mode_Status_ Register (Offset = 0x1) [reset = 0x141]

Basic_Mode_Status_ is shown in Table 7-156.

Return to the Summary Table.

Table 7-156. Basic_Mode_Status_ Register Field Descriptions

Bit	Field	Type	Reset	Description
15	100BASE-T4	R	0x0	100BASE-T4 0x0 = PHY not able to perform 100BASE-T4 0x1 = PHY able to perform 100BASE-T4
14	100BASE-TX Full-Duplex	R	0x0	100BASE-TX Full-Duplex 0x0 = PHY not able to perform full duplex 100BASE-X 0x1 = PHY able to perform full duplex 100BASE-X
13	100BASE-TX Half-Duplex	R	0x0	100BASE-TX Half-Duplex 0x0 = PHY not able to perform half duplex 100BASE-X 0x1 = PHY able to perform half duplex 100BASE-X
12	10BASE-T Full-Duplex	R	0x0	10BASE-T Full-Duplex 0x0 = PHY not able to operate at 10 Mb/s in full duplex mode 0x1 = PHY able to operate at 10 Mb/s in full duplex mode
11	10BASE-T Half-Duplex	R	0x0	10BASE-T Half-Duplex 0x0 = PHY not able to operate at 10 Mb/s in half duplex mode 0x1 = PHY able to operate at 10 Mb/s in half duplex mode
10	100BASE-T2 Full-Duplex	R	0x0	100BASE-T2 Full-Duplex 0x0 = PHY not able to perform full duplex 100BASE-T2 0x1 = PHY able to perform full duplex 100BASE-T2
9	100BASE-T2 Half-Duplex	R	0x0	100BASE-T2 Half-Duplex 0x0 = PHY not able to perform half duplex 100BASE-T2 0x1 = PHY able to perform half duplex 100BASE-T2

Table 7-156. Basic_Mode_Status_ Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	Extended Status Ready	R	0x1	Extended status in register 0xf 0x0 = No extended status information in Register 0xF 0x1 = Extended status information in Register 0xF
7	RESERVED	R	0x0	Reserved
6	SMI Preamble Supression	R	0x1	SMI preamble supression 0x0 = PHY will not accept management frames with preamble suppressed 0x1 = PHY will accept management frames with preamble suppressed.
5	RESERVED	R	0x0	Reserved
4	RESERVED	R/W0C	0x0	Reserved
3	RESERVED	R	0x0	Reserved
2	Link Status	R/W0S	0x0	Link status, latch low 0x0 = link had been down 0x1 = link is up
1	RESERVED	R/W0C	0x0	Reserved
0	Extended Capability	R	0x1	Extended capabilities status 0x0 = basic register set capabilities only 0x1 = extended register capabilities

7.6.2.1.3 PHY_Identification__1 Register (Offset = 0x2) [reset = 0x2000]

PHY_Identification__1 is shown in Table 7-157.

Return to the Summary Table.

Table 7-157. PHY_Identification__1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	Organizationally Unique Identifier Bits [21:6]	R	0x2000	

7.6.2.1.4 PHY_Identification__2 Register (Offset = 0x3) [reset = 0xA000]

PHY_Identification__2 is shown in Table 7-158.

Return to the Summary Table.

Table 7-158. PHY_Identification__2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-10	Organizationally Unique Identifier Bits [5:0]	R	0x28	
9-4	Model Number	R	0x0	Vendor Model Number: The six bits of vendor model number are mapped from bits 9 to 4

Table 7-158. PHY_Identification__2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	Revision Number	R	0x0	Model Revision Number: Four bits of the vendor model revision number are mapped from bits 3 to 0. This field is incremented for all major device changes.

7.6.2.1.5 Extended__Control_Register Register (Offset = 0xD) [reset = 0x0]

Extended__Control_Register is shown in Table 7-159.

Return to the Summary Table.

Table 7-159. Extended__Control_Register Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	Extended Register Command	R/W	0x0	Extended Register Command: 0x0 = Address 0x1 = Data, no post increment 0x2 = Data, post increment on read and write 0x3 = Data, post increment on write only
13-5	RESERVED	R	0x0	Reserved
4-0	DEVAD	R/W	0x0	Device Address: Bits[4:0] are the device address, DEVAD, that directs any access of ADDAR Register 0x000E - Address/Data Register to the appropriate MMD. Specifically, the DP83TC811S-Q1 uses the vendor specific DEVAD [4:0] = "11111" for access to registers 0x04D1 and lower. For MMD1 access the DEVAD[4:0] = "00001". All accesses through registers REGCR and ADDAR should use the DEVAD for either MMD or MMD1. Transactions with other DEVAD are ignored.

7.6.2.1.6 Address_or_Data_ Register (Offset = 0xE) [reset = 0x0]

Address_or_Data_ is shown in Table 7-160.

Return to the Summary Table.

Table 7-160. Address_or_Data_ Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	Address/Data	R/W	0x0	If REGCR register 15:14 = '00', holds the MMD DEVAD's address register, otherwise holds the MMD DEVAD's data.

7.6.2.1.7 PHY_Control_ Register (Offset = 0x10) [reset = 0x4]

PHY_Control_ is shown in Table 7-161.

Return to the Summary Table.

Table 7-161. PHY_Control_ Register Field Descriptions

Bit	Field	Type	Reset	Description
15-11	RESERVED	R	0x0	Reserved

Table 7-161. PHY_Control_ Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	Channel OK	R/W0S	0x0	Channel ok, latched low 0x0 = Channel ok had been reset 0x1 = Channel ok is set
9	Descrambler Lock	R/W0S	0x0	Descrambler lock, latched low 0x0 = Descrmabler had been locked 0x1 = Descrambler is locked
8	RESERVED	R	0x0	Reserved
7	Interrupt Pin Status		0x0	Interrupts pin status, cleared on reading register 0x12 0x0 = Interrupts pin not set 0x1 = Interrupt pin had been set
6-4	RESERVED	R	0x0	Reserved
3	MII Loopback Status	R	0x0	MII loopback status 0x0 = No MII loopback 0x1 = MII loopback
2	Duplex Mode Status	R	0x1	Duplex mode status 0x0 = Half duplex 0x1 = Full duplex
1	RESERVED	R	0x0	Reserved
0	Link Status	R	0x0	Link status 0x0 = link had been down 0x1 = link is up

7.6.2.1.8 PHY_Configuration_ Register (Offset = 0x11) [reset = 0x8]

PHY_Configuration_ is shown in Table 7-162 .

Return to the Summary Table.

Table 7-162. PHY_Configuration_ Register Field Descriptions

Bit	Field	Type	Reset	Description
15	Disable MAC Clock	R/W	0x0	Disable MAC clock 0x0 = keep clk_125 to MAC 0x1 = stop clk_125 to MAC on IEEE power save mode
14	Enable Force Power Mode	R/W	0x0	Enable power save mode config from reg
13-12	RESERVED	R/W	0x0	Reserved Must be written as 0x0
11	Reset SGMII	R/WSC	0x0	Reset SGMII block
10-4	RESERVED	R	0x0	Reserved

Table 7-162. PHY_Configuration_ Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	Interrupt Pin Polarity	R/W	0x1	Interrupt pin polarity 0x0 = Active high 0x1 = Active low
2	Force Interrupt Pin	R/W	0x0	Force interrupt pin 0x0 = Do not force interrupt pin 0x1 = Force interrupt pin
1	Interrupt Enable	R/W	0x0	Enable interrupts 0x0 = Disable interrupts 0x1 = Enable interrupts
0	RESERVED	R/W	0x0	Reserved Must be written as 0x0

7.6.2.1.9 Interrupt_Status__1 Register (Offset = 0x12) [reset = 0x0]

Interrupt_Status__1 is shown in Table 7-163.

Return to the Summary Table.

Table 7-163. Interrupt_Status__1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	Link Quality Low Interrupt	R	0x0	Link quality low interrupt status
14	Energy Detect Interrupt	R	0x0	Energy det change interrupt status
13	Link Status Changed Interrupt	R	0x0	Link status change interrupt status
12	RESERVED	R	0x0	Reserved
11	ESD Event Interrupt	R	0x0	ESD fault detected interrupt status
10	1000BASE-T1 Link Training Done Interrupt	R	0x0	Training done interrupt status
9-8	RESERVED	R	0x0	Reserved
7	Link Quality Interrupt Enable	R/W	0x0	Link quality bad interrupt enable
6	Energy Detect Interrupt Enable	R/W	0x0	Energy det change interrupt enable
5	Link Status Changed Interrupt Enable	R/W	0x0	Link status change interrupt enable
4	RESERVED	R	0x0	Reserved
3	ESD Event Interrupt Enable	R/W	0x0	ESD fault detected interrupt enable
2	1000BASE-T1 Link Training Done Enable	R/W	0x0	Training done interrupt enable
1-0	RESERVED	R	0x0	Reserved

7.6.2.1.10 Interrupt_Status__2 Register (Offset = 0x13) [reset = 0x0]

Interrupt_Status__2 is shown in Table 7-164.

Return to the Summary Table.

Table 7-164. Interrupt_Status__2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	Undervoltage Interrupt	R	0x0	Under volt interrupt status
14	Overvoltage Interrupt	R	0x0	Over volt interrupt status
13-12	RESERVED	R	0x0	Reserved
11	Overtemperature Interrupt	R	0x0	Over temp interrupt status
10	Sleep Mode Change Interrupt	R	0x0	Sleep mode change interrupt status
9	RESERVED	R	0x0	Reserved
8	not_one_hot_int	R	0x0	Not one hot interrupt status
7	Undervoltage Interrupt Enable	R/W	0x0	Under volt interrupt enable
6	Overvoltage Interrupt Enable	R/W	0x0	Over volt interrupt enable
5-4	RESERVED	R	0x0	Reserved
3	Overtemperature Interrupt Enable	R/W	0x0	Over temp interrupt enable
2	Sleep Mode Change Interrupt Enable	R/W	0x0	Sleep mode change interrupt enable
1-0	RESERVED	R	0x0	Reserved

7.6.2.1.11 Loopback_Control_ Register (Offset = 0x16) [reset = 0x0]

Loopback_Control_ is shown in Table 7-165.

Return to the Summary Table.

Table 7-165. Loopback_Control_ Register Field Descriptions

Bit	Field	Type	Reset	Description
15-11	RESERVED	R	0x0	Reserved
10	PRBS Checker Sync Loss	R/W0C	0x0	PRBS Checker Sync Loss Indication: 0x0 = PRBS checker has not lost sync 0x1 = PRBS checker has lost sync
9	RESERVED	R	0x0	Reserved
8	Core Power Mode	R	0x0	1b = Core is is normal power mode 0b = Core is in power down or sleep mode 0x0 = Core is in power down or sleep mode 0x1 = Core is is normal power mode
7	PCS Digital Loopback Enable	R/W	0x0	PCS digital loopback 0x0 = PCS digital loopback disabled 0x1 = PCS digital loopback enabled
6	Transmit Data In Loopback Enable	R/W	0x0	Transmit MII loopback data to MDI. This bit should only be used when in MII loopback mode. 0x0 = Suppress data to MDI 0x1 = Transmit data to MDI

Table 7-165. Loopback_Control_ Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-0	Loopback Select	R/W	0x0	Loopback mode selection: 0x1 = PCS loop 0x2 = RS loop 0x4 = Digital loop 0x8 = Analog loop 0x10 = Reverse loop 0x20 = Ext Reverse loop

7.6.2.1.12 Interrupt_Status__3 Register (Offset = 0x18) [reset = 0x8]

Interrupt_Status__3 is shown in Table 7-166.

Return to the Summary Table.

Table 7-166. Interrupt_Status__3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	Ack Received Interrupt	R	0x0	Ack received interrupt status (OAM)
14	TX Valid CLR Interrupt	R	0x0	mr_tx_valid clear interrupt status (OAM)
13-12	RESERVED	R	0x0	Reserved
11	POR Done Interrupt	R	0x0	POR done interrupt status
10	No Frame Interrupt	R	0x0	No frame detect interrupt status
9	Wake Request Interrupt	R	0x0	Wake request interrupt status
8	LPS Interrupt	R	0x0	LPS interrupt status
7	Ack Received Interrupt Enable	R/W	0x0	Ack received interrupt enable (OAM)
6	TX Valid CLR Interrupt Enable	R/W	0x0	mr_tx_valid clear interrupt enable (OAM)
5-4	RESERVED	R	0x0	Reserved
3	POR Done Interrupt Enable	R/W	0x1	POR done interrupt enable
2	No Frame Interrupt Enable	R/W	0x0	No frame detect interrupt enable
1	Wake Request Interrupt Enable	R/W	0x0	Wake request interrupt enable
0	LPS Interrupt Enable	R/W	0x0	LPS interrupt enable

7.6.2.1.13 TDR_Control_ Register (Offset = 0x1E) [reset = 0x0]

TDR_Control_ is shown in Table 7-167.

Return to the Summary Table.

Table 7-167. TDR_Control_ Register Field Descriptions

Bit	Field	Type	Reset	Description
15	TDR Start	R/WMC	0x0	Start TDR manually 0x0 = No TDR 0x1 = TDR start

Table 7-167. TDR_Control_ Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14	TDR Auto Run Enable	R/W	0x0	Enable TDR auto run on link down 0x0 = TDR start manually 0x1 = TDR start automatically on link down
13-2	RESERVED	R	0x0	Reserved
1	TDR Done	R	0x0	TDR Done: 0x0 = Cable diagnostic has not completed 0x1 = Indication that cable measurement process is complete
0	TDR Test Fail	R	0x0	TDR Test Fail: 0x0 = TDR has not suffered a failure 0x1 = TDR cable measurement process has failed

7.6.2.1.14 PHY_Reset_ Register (Offset = 0x1F) [reset = 0x0]

PHY_Reset_ is shown in Table 7-168.

Return to the Summary Table.

Table 7-168. PHY_Reset_ Register Field Descriptions

Bit	Field	Type	Reset	Description
15	Hardware Reset	R/WMC	0x0	Hardware Reset: 0x0 = Normal operation 0x1 = Reset PHY. This bit is self cleared and has the same effect as the RESET_N pin.
14	Software Restart	R/WMC	0x0	Software Restart: 0x0 = Normal operation 0x1 = Restart PHY. This bit is self cleared and resets all PHY circuitry except current control register values.
13-0	RESERVED	R/W	0x0	Reserved Must be written as 0x0

7.6.2.1.15 Receiver_Status_ Register (Offset = 0x180) [reset = 0x0]

Receiver_Status_ is shown in Table 7-169.

Return to the Summary Table.

Table 7-169. Receiver_Status_ Register Field Descriptions

Bit	Field	Type	Reset	Description
15-13	RESERVED	R	0x0	Reserved
12	Link Status	R	0x0	Unlatched Link Status: 0x0 = No link 0x1 = Valid link established
11-3	RESERVED	R	0x0	Reserved

Table 7-169. Receiver_Status_ Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	Descrambler Lock	R	0x0	Descrambler lock status: 0x0 = Descrambler not locked 0x1 = Descrambler locked on incoming symbols
1	Local Receiver Status	R	0x0	Local receiver status: 0x0 = Local PHY received invalid link 0x1 = Local PHY received valid link
0	Remote Receiver Status	R	0x0	Remote receiver status: 0x0 = Remote PHY received invalid link 0x1 = Remote PHY received valid link

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The DP83TG720S-Q1 is a single-port 1-Gbps Automotive Ethernet PHY. It supports IEEE 802.3bp and allows for connections to an Ethernet MAC through RGMII or SGMII. When using the device for Ethernet applications, it is necessary to meet certain requirements for normal operation. The following subsections are intended to assist in appropriate component selection and required connections.

8.2 Typical Applications

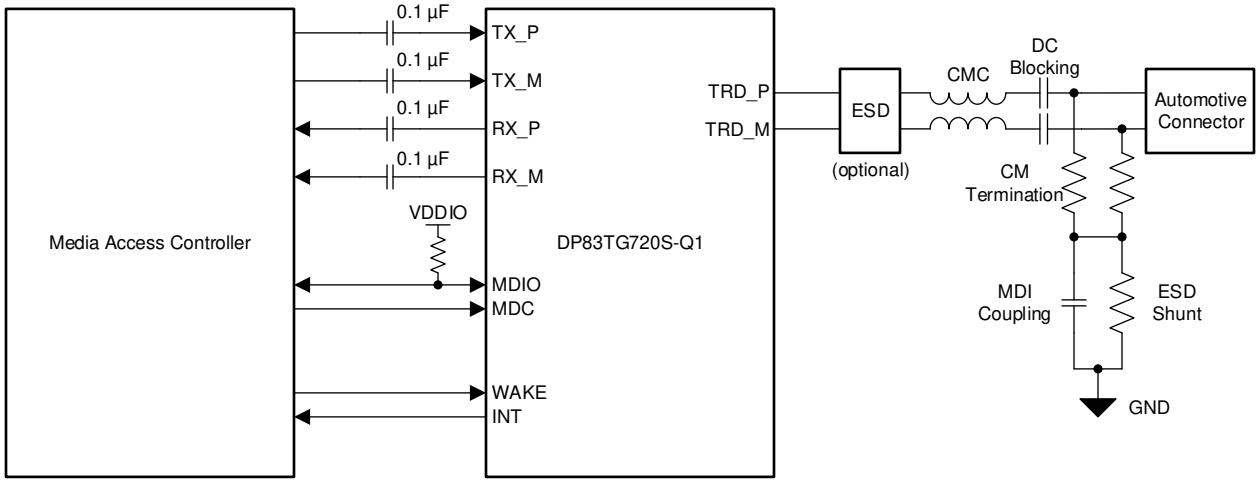


Figure 8-1. Typical Application (SGMII)

Table 8-1. Recommended Components for MDI Network

Design Parameter	Value
DC Blocking Capacitors 1	0.1 µF
Common-Mode Choke	Murata :DLW32MH101XT2
Common Mode Termination Resistors 1 2	1 kΩ
MDI Coupling Capacitor	4.7 nF
ESD Shunt	100 kΩ

1. 1% tolerance components are recommended for margins over spec of return loss and mode conversion.
2. CM termination resistor's size higher than 0805 helps in increasing ESD margin.

9 Power Supply Recommendations

The DP83TG720S-Q1 is capable of operating with a wide range of IO supply voltages (3.3 V, 2.5 V, or 1.8 V). No power supply sequencing is required. The recommended power supply de-coupling network is shown in following figure :

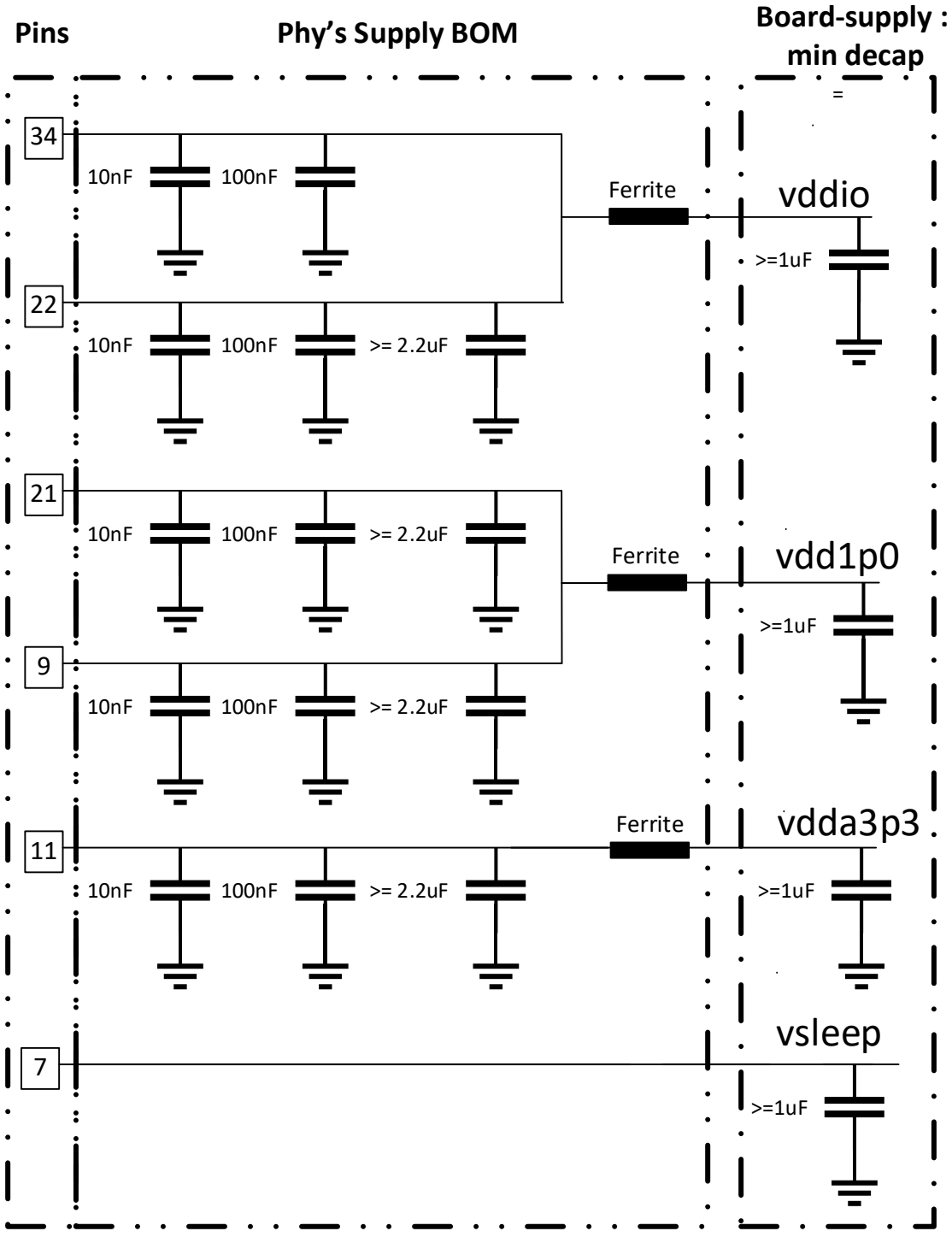


Figure 9-1. Recommended Supply De-Coupling Network (if sleep mode is used in the application)

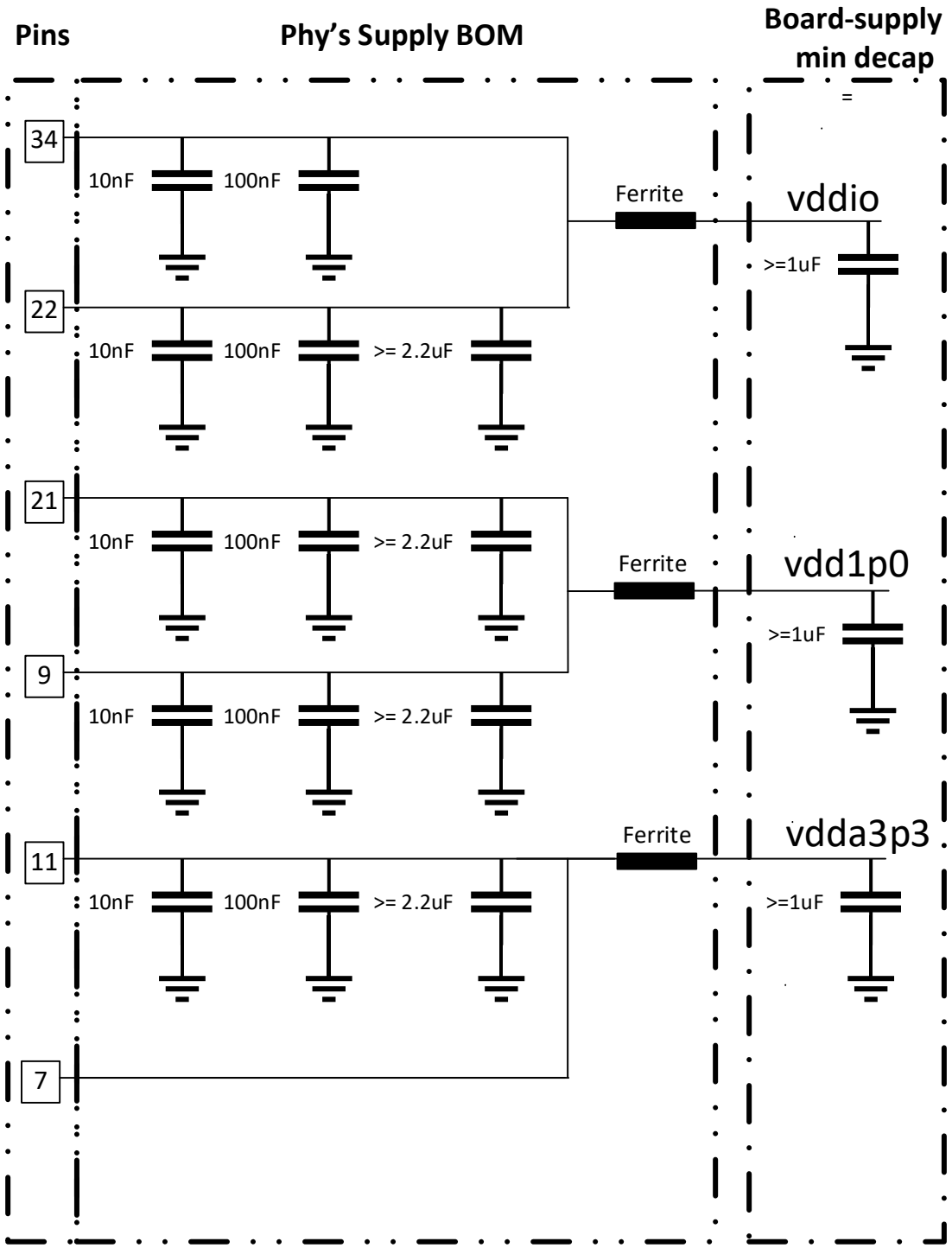


Figure 9-2. Recommended Supply De-Coupling Network (if sleep mode is not used in application)

Table 9-1. Recommended Components for Power Network

Design Parameter	Value
V_{DDIO}	1.8 V, 2.5 V, or 3.3 V
De-Coupling Capacitors V_{DDIO} (pin 34)	10 nF, 100 nF
De-Coupling Capacitors V_{DDIO} (pin 22)	10 nF, 100 nF, 2.2uF
Combined Ferrite Bead for VDDIO	BLM18HE102SN1

Table 9-1. Recommended Components for Power Network (continued)

Design Parameter	Value
V_{DDA}	3.3 V
De-Coupling Capacitors V_{DDA} (pin 11)	10 nF, 100 nF, 2.2uF
Ferrite Bead for V_{DDA}	BLM18KG601SH1
V_{DD1p0}	1 V
De-Coupling Capacitors V_{DD1P0} (pin 9)	10 nF, 100 nF, 2.2uF
De-Coupling Capacitors V_{DDA} (pin 21)	10 nF, 100 nF, 2.2uF
Combined Ferrite Bead for V_{DD1P0}	BLM18KG601SH1
V_{sleep}	3.3 V

Note

For recommendation on LDOs for VDD1p0 and Vsleep, please refer to the *DP83TC811, DP83TG730 Rollover Document* application report.

10 Compatibility with TI's 100BT1 PHY

Following table shows pin comparison between DP83TC811 and DP83TG720. Pins highlighted in bold need attention while designing a common board for both 100BT1 and 1000BT1 PHY. 100BT1 and 1000BT1 PHY's different BOM requirements can also be taken care by a common board.

Details and recommendation for common board design can be found in *DP83TC811, DP83TG720 Rollover Document* application report.

Table 10-1. Pin Comparison Table

Pin No.	DP83TC811	DP83TG720
1	MDC	MDC
2	INT_N	INT_N
3	RESET_N	RESET_N
4	XO	XO
5	XI	XI
6	LED_1	LED_1
7	**EN**	**VSLEEP**
8	**WAKE**	**WAKE**
9	**DNC**	**VDD1P0**
10	**INH**	**INH**
11	VDDA	VDDA
12	TRD_P	TRD_P
13	TRD_M	TRD_M
14	RX_ER	STRP1
15	RX_DV	RX_CTRL
16	CLKOUT	CLKOUT
17	**TCK**	**DNC**
18	**TDO**	**DNC**
19	**TMS**	**DNC**
20	**TCK**	**DNC**
21	**DNC**	**VDD1P0**
22	VDDIO	VDDIO
23	RX_D3	RX_D3
24	RX_D2	RX_D2
25	RX_D1	RX_D1
26	RX_D0	RX_D0
27	RX_CLK	RX_CLK
28	TXCLK	TXCLK
29	TX_EN	TX_CTRL
30	TX_D3	TX_D3
31	TX_D2	TX_D2
32	TX_D1	TX_D1
33	TX_D0	TX_D0
34	**TX_ER**	**VDDIO**
35	LED_0	LED_0
36	MDIO	MDIO

11 Layout

11.1 Layout Guidelines

11.1.1 Signal Traces

PCB traces are lossy and long traces can degrade signal quality. Traces should be kept short as possible. Unless mentioned otherwise, all signal traces should be 50-Ω, single-ended impedance. Differential traces should be 50-Ω single-ended and 100-Ω differential. Take care to ensure impedance is controlled throughout. Impedance discontinuities will cause reflections leading to emissions and signal integrity issues. Stubs should be avoided on all signal traces, especially differential signal pairs.

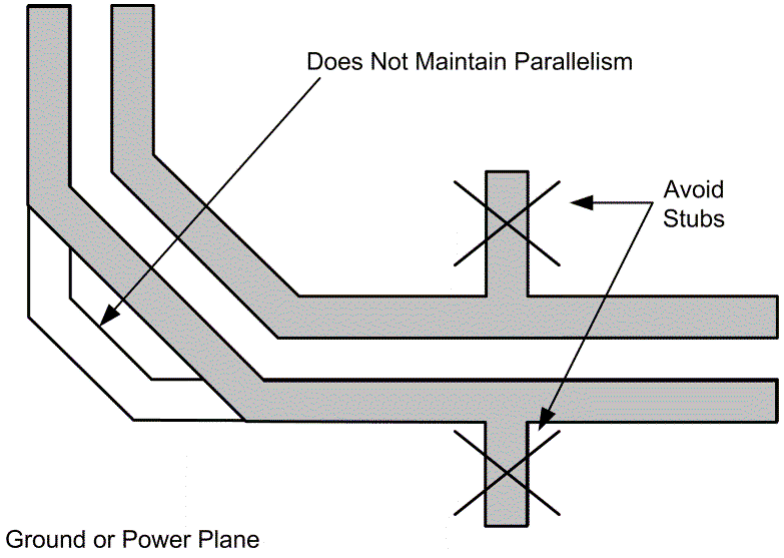


Figure 11-1. Differential Signal Trace Routing

Within the differential pairs, trace lengths should be run parallel to each other and matched in length. Matched lengths minimize delay differences, avoiding an increase in common mode noise and emissions. Length matching is also important for MAC interface connections. All transmit signal traces should be length matched to each other and all receive signal traces should be length matched to each other.

Ideally, there should be no crossover or vias on signal path traces. Vias present impedance discontinuities and should be minimized when possible. Route trace pairs on the same layer. Signals on different layers should not cross each other without at least one return path plane between them. Differential pairs should always have a constant coupling distance between them. For convenience and efficiency, TI recommends routing critical signals first (that is, MDI differential pairs, reference clock, and MAC IF traces).

11.1.2 Return Path

A general best practice is to have a solid return path beneath all signal traces. This return path can be a continuous ground or DC power plane. Reducing the width of the return path can potentially affect the impedance of the signal trace. This effect is more prominent when the width of the return path is comparable to the width of the signal trace. Breaks in return path between the signal traces should be avoided at all cost. A signal crossing a split plane may cause unpredictable return path currents and could impact signal quality and result in emissions issues.

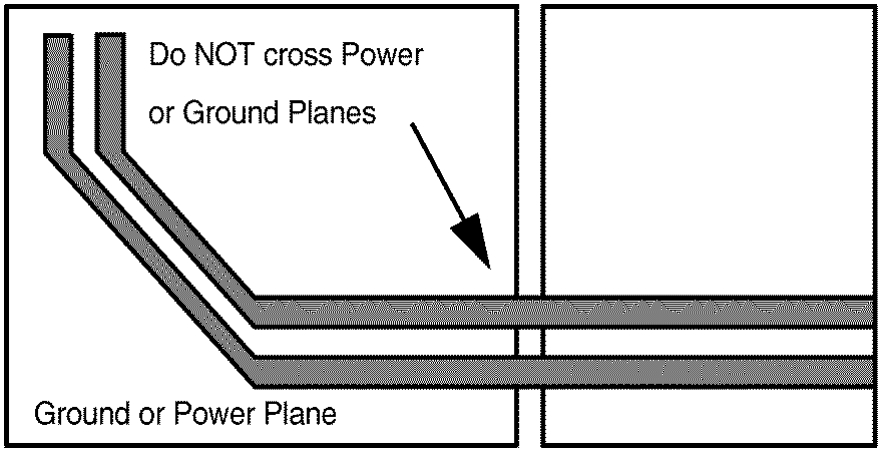


Figure 11-2. Power and Ground Plane Breaks

11.1.3 Physical Medium Attachment

There must be no metal running beneath the common-mode choke. CMCs can inject noise into metal beneath them, which can affect the emissions and immunity performance of the system. Because the DP83TG720S-Q1 is a voltage mode line driver, no external termination resistors are required. The ESD shunt and MDI coupling capacitor should be connected to ground. Ensure that the common mode termination resistors are 1% tolerance or better to improve differential coupling.

11.1.4 Metal Pour

All metal pours that are not signals or power must be tied to ground. There must be no floating metal in the system, and there must be no metal between differential traces.

11.1.5 PCB Layer Stacking

To meet signal integrity and performance requirements, minimum four-layer PCB is recommended. However, a six-layer PCB and above should be used when possible.

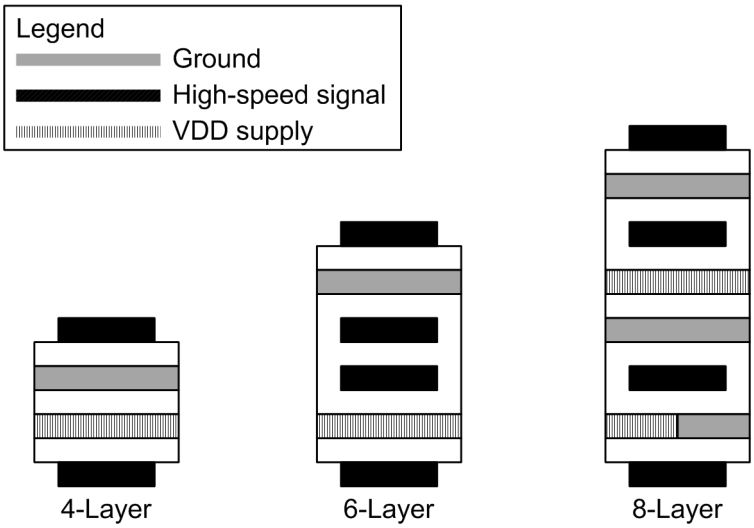


Figure 11-3. Recommended PCB Layer Stack-Up

12 Device and Documentation Support

12.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left navigation.

13.1 Package Option Addendum

13.1.1 Packaging Information

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish(4)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking(5) (6)
PDP83TG720SWCSTQ1	EARLY SAMPLE	VQFN	RHA	36	250	RoHS	NiPdAu	MSL3-260C	-40 to 125	
DP83TG720SWRHATQ1	ACTIVE	VQFN	RHA	36	250	RoHS	NiPdAu	MSL3-260C	-40 to 125	720S
DP83TG720SWRHARQ1	ACTIVE	VQFN	RHA	36	2500	RoHS	NiPdAu	MSL3-260C	-40 to 125	720S

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PRE_PROD Unannounced device, not in production, not available for mass market, nor on the web, samples not available.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

(5) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device

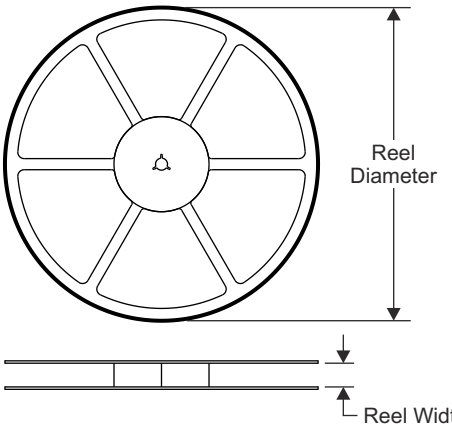
(6) Multiple Device markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

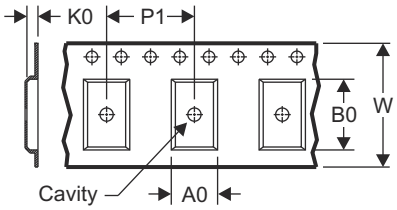
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

13.1.2 Tape and Reel Information

REEL DIMENSIONS

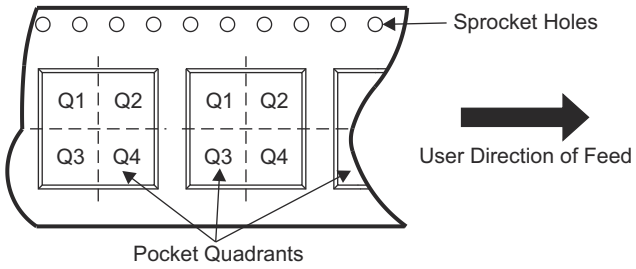


TAPE DIMENSIONS



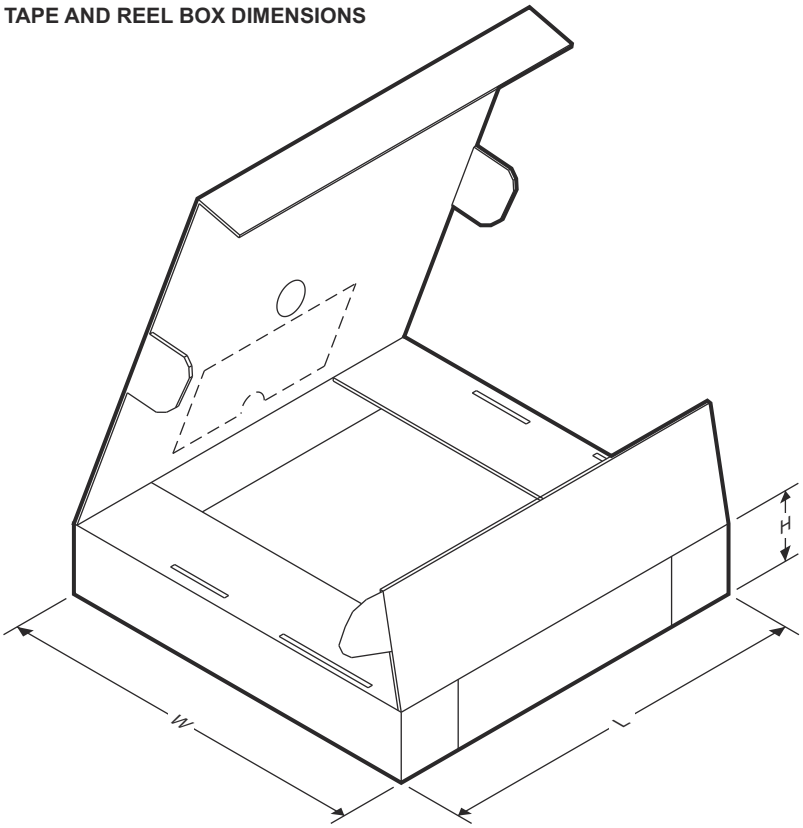
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PDP83TG720SWCSTQ1	VQFN	RHA	36	250	Call TI	Call TI	Call TI	Call TI	Call TI	Call TI	Call TI	Call TI
DP83TG720SWRHATQ1	VQFN	RHA	36	250	180	16.4	6.3	6.3	1.1	12	16	Q2
DP83TG720SWRHARQ1	VQFN	RHA	36	2500	330	16.4	6.3	6.3	1.1	12	16	Q2

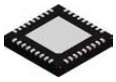
TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DP83TG720SWRHATQ1	VQFN	RHA	36	250	210	185	35
DP83TG720SWRHARQ1	VQFN	RHA	36	2500	367	367	35

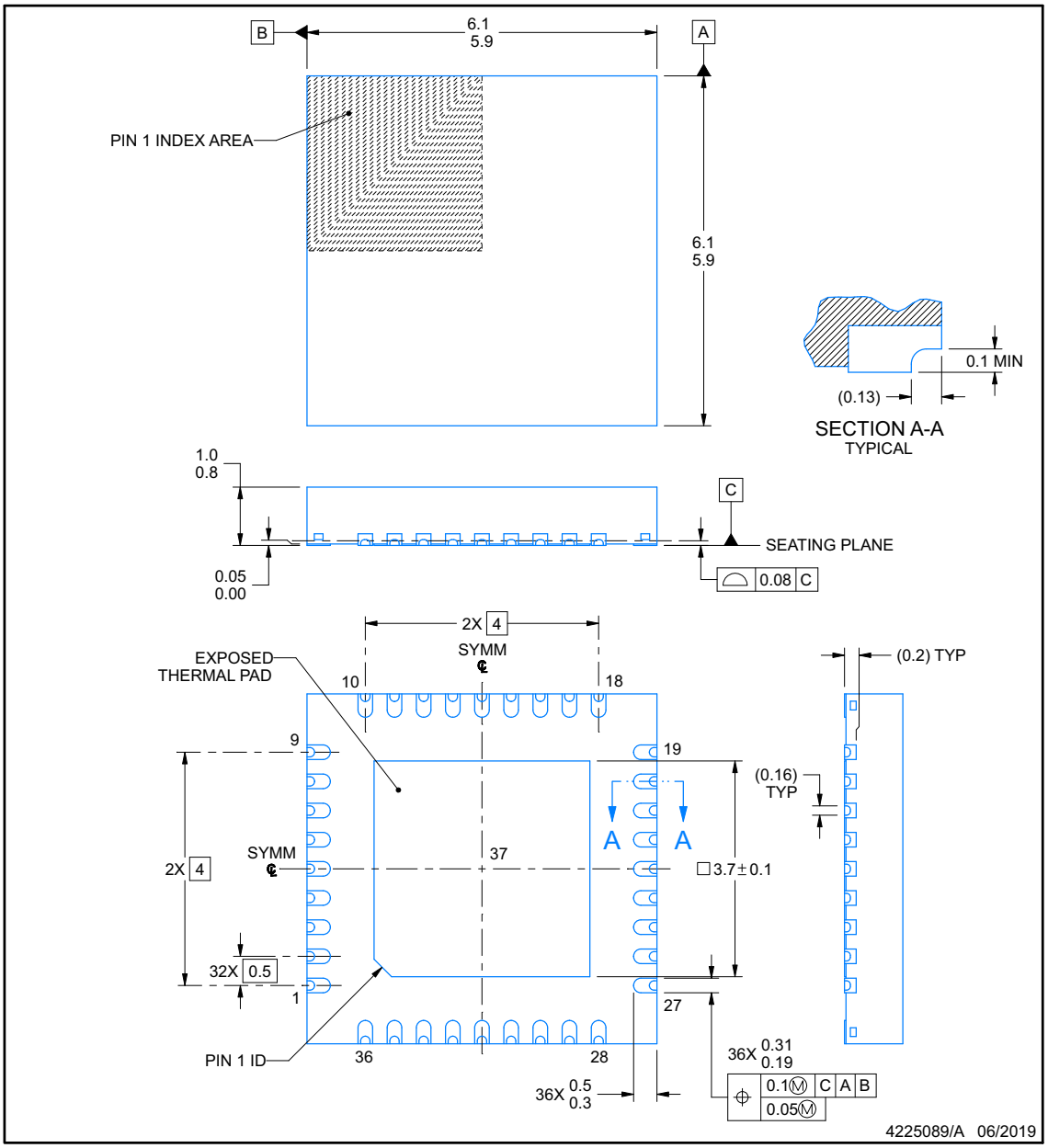
PACKAGE OUTLINE

RHA0036A



VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



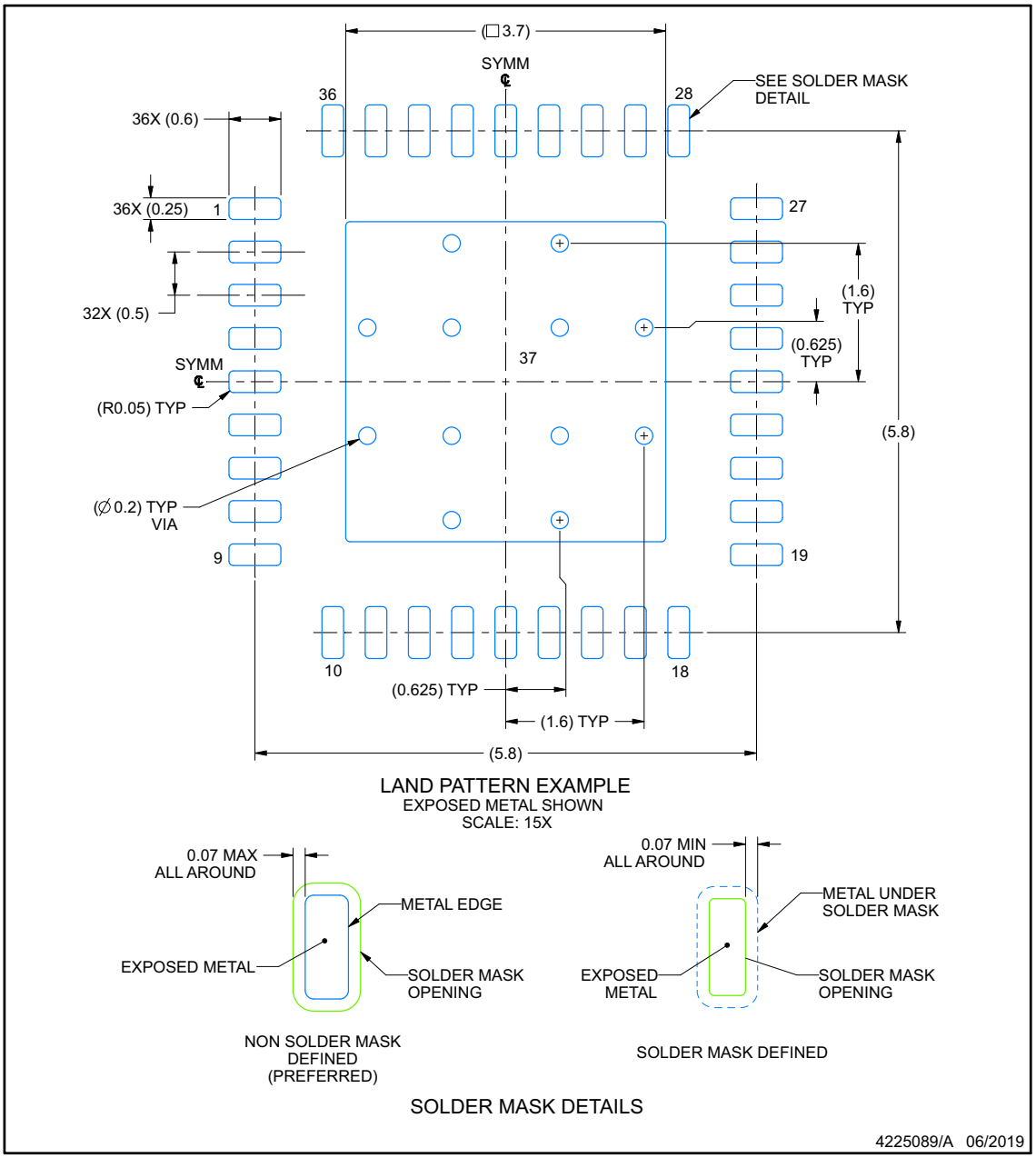
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

RHA0036A — **VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

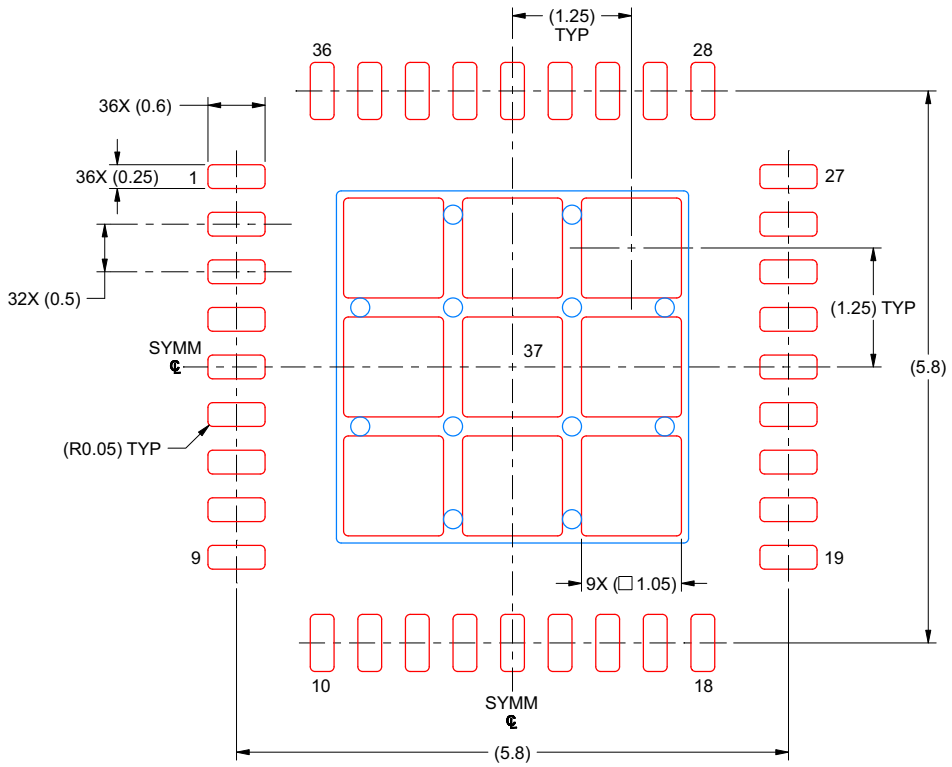
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RHA0036A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 15X

EXPOSED PAD 37
72% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4225089/A 06/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DP83TG720SWRHARQ1	ACTIVE	VQFN	RHA	36	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	720S	Samples
DP83TG720SWRHATQ1	ACTIVE	VQFN	RHA	36	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	720S	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

GENERIC PACKAGE VIEW

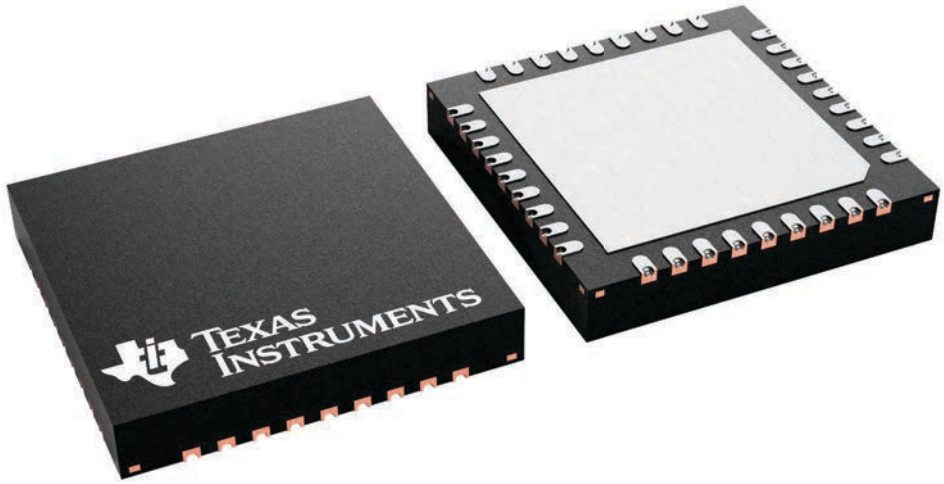
RHA 36

VQFN - 1 mm max height

6 x 6, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



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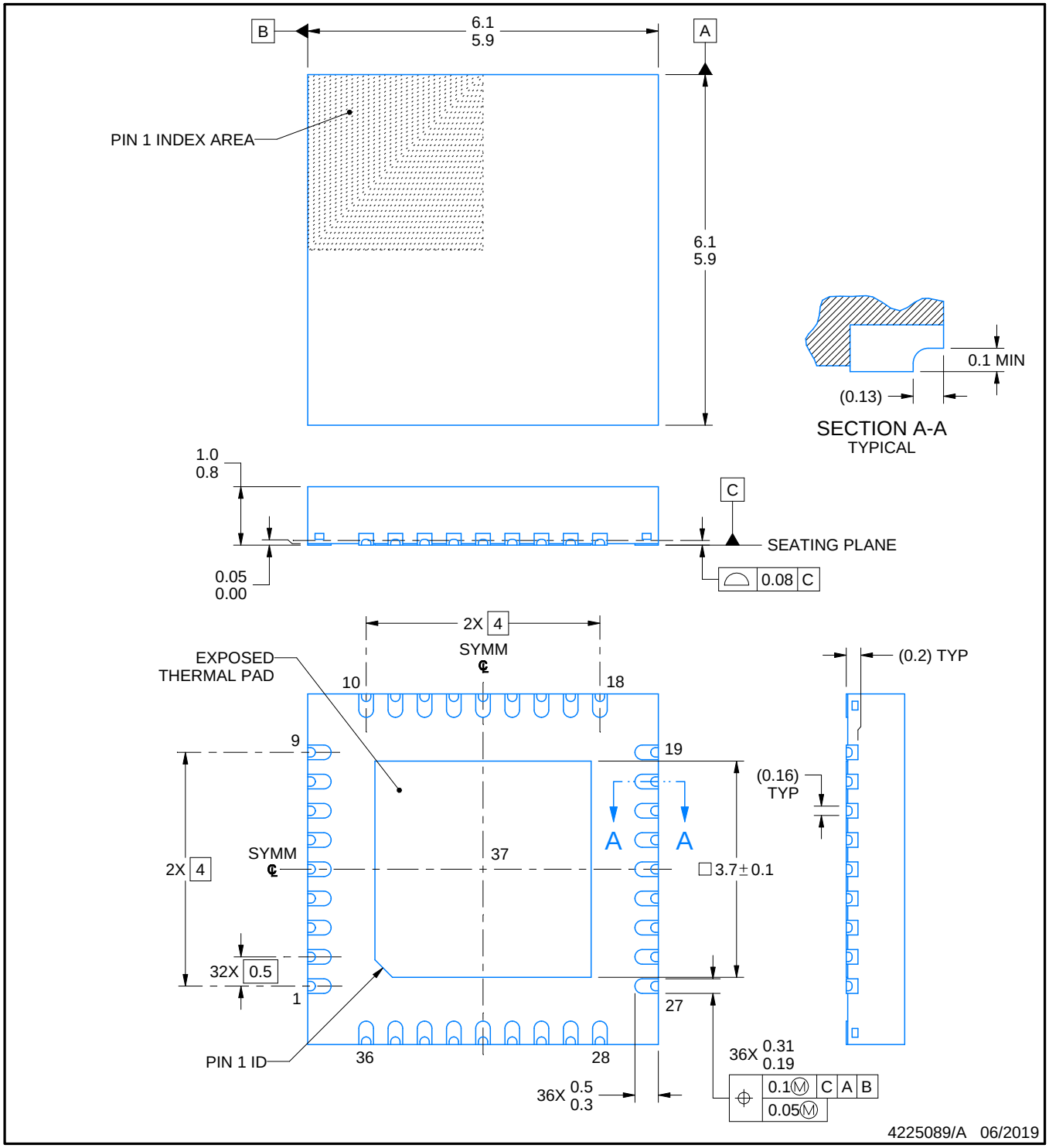
PACKAGE OUTLINE

RHA0036A

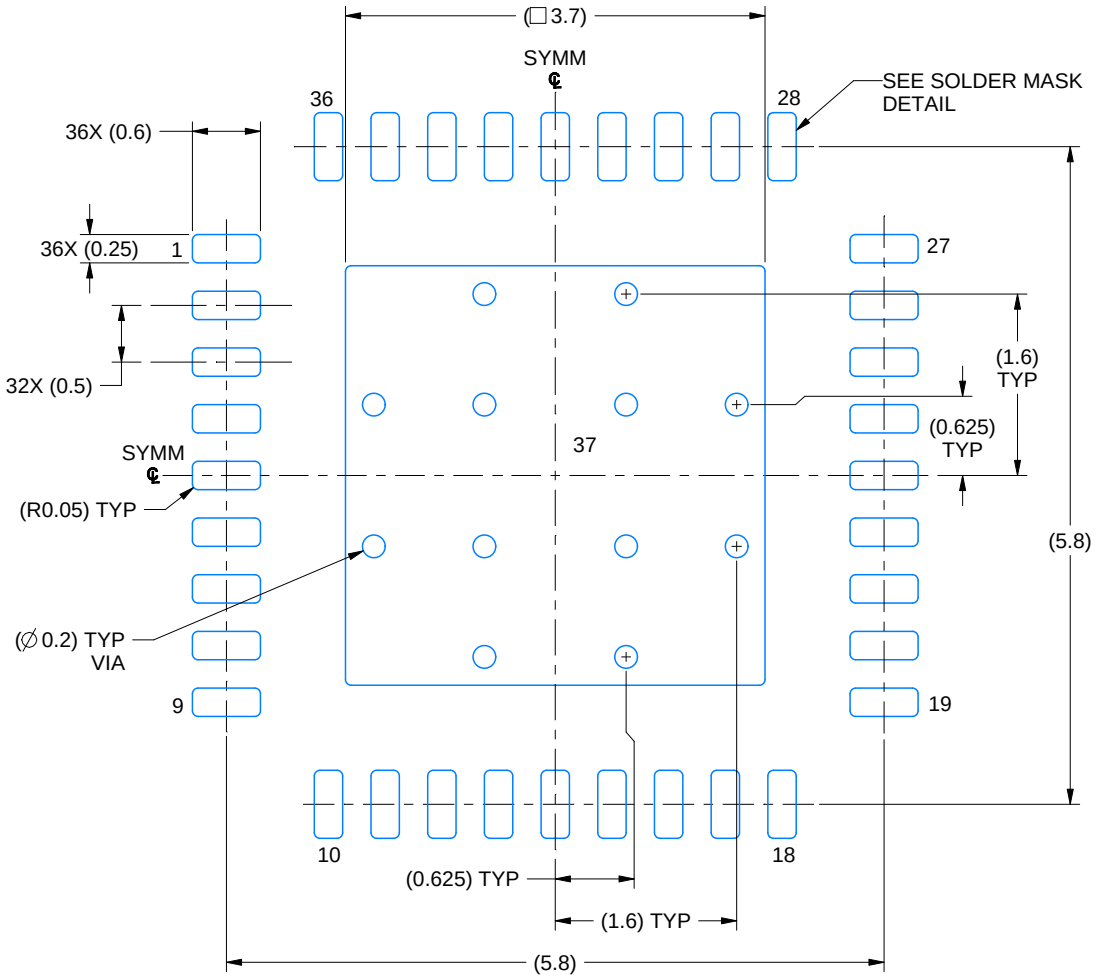
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

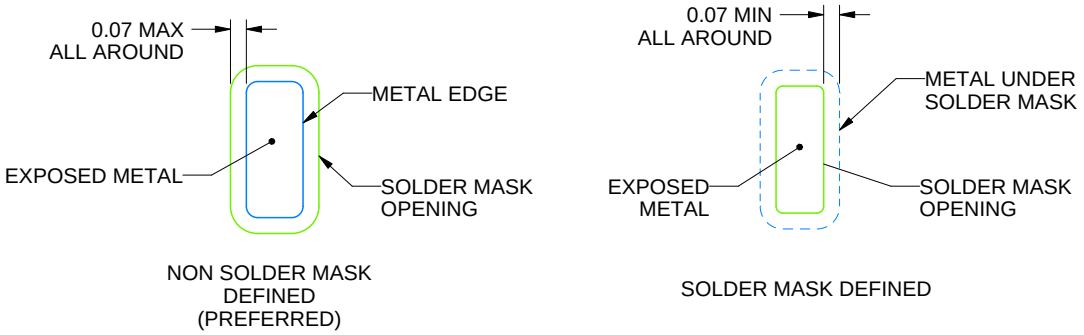


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



SOLDER MASK DETAILS

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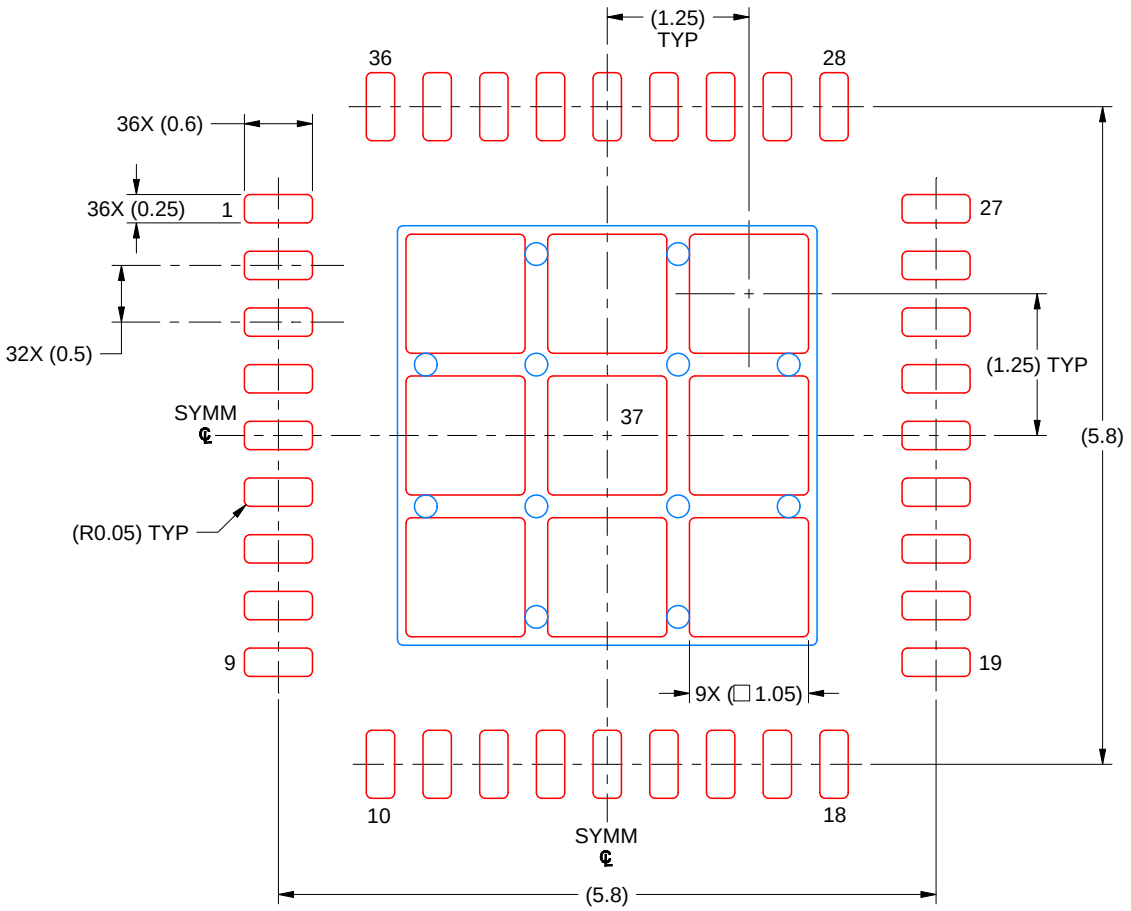
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 15X

EXPOSED PAD 37
72% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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