



Product Change Notification / SYST-30ACHB746

Date:

01-Jul-2021

Product Category:

32-bit Microcontrollers

PCN Type:

Document Change

Notification Subject:

Data Sheet - PIC32MZ Graphics (DAK/DAL/DAR/DAS) Family Data Sheet

Affected CPNs:

[SYST-30ACHB746_Affected_CPN_07012021.pdf](#)

[SYST-30ACHB746_Affected_CPN_07012021.csv](#)

Notification Text:

SYST-30ACHB746

Microchip has released a new Product Documents for the PIC32MZ Graphics (DAK/DAL/DAR/DAS) Family Data Sheet of devices. If you are using one of these devices please read the document located at [PIC32MZ Graphics \(DAK/DAL/DAR/DAS\) Family Data Sheet](#)

Notification Status: Final

Description of Change: The following updates were made during this release. e I2C, SPI, and I2S standards use the terminology "Master" and "Slave". The equivalent Microchip terminology used in this document is "Host" and "Client" respectively.

1. General - Throughout the document, References to both "Master" and "Slave" were revised to read "Host" and "Client" where applicable.
2. Updated 2.9.2 "5V Tolerant Input Pins", corrected VDD to VDDIO, and updated VDDIO specifications in the text
3. Removed erroneous information within parenthesis on Note 6 for Table 8-1: "System and Peripheral clock Distribution"

4. Updated Register 8-4: "REFOxCON: Reference Oscillator Control Register ('x' = 1-5)" to properly display x=1-5, and added Note 4
5. Updated the Note for Register 17-1: "DMTCN: Dead-man Timer Control Register"
6. Updated FIGURE 21-1: "SPI/I2S Module Block Diagram" to read "SPI Select" instead of "Slave Select"
7. Added a new note to the IRQM bit of Register 25-2: "PMMODE: Parallel Port Mode Register"
8. Added a new note to the IBOV bit of Register 25-7: "PMSTAT: Parallel Port Status Register (client modes only)"
9. Added AN5 to AN39 to the first bulleted item on page 585
10. Corrected typographical errors in bitfield 5-0 for Register 36-2: "GLCDCLKCON: Graphics LCD Controller Clock Control Register"
11. Added a note to the bit 28 of Register 38-24: "DDRSCLSTART: DDL SELF CALIBRATION LOGIC START REGISTER"
12. Corrected a typographical error in the DLYSTVAL bitfield of Register 38-29: "DDRPHYDLLR: DDR PHY DLL Recalibrate Register"
13. Updated FIGURE 40-1: "XLP Device Block Diagram" to properly display VDDCORE
14. A new note was added to 40.4 "Peripheral Module Disable"
15. Added a new note to the FDMTEN bitfield for Register 41-4: "DEVCFG1/ADEVCFG1: Device Configuration Word 1"
16. Corrected typographical errors in 41.4 "On-Chip Voltage Regulator"
17. Updated Table 44-23: System Timing Requirements with new conditions for the Reference Clock frequency
18. Updated Table 44-25: MPLL Clock Timing Requirements with a new maximum value for the MP12 Parameter
19. Updated the characteristics for Table 44-54: GLCD Controller Timing Specifications with the addition of GLCD pin verbiage
20. Updated Table 44-55: DDR2 SDRAM Timing Specifications with a correction to note 5
21. Updated the Descriptions for the 169-Ball Low Profile Ball Grid Array
22. Updated the Package description for the 169 Lead LFBGA

Impacts to Data Sheet: None

Reason for Change: To Improve Productivity

Change Implementation Status: Complete

Date Document Changes Effective: 01 Jul 2021

NOTE: Please be advised that this is a change to the document only the product has not been changed.

Markings to Distinguish Revised from Unrevised Devices: N/A

Attachments:

PIC32MZ Graphics (DAK/DAL/DAR/DAS) Family Data Sheet

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Affected Catalog Part Numbers (CPN)

PIC32MZ1025DAK169-I/HF
PIC32MZ1025DAK169-V/HF
PIC32MZ1025DAK169T-I/HF
PIC32MZ1025DAK169T-V/HF
PIC32MZ1025DAK176-I/2J
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