Product/Process Change Notice - PCN 19_0080 Rev. B

Analog Devices, Inc. Three Technology Way Norwood, Massachusetts 02062-9106

This notice is to inform you of a change that will be made to certain ADI products (see Appendix A) that you may have purchased in the last 2 years. **Any inquiries or requests with this PCN (additional data or samples) must be sent to ADI within 30 days of publication date.** ADI contact information is listed below.

Note: Revised fields are indicated by a red field name. See Appendix B for revision history.

PCN Title: ADIS1649X Layout Change

Publication Date: 30-Mar-2020

Effectivity Date: 10-Apr-2020 *(the earliest date that a customer could expect to receive changed material)*

Revision Description:

update /CS minimum stall time specification from 2us to 5 us. the effective startup time will increase from 170 ms to 220 ms.

Description Of Change:

Add voltage supervisory circuitry to limit the in-rush current of the module during turn on, which requires a layout change and additional components.
Data sheet changes:
From:
ADIS16490:Tstall time 2us; Initial startup time 170ms
ADIS16495:Tstall time 2us
ADIS16497:Tstall time 2us

To:
ADIS16490:Tstall time 5us; Initial startup time 250ms
ADIS16495:Tstall time 5us
ADIS16497:Tstall time 5us

Reason For Change:

This PCN covers an ADIS16490, ADIS16495 and ADIS16497 IMU design change which brings the observable in-rush current during power-up initialization sequence to 300 mA. During the initial power on sequence, a nominal peak of 500mA will still be experienced during the ramp of the VDD supply which is unchanged and follows: I = C x dVDD/dt, where C = 46µF. While there is no reliability concern for the existing IMU design, this change helps ensure that customers' IMU power supplies are not overstressed during IMU power-up.

The peak current consumption at power-up for existing ADIS16490, ADIS16495 and ADIS16497 IMUs is 3.2A at VDD = +3.6V. A plot of the VDD current with respect to time is a triangular profile with a total duration of less than 100µs. Note that a lower VDD will result in a peak current level that is less than 3.2A.

Impact of the change (positive or negative) on fit, form, function & reliability:

Removes the most stressing current demand at turn on. Tstall time increase on datasheet
ADIS16490 start up initialization time increase

Product Identification *(this section will describe how to identify the changed material)*

Earliest Possible date that will include the change is DC2015

Summary of Supporting Information:

Qualification will be performed per Industry Standard Test Methods. See attached Qualification Plan.

Supporting Documents

Attachment 1: Type: Qualification Plan

ADI_PCN_19_0080_Rev_B_ADIS1649x Product Revision Qual Plan_Rev 2.docx

For questions on this PCN, please send an email to the regional contacts below or contact your local ADI sales representatives.			
Americas: PCN_Americas@analog.com	**Europe:** PCN_Europe@analog.com	**Japan:** PCN_Japan@analog.com	**Rest of Asia:** PCN_ROA@analog.com

Appendix A - Affected ADI Models				
Existing Parts - Product Family / Model Number (8)				
ADIS16490 / ADIS16490BMLZ	ADIS16495 / AD24495	ADIS16495 / ADIS16495-1BMLZ	ADIS16495 / ADIS16495-2BMLZ	ADIS16495 / ADIS16495-3BMLZ
ADIS16497 / ADIS16497-1BMLZ	ADIS16497 / ADIS16497-2BMLZ	ADIS16497 / ADIS16497-3BMLZ		

Appendix B - Revision History			
Rev	**Publish Date**	**Effectivity Date**	**Rev Description**
Rev. -	26-Jun-2019	28-Sep-2019	Initial Release
Rev. A	26-Aug-2019	28-Sep-2019	Revised to clarify reason for change.
Rev. B	30-Mar-2020	10-Apr-2020	update /CS minimum stall time specification from 2us to 5 us. the effective startup time will increase from 170 ms to 220 ms.