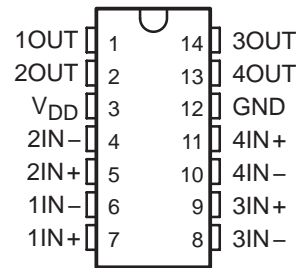- **Very Low Power . . . 200 μW Typ at 5 V**
- **Fast Response Time . . . 2.5 μs Typ With 5-mV Overdrive**
- **Single Supply Operation:**
  - **TLC139M . . . 4 V to 16 V**
  - **TLC339M . . . 4 V to 16 V**
  - **TLC339C . . . 3 V to 16 V**
  - **TLC339I . . . 3 V to 16 V**
- **High Input Impedance . . . $10^{12}$ Ω Typ**
- **Input Offset Voltage Change at Worst Case Input at Condition Typically 0.23 μV/Month Including the First 30 Days**
- **On-Chip ESD Protection**

**D, J, N, OR PW PACKAGE**
**(TOP VIEW)**

| | | |
|---|---|---|
| 1OUT | 1 | 14 | 3OUT |
| 2OUT | 2 | 13 | 4OUT |
| V$_{DD}$ | 3 | 12 | GND |
| 2IN− | 4 | 11 | 4IN+ |
| 2IN+ | 5 | 10 | 4IN− |
| 1IN− | 6 | 9 | 3IN+ |
| 1IN+ | 7 | 8 | 3IN− |

**FK PACKAGE**
**(TOP VIEW)**

Top pins: 2OUT, 1OUT, NC, 3OUT, 3OUT (3 2 1 20 19)

| | | |
|---|---|---|
| V$_{DD}$ | 4 | 18 | GND |
| NC | 5 | 17 | NC |
| 2IN− | 6 | 16 | 4IN+ |
| NC | 7 | 15 | NC |
| 2IN+ | 8 | 14 | 4IN− |

Bottom pins: 1IN−, 1IN+, NC, 3IN−, 3IN+ (9 10 11 12 13)
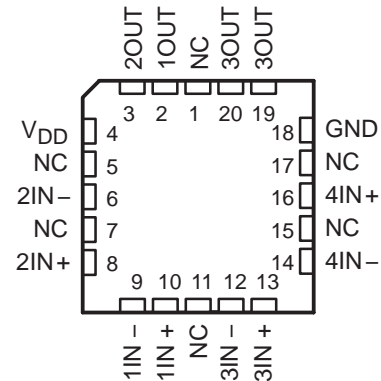
NC – No internal connection

## description

The TLC139/TLC339 consists of four independent differential-voltage comparators designed to operate from a single supply. It is functionally similar to the LM139/LM339 family but uses 1/20th the power for similar response times. The open-drain MOS output stage interfaces to a variety of leads and supplies, as well as wired logic functions. For a similar device with a push-pull output configuration, see the TLC3704 data sheet.

The Texas Instruments LinCMOS™ process offers superior analog performance to standard CMOS processes. Along with the standard CMOS advantages of low power without sacrificing speed, high input impedance, and low bias currents, the LinCMOS™ process offers extremely stable input offset voltages, even with differential input stresses of several volts. This characteristic makes it possible to build reliable CMOS comparators.

## symbol (each comparator)



**AVAILABLE OPTIONS**

| T$_A$ | V$_{IO}$ max AT 25°C | PACKAGE | | | | |
|---|---|---|---|---|---|---|
| | | SMALL OUTLINE (D) | CHIP CARRIER (FK) | CERAMIC DIP (J) | PLASTIC DIP (P) | TSSOP (PW) |
| 0°C to 70°C | 5 mV | TLC339CD | — | — | TLC339CN | TLC339CPW |
| −40°C to 85°C | 5 mV | TLC339ID | — | — | TLC339IN | TLC339IPW |
| −40°C to 125°C | 5 mV | TLC339QD | — | — | TLC339QN | — |
| −55°C to 125°C | 5 mV | TLC339MD | TLC139MFK | TLC139MJ | TLC339MN | — |

The D and PW packages are available taped and reeled. Add the suffix R to the device type (e.g., TLC339CDR or TLC339CPWR).

**TEXAS INSTRUMENTS**

## description (continued)

The TLC139M and TLC339M are characterized for operation over the full military temperature range of −55°C to 125°C. The TLC339C is characterized for operation over the commercial temperature range of 0°C to 70°C. The TLC339I is characterized for operation over the industrial temperature range of −40°C to 85°C. The TLC339Q is characterized for operation over the extended industrial temperature range of −40°C to 125°C.

## output schematic

```
┌─────────────────────────────────────┐
│         OPEN-DRAIN CMOS OUTPUT        │
│                                       │
│                      ┌──── Output     │
│                      │                │
│                    ──┤                │
│              ◄──   ──┤                │
│           ─ ─       └─●               │
│                       │               │
│                       │               │
│                      ═╧═              │
└─────────────────────────────────────┘
```

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{DD}$ (see Note 1) ......................................... −0.3 V to 18 V
Differential input voltage, $V_{ID}$ (see Note 2) ....................................... ±18 V
Input voltage range, $V_I$ ................................................ −0.3 V to $V_{DD}$
Output voltage range, $V_O$ .............................................. −0.3 V to $V_{DD}$
Input current, $I_I$ ......................................................... ±5 mA
Output current, $I_O$ (each output) ........................................... 20 mA
Total supply current into $V_{DD}$ ............................................ 40 mA
Total current out of GND ................................................. 60 mA
Continuous total dissipation ........................................ See Dissipation Rating Table
Operating free-air temperature range, $T_A$: TLC139M ...................................... −55°C to 125°C
                                      TLC339C .......................................... 0°C to 70°C
                                        TLC339I ....................................... −40°C to 85°C
                                        TLC339M ...................................... −55°C to 125°C
                                        TLC339Q ...................................... −40°C to 125°C
Storage temperature range ............................................... −65°C to 150°C
Case temperature for 60 seconds: FK package .............................................. 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package ................ 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package ..................... 300°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to network ground.
2. Differential voltages are at IN+ with respect to IN −.

**DISSIPATION RATING TABLE**

| PACKAGE | $T_A \leq 25$°C POWER RATING | DERATING FACTOR ABOVE $T_A = 25$°C | $T_A = 70$°C POWER RATING | $T_A = 85$°C POWER RATING | $T_A = 125$°C POWER RATING |
|---------|------------------------------|-------------------------------------|----------------------------|----------------------------|-----------------------------|
| D | 950 mW | 7.6 mW/°C | 608 mW | 494 mW | 190 mW |
| FK | 1375 mW | 11.0 mW/°C | 880 mW | 715 mW | 275 mW |
| J | 1375 mW | 11.0 mW/°C | 880 mW | 715 mW | 275 mW |
| N | 1150 mW | 9.2 mW/°C | 736 mW | 598 mW | 230 mW |
| PW | 700 mW | 5.6 mW/°C | 448 mW | 364 mW | 140 mW |

**TEXAS INSTRUMENTS**

## recommended operating conditions

| | TLC139M, TLC339M | | | UNIT |
|---|---|---|---|---|
| | MIN | NOM | MAX | |
| Supply voltage, $V_{DD}$ | 4 | 5 | 16 | V |
| Common-mode input voltage, $V_{IC}$ | 0 | | $V_{DD}-1.5$ | V |
| Low-level output current, $I_{OL}$ | | | 20 | mA |
| Operating free-air temperature, $T_A$ | −55 | | 125 | °C |

## electrical characteristics at specified operating free-air temperature, $V_{DD}$ = 5 V (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS† | $T_A$ | TLC139M, TLC339M | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | |
| $V_{IO}$ | Input offset voltage | $V_{IC}$ = $V_{ICR}$min, $V_{DD}$ = 5 V to 10 V, See Note 3 | 25°C | | 1.4 | 5 | mV |
| | | | −55°C to 125°C | | | 10 | |
| $I_{IO}$ | Input offset current | $V_{IC}$ = 2.5 V | 25°C | | 1 | | pA |
| | | | 125°C | | | 15 | nA |
| $I_{IB}$ | Input bias current | $V_{IC}$ = 2.5 V | 25°C | | 5 | | pA |
| | | | 125°C | | | 30 | nA |
| $V_{ICR}$ | Common-mode input voltage range | | 25°C | 0 to $V_{DD}-1$ | | | V |
| | | | −55°C to 125°C | 0 to $V_{DD}-1.5$ | | | |
| CMRR | Common-mode rejection ratio | $V_{IC}$ = $V_{ICR}$min | 25°C | | 84 | | dB |
| | | | 125°C | | 84 | | |
| | | | −55°C | | 84 | | |
| $k_{SVR}$ | Supply-voltage rejection ratio | $V_{DD}$ = 5 V to 10 V | 25°C | | 85 | | dB |
| | | | 125°C | | 84 | | |
| | | | −55°C | | 84 | | |
| $V_{OL}$ | Low-level output voltage | $V_{ID}$ = − 1 V, $I_{OL}$ = 6 mA | 25°C | | 300 | 400 | mV |
| | | | 125°C | | | 800 | |
| $I_{OH}$ | High-level output current | $V_{ID}$ = − 1 V, $V_O$ = 5 V | 25°C | | 0.8 | 40 | nA |
| | | | 125°C | | | 1 | μA |
| $I_{DD}$ | Supply current (four comparators) | Outputs low, No load | 25°C | | 44 | 80 | μA |
| | | | −55°C to 125°C | | | 175 | |

† All characteristics are measured with zero common-mode voltage unless otherwise noted.
NOTE 3: The offset voltage limits given are the maximum values required to drive the output up to 4.5 V or down to 0.3 V with a 2.5-kΩ load to $V_{DD}$.

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**TEXAS INSTRUMENTS**

## recommended operating conditions

| | | TLC339C | | | UNIT |
|---|---|---|---|---|---|
| | | MIN | NOM | MAX | |
| Supply voltage, $V_{DD}$ | | 3 | 5 | 16 | V |
| Common-mode input voltage, $V_{IC}$ | | −0.2 | | $V_{DD}$−1.5 | V |
| Low-level output current, $I_{OL}$ | | | 8 | 20 | mA |
| Operating free-air temperature, $T_A$ | | 0 | | 70 | °C |

## electrical characteristics at specified operating free-air temperature, $V_{DD}$ = 5 V (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS† | $T_A$ | TLC339C | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | |
| $V_{IO}$ | Input offset voltage | $V_{IC}$ = $V_{ICR}$min,     $V_{DD}$ = 5 V to 10 V, See Note 3 | 25°C | | 1.4 | 5 | mV |
| | | | 0°C to 70°C | | | 6.5 | |
| $I_{IO}$ | Input offset current | $V_{IC}$ = 2.5 V | 25°C | | 1 | | pA |
| | | | 70°C | | | 0.3 | nA |
| $I_{IB}$ | Input bias current | $V_{IC}$ = 2.5 V | 25°C | | 5 | | pA |
| | | | 70°C | | | 0.6 | nA |
| $V_{ICR}$ | Common-mode input voltage range | | 25°C | 0 to $V_{DD}$−1 | | | V |
| | | | 0°C to 70°C | 0 to $V_{DD}$−1.5 | | | |
| CMRR | Common-mode rejection ratio | $V_{IC}$ = $V_{ICR}$min | 25°C | | 84 | | dB |
| | | | 70°C | | 84 | | |
| | | | 0°C | | 84 | | |
| $k_{SVR}$ | Supply-voltage rejection ratio | $V_{DD}$ = 5 V to 10 V | 25°C | | 85 | | dB |
| | | | 70°C | | 85 | | |
| | | | 0°C | | 85 | | |
| $V_{OL}$ | Low-level output voltage | $V_{ID}$ = −1 V,     $I_{OL}$ = 6 mA | 25°C | | 300 | 400 | mV |
| | | | 70°C | | | 650 | |
| $I_{OH}$ | High-level output current | $V_{ID}$ = −1 V,     $V_O$ = 5 V | 25°C | | 0.8 | 40 | nA |
| | | | 70°C | | | 1 | µA |
| $I_{DD}$ | Supply current (four comparators) | Outputs low,     No load | 25°C | | 44 | 80 | µA |
| | | | 0°C to 70°C | | | 100 | |

† All characteristics are measured with zero common-mode voltage unless otherwise noted.
NOTE 4: The offset voltage limits given are the maximum values required to drive the output up to 4.5 V or down to 0.3 V with a 2.5-kΩ load to $V_{DD}$.

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## recommended operating conditions

| | TLC339I | | | UNIT |
|---|---|---|---|---|
| | MIN | NOM | MAX | |
| Supply voltage, $V_{DD}$ | 3 | 5 | 16 | V |
| Common-mode input voltage, $V_{IC}$ | −0.2 | | $V_{DD}$−1.5 | V |
| Low-level output current, $I_{OL}$ | | 8 | 20 | mA |
| Operating free-air temperature, $T_A$ | 0 | | 70 | °C |

## electrical characteristics at specified operating free-air temperature, $V_{DD}$ = 5 V (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS† | $T_A$ | TLC339I | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | |
| $V_{IO}$ | Input offset voltage | $V_{IC} = V_{ICR}$min,     $V_{DD}$ = 5 V to 10 V, See Note 3 | 25°C | | 1.4 | 5 | mV |
| | | | −40°C to 85°C | | | 7 | |
| $I_{IO}$ | Input offset current | $V_{IC}$ = 2.5 V | 25°C | | 1 | | pA |
| | | | 85°C | | | 1 | nA |
| $I_{IB}$ | Input bias current | $V_{IC}$ = 2.5 V | 25°C | | 5 | | pA |
| | | | 85°C | | | 2 | nA |
| $V_{ICR}$ | Common-mode input voltage range | | 25°C | 0 to $V_{DD}$−1 | | | V |
| | | | −40°C to 85°C | 0 to $V_{DD}$−1.5 | | | |
| CMRR | Common-mode rejection ratio | $V_{IC} = V_{ICR}$min | 25°C | | 84 | | dB |
| | | | 85°C | | 84 | | |
| | | | −40°C | | 84 | | |
| $k_{SVR}$ | Supply-voltage rejection ratio | $V_{DD}$ = 5 V to 10 V | 25°C | | 85 | | dB |
| | | | 85°C | | 85 | | |
| | | | −40°C | | 84 | | |
| $V_{OL}$ | Low-level output voltage | $V_{ID} = −1$ V,     $I_{OL}$ = 6 mA | 25°C | | 300 | 400 | mV |
| | | | 85°C | | | 700 | |
| $I_{OH}$ | High-level output current | $V_{ID} = −1$ V,     $V_O$ = 5 V | 25°C | | 0.8 | 40 | nA |
| | | | 85°C | | | 1 | μA |
| $I_{DD}$ | Supply current (four comparators) | Outputs low,     No load | 25°C | | 44 | 80 | μA |
| | | | −40°C to 85°C | | | 125 | |

† All characteristics are measured with zero common-mode voltage unless otherwise noted.
NOTE 3: The offset voltage limits given are the maximum values required to drive the output up to 4.5 V or down to 0.3 V with a 2.5-kΩ load to $V_{DD}$.

## recommended operating conditions

| | TLC339Q | | | UNIT |
|---|---|---|---|---|
| | MIN | NOM | MAX | |
| Supply voltage, $V_{DD}$ | 4 | 5 | 16 | V |
| Common-mode input voltage, $V_{IC}$ | 0 | | $V_{DD}-1.5$ | V |
| Low-level output current, $I_{OL}$ | | | 20 | mA |
| Operating free-air temperature, $T_A$ | −40 | | 125 | °C |

## electrical characteristics at specified operating free-air temperature, $V_{DD}$ = 5 V (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS† | $T_A$ | TLC339Q | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | |
| $V_{IO}$ | Input offset voltage | $V_{IC} = V_{ICR}$min, $V_{DD}$ = 5 V to 10 V, See Note 3 | 25°C | | 1.4 | 5 | mV |
| | | | −40°C to 125°C | | | 10 | |
| $I_{IO}$ | Input offset current | $V_{IC}$ = 2.5 V | 25°C | | 1 | | pA |
| | | | 125°C | | | 15 | nA |
| $I_{IB}$ | Input bias current | $V_{IC}$ = 2.5 V | 25°C | | 5 | | pA |
| | | | 125°C | | | 30 | nA |
| $V_{ICR}$ | Common-mode input voltage range | | 25°C | 0 to $V_{DD}-1$ | | | V |
| | | | −40°C to 125°C | 0 to $V_{DD}-1.5$ | | | |
| CMRR | Common-mode rejection ratio | $V_{IC} = V_{ICR}$min | 25°C | | 84 | | dB |
| | | | 125°C | | 84 | | |
| | | | −40°C | | 84 | | |
| $k_{SVR}$ | Supply-voltage rejection ratio | $V_{DD}$ = 5 V to 10 V | 25°C | | 85 | | dB |
| | | | 125°C | | 84 | | |
| | | | −40°C | | 84 | | |
| $V_{OL}$ | Low-level output voltage | $V_{ID}$ = −1 V, $I_{OL}$ = 6 mA | 25°C | | 300 | 400 | mV |
| | | | 125°C | | | 800 | |
| $I_{OH}$ | High-level output current | $V_{ID}$ = −1 V, $V_O$ = 5 V | 25°C | | 0.8 | 40 | nA |
| | | | 125°C | | | 1 | µA |
| $I_{DD}$ | Supply current (four comparators) | Outputs low, No load | 25°C | | 44 | 80 | µA |
| | | | −40°C to 125°C | | | 125 | |

† All characteristics are measured with zero common-mode voltage unless otherwise noted.
NOTE 4:   The offset voltage limits given are the maximum values required to drive the output up to 4.5 V or down to 0.3 V with a 2.5-kΩ load to $V_{DD}$.

**switching characteristics, $V_{DD}$ = 5 V, $T_A$ = 25°C (see Figure 3)**

| PARAMETER | | TEST CONDITIONS | | TLC139M, TLC339C TLC339I, TLC339M TLC339Q | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | |
| $t_{PLH}$ | Propagation delay time, low-to-high output | f = 10 kHz, $C_L$ = 15 pF | Overdrive = 2 mV | | 4.5 | | µs |
| | | | Overdrive = 5 mV | | 2.5 | | |
| | | | Overdrive = 10 mV | | 1.7 | | |
| | | | Overdrive = 20 mV | | 1.2 | | |
| | | | Overdrive = 40 mV | | 1.0 | | |
| | | $V_I$ = 1.4 V step at IN+ | | | 1.1 | | |
| $t_{PHL}$ | Propagation delay time, high-to-low level output | f = 10 kHz, $C_L$ = 15 pF | Overdrive = 2 mV | | 3.6 | | µs |
| | | | Overdrive = 5 mV | | 2.1 | | |
| | | | Overdrive = 10 mV | | 1.3 | | |
| | | | Overdrive = 20 mV | | 0.85 | | |
| | | | Overdrive = 40 mV | | 0.55 | | |
| | | $V_I$ = 1.4 V step at IN+ | | | 0.10 | | |
| $t_{THL}$ | Transition time, high-to-low level output | f = 10 kHz, $C_L$ = 15pF | Overdrive = 50 mV | | 20 | | ns |

## PARAMETER MEASUREMENT INFORMATION

The TLC139 and TLC339 contain a digital output stage that, if held in the linear region of the transfer curve, can cause damage to the device. Conventional operational amplifier/comparator testing incorporates the use of a servo-loop that is designed to force the device output to a level within this linear region. Since the servo-loop method of testing cannot be used, the following alternatives for testing parameters such as input offset voltage, common-mode rejection, etc., are suggested.

To verify that the input offset voltage falls within the limits specified, the limit value is applied to the input as shown in Figure 1(a). With the noninverting input positive with respect to the inverting input, the output should be high. With the input polarity reversed, the output should be low.

A similar test can be made to verify the input offset voltage at the common-mode extremes. The supply voltages can be slewed as shown in Figure 1(b) for the $V_{ICR}$ test, rather than changing the input voltages, to provide greater accuracy.
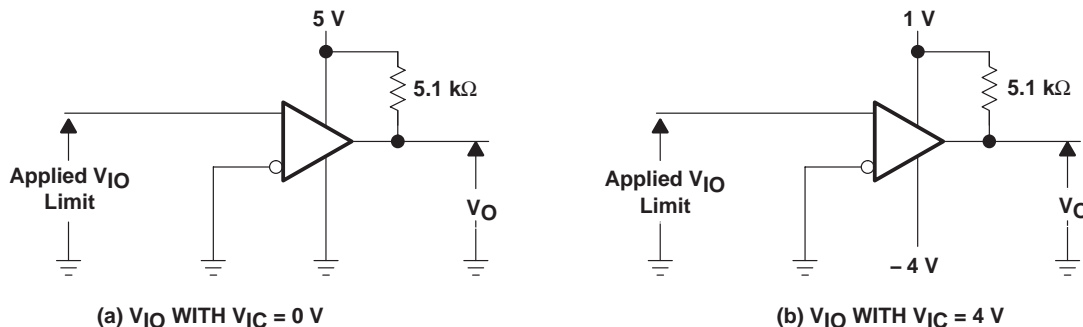


**Figure 1. Method for Verifying That Input Offset Voltage Is Within Specified Limits**

## PARAMETER MEASUREMENT INFORMATION

A close approximation of the input offset voltage can be obtained by using a binary search method to vary the differential input voltage while monitoring the output state. When the applied input voltage differential is equal but opposite in polarity to the input offset voltage, the output changes state.

Figure 2 illustrates a practical circuit for direct dc measurement of input offset voltage that does not bias the comparator into the linear region. The circuit consists of a switching mode servo loop in which U1A generates a triangular waveform of approximately 20-mV amplitude. U1B acts as a buffer, with C2 and R4 removing any residual dc offset. The signal is then applied to the inverting input of the comparator under test, while the noninverting input is driven by the output of the integrator formed by U1C through the voltage divider formed by R9 and R10. The loop reaches a stable operating point when the output of the comparator under test has a duty cycle of exactly 50%, which can only occur when the incoming triangle wave is sliced symmetrically or when the voltage at the noninverting input exactly equals the input offset voltage.

Voltage divider R9 and R10 provides a step-up of the input offset voltage by a factor of 100 to make measurement easier. The values of R5, R8, R9, and R10 can significantly influence the accuracy of the reading; therefore, it is suggested that their tolerance level be 1% or lower.
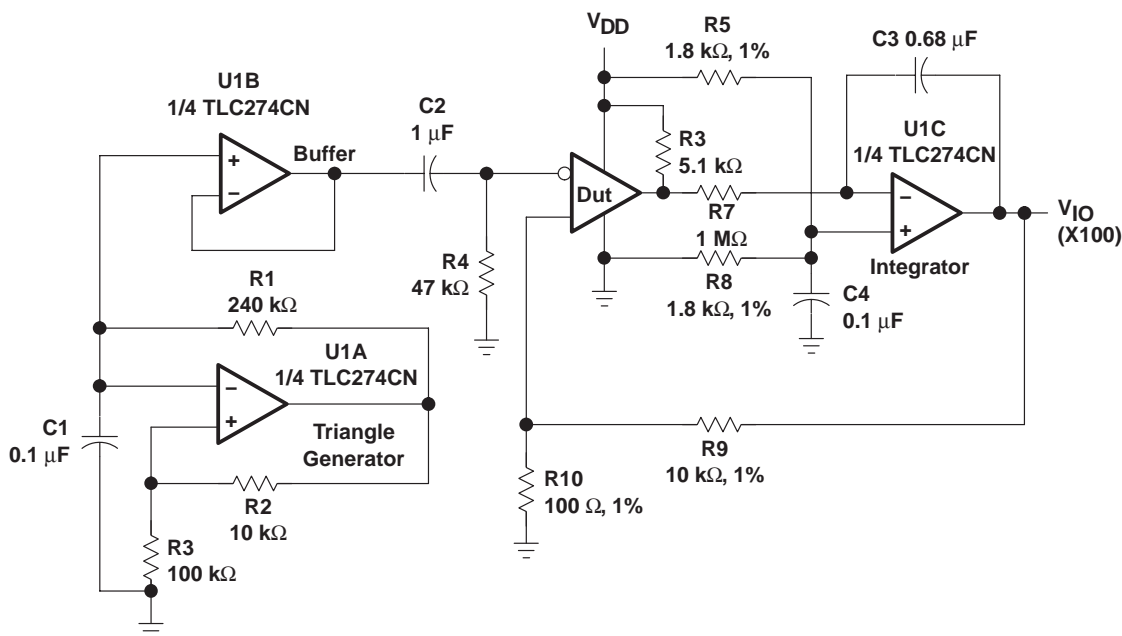


**Figure 2. Circuit for Input Offset Voltage Measurement**

Measuring the extremely low values of input current requires isolation from all other sources of leakage current and compensation for the leakage of the test socket and board. With a good picoammeter, the socket and board leakage can be measured with no device in the socket. Subsequently, this open socket leakage value can be subtracted from the measurement obtained, with a device in the socket to obtain the actual input current of the device.

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## PARAMETER MEASUREMENT INFORMATION

Propagation delay time is defined as the interval between the application of an input step function and the instant when the output reaches 50% of its maximum value. Propagation delay time, low-to-high-level output, is measured from the leading edge of the input pulse, while propagation delay time, high-to-low-level output, is measured from the trailing edge of the input pulse. Propagation delay time measurement at low input signal levels can be greatly affected by the input offset voltage. The offset voltage should be balanced by the adjustment at the inverting input as shown in Figure 3, so that the circuit is just at the transition point. Then a low signal, for example 105-mV or 5-mV overdrive, causes the output to change state.

**TEST CIRCUIT**

**VOLTAGE WAVEFORMS**

NOTE A: $C_L$ includes probe and jig capacitance.

**Figure 3. Propagation Delay, Rise, and Fall Times Test Circuit and Voltage Waveforms**

## TYPICAL CHARACTERISTICS

**Table of Graphs**

| | | | FIGURE |
|---|---|---|---|
| $V_{IO}$ | Input offset voltage | Distribution | 4 |
| $I_{IB}$ | Input bias current | vs Free-air temperature | 5 |
| CMRR | Common-mode rejection ratio | vs Free-air temperature | 6 |
| $k_{SVR}$ | Supply-voltage rejection ratio | vs Free-air temperature | 7 |
| $I_{OH}$ | High-level output current | vs High-level output voltage<br>vs Free-air temperature | 8<br>9 |
| $V_{OL}$ | Low-level output voltage | vs Low-level output current<br>vs Free-air temperature | 10<br>11 |
| $I_{DD}$ | Supply current | vs Supply voltage<br>vs Free-air temperature | 12<br>13 |
| $t_{PLH}$ | Low-to-high level output propagation delay time | vs Supply voltage | 14 |
| $t_{PHL}$ | Low-to-high level output propagation delay time | vs Supply voltage | 15 |
| | Overdrive voltage | vs Low-to-high-level output propagation delay time | 16 |
| $t_f$ | Output fall time | vs Supply voltage | 17 |
| | Overdrive voltage | vs High-to-low-level output propagation delay time | 18 |

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## TYPICAL CHARACTERISTICS†

**DISTRIBUTION OF INPUT
OFFSET VOLTAGE**



V_DD = 5 V
V_IC = 2.5 V
T_A = 25°C

**Figure 4**

**INPUT BIAS CURRENT
vs
FREE-AIR TEMPERATURE**



V_DD = 5 V
V_IC = 2.5 V

**Figure 5**

**COMMON-MODE REJECTION
RATIO
vs
FREE-AIR TEMPERATURE**



V_DD = 5 V

**Figure 6**

**SUPPLY-VOLTAGE REJECTION RATIO
vs
FREE-AIR TEMPERATURE**



V_DD = 5 V to 10 V
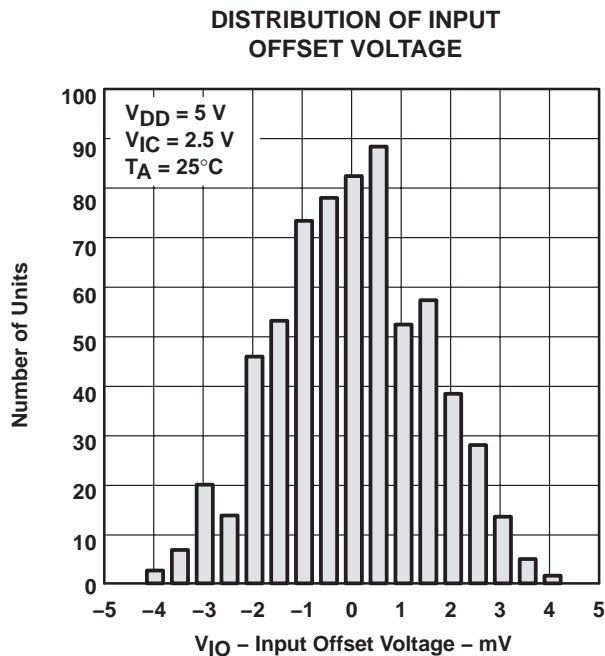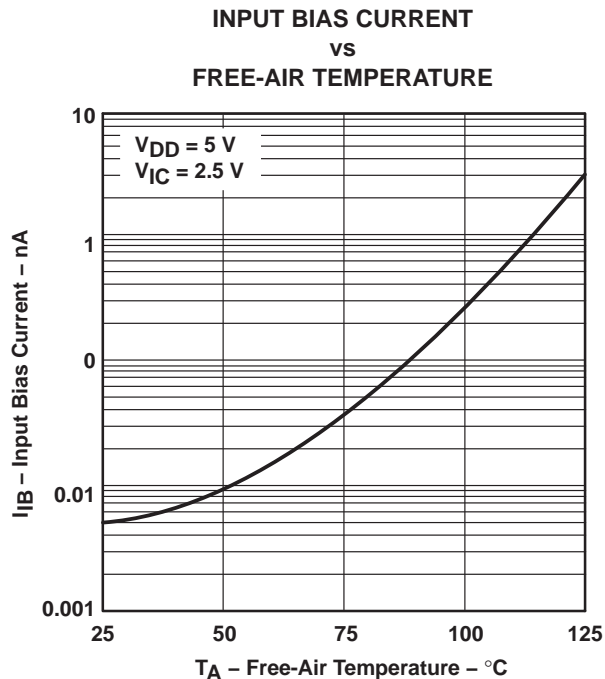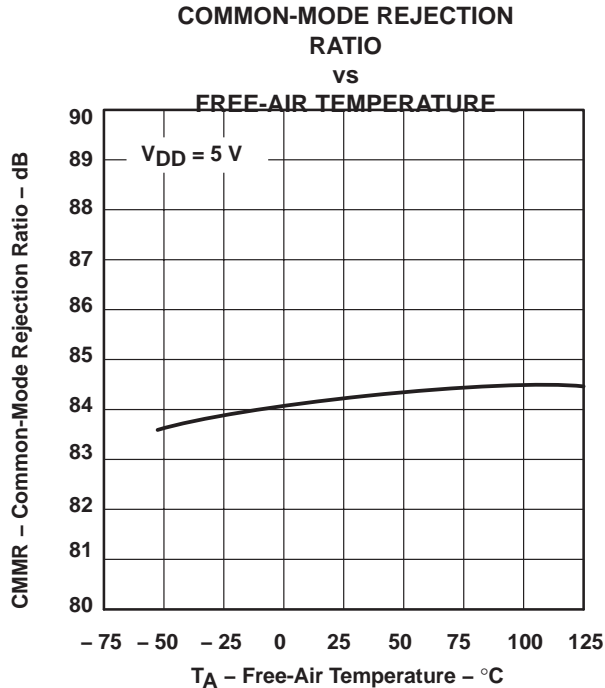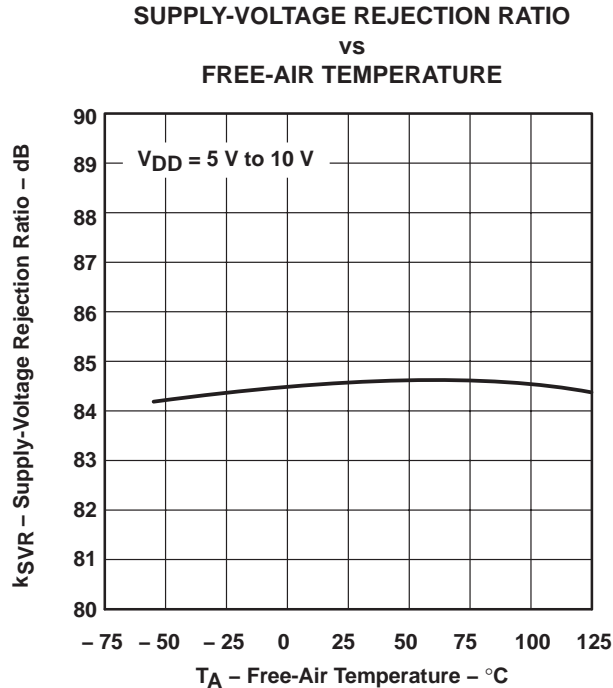
**Figure 7**

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

**TEXAS
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## TYPICAL CHARACTERISTICS†

### HIGH-LEVEL OUTPUT CURRENT
### vs
### HIGH-LEVEL OUTPUT VOLTAGE
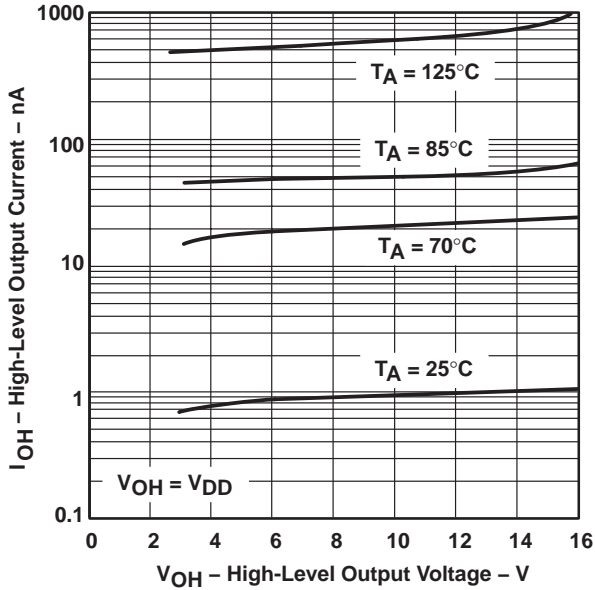


**Figure 8**

### HIGH-LEVEL OUTPUT CURRENT
### vs
### FREE-AIR TEMPERATURE
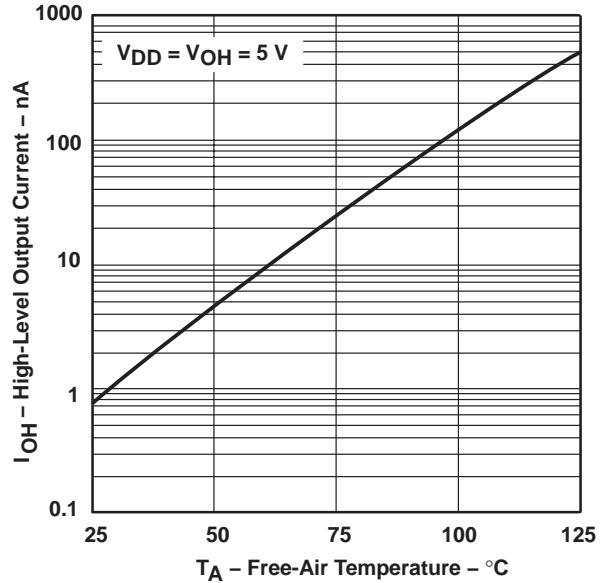


**Figure 9**

### LOW-LEVEL OUTPUT VOLTAGE
### vs
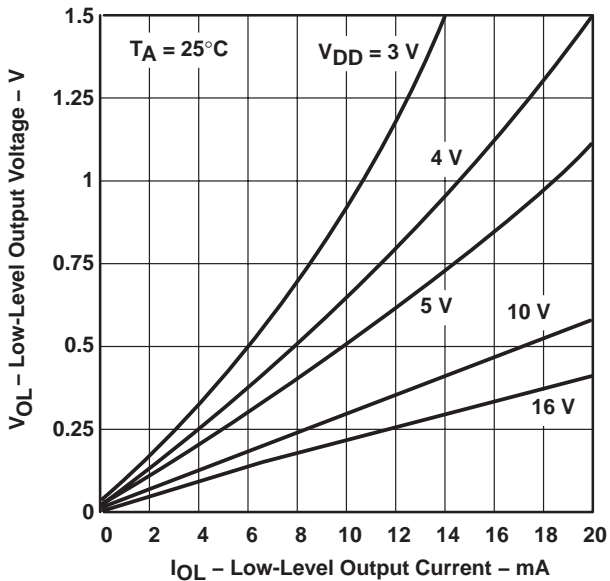### LOW-LEVEL OUTPUT CURRENT



**Figure 10**

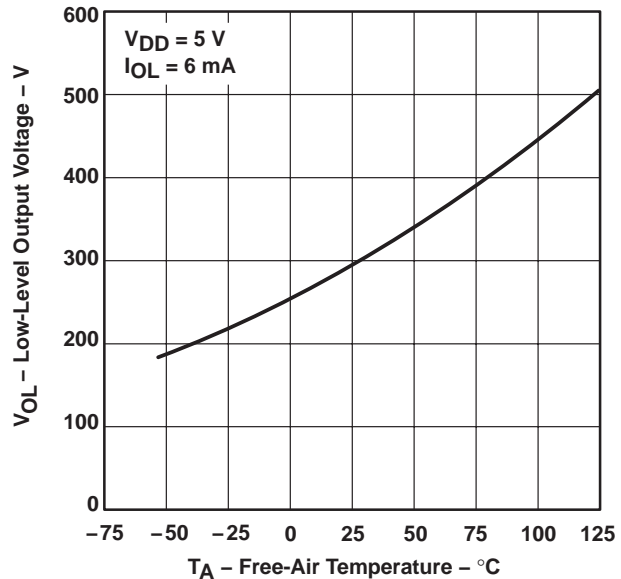### LOW-LEVEL OUTPUT VOLTAGE
### vs
### FREE-AIR TEMPERATURE



**Figure 11**

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
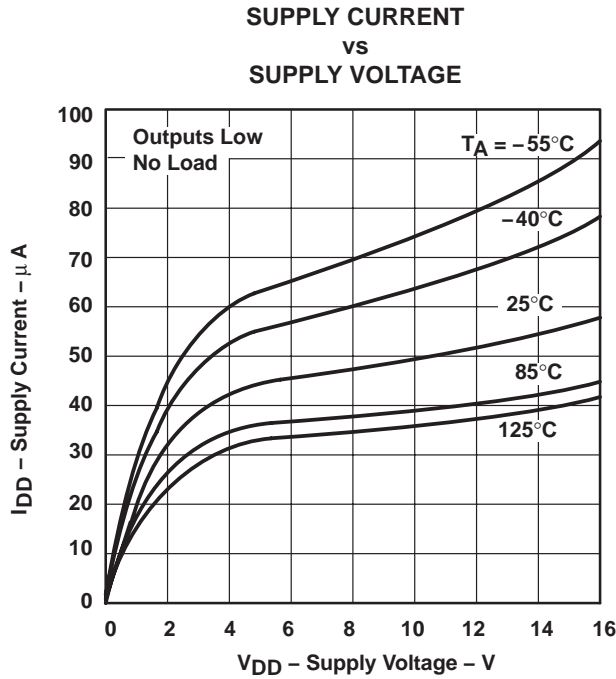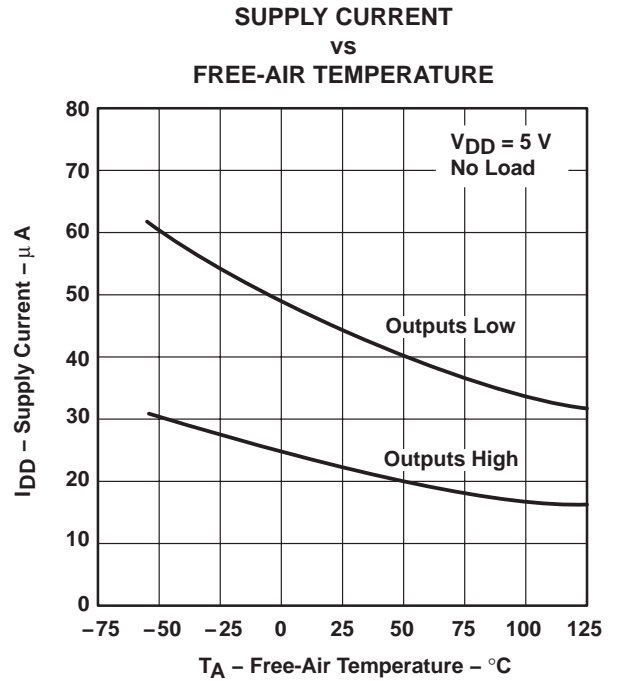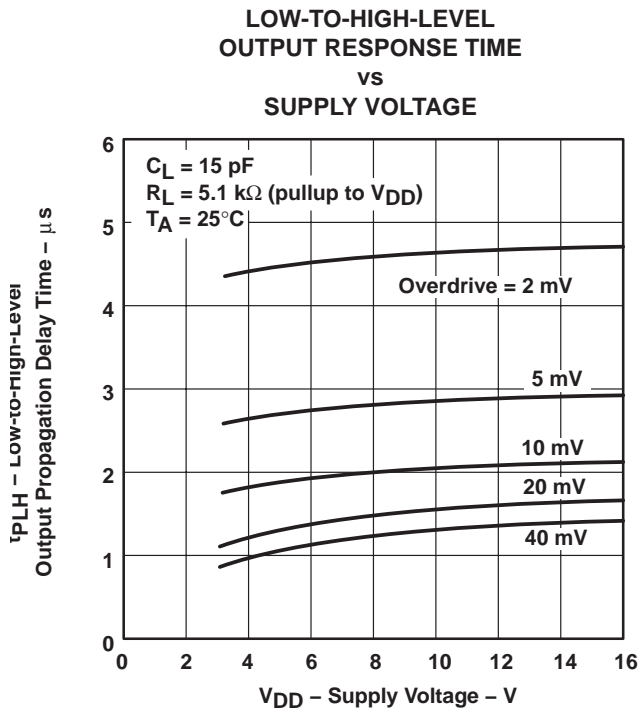
## TYPICAL CHARACTERISTICS†

**SUPPLY CURRENT**
**vs**
**SUPPLY VOLTAGE**

Outputs Low No Load. Curves for $T_A = -55°C$, $-40°C$, $25°C$, $85°C$, $125°C$. $I_{DD}$ – Supply Current – $\mu A$ (0 to 100) vs $V_{DD}$ – Supply Voltage – V (0 to 16).

**Figure 12**

**SUPPLY CURRENT**
**vs**
**FREE-AIR TEMPERATURE**

$V_{DD}$ = 5 V No Load. Curves for Outputs Low and Outputs High. $I_{DD}$ – Supply Current – $\mu A$ (0 to 80) vs $T_A$ – Free-Air Temperature – °C (−75 to 125).

**Figure 13**

**LOW-TO-HIGH-LEVEL**
**OUTPUT RESPONSE TIME**
**vs**
**SUPPLY VOLTAGE**

$C_L$ = 15 pF, $R_L$ = 5.1 k$\Omega$ (pullup to $V_{DD}$), $T_A$ = 25°C. Overdrive = 2 mV, 5 mV, 10 mV, 20 mV, 40 mV. $t_{PLH}$ – Low-to-High-Level Output Propagation Delay Time – $\mu s$ (0 to 6) vs $V_{DD}$ – Supply Voltage – V (0 to 16).

**Figure 14**

**HIGH-TO-LOW-LEVEL**
**OUTPUT RESPONSE TIME**
**vs**
**SUPPLY VOLTAGE**

$C_L$ = 15 pF, $R_L$ = 5.1 k$\Omega$ (pullup to $V_{DD}$), $T_A$ = 25°C. Overdrive = 2 mV, 5 mV, 10 mV, 20 mV, 40 mV. $t_{PHL}$ – High-to-Low-Level Output Propagation Delay Time – $\mu s$ (0 to 5) vs $V_{DD}$ – Supply Voltage – V (0 to 16).
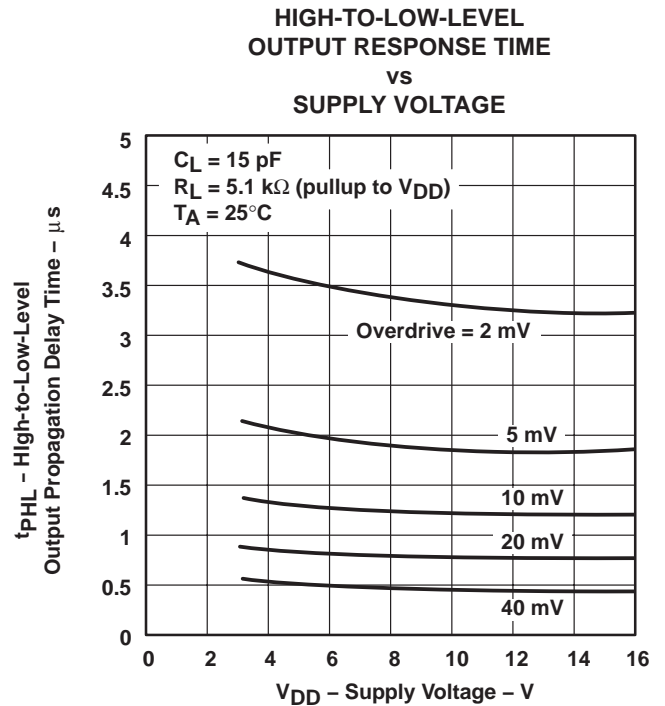
**Figure 15**

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

**TEXAS**
**INSTRUMENTS**

# TLC139, TLC339, TLC339Q
## LinCMOS™ MICROPOWER QUAD COMPARATORS

## TYPICAL CHARACTERISTICS

LOW-TO-HIGH-LEVEL OUTPUT
PROPAGATION DELAY
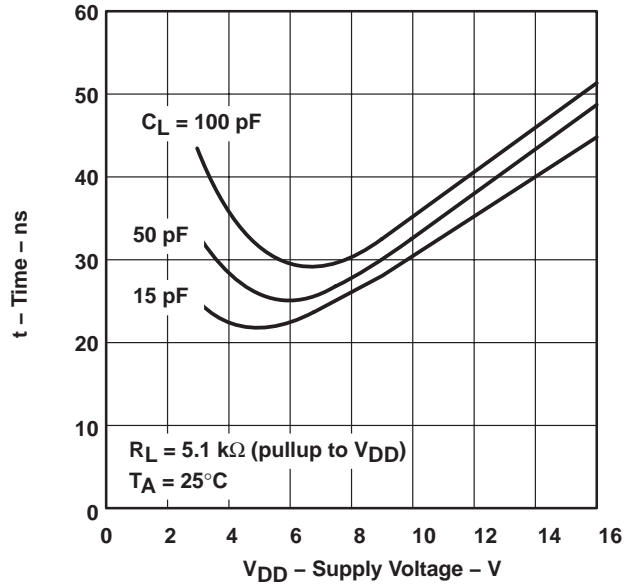FOR VARIOUS OVERDRIVE VOLTAGES

OUTPUT FALL TIME
vs
SUPPLY VOLTAGE



Figure 16



Figure 17

HIGH-TO-LOW-LEVEL OUTPUT
PROPAGATION DELAY
FOR VARIOUS OVERDRIVE VOLTAGES



Figure 18

![Texas Instruments logo]
TEXAS
INSTRUMENTS
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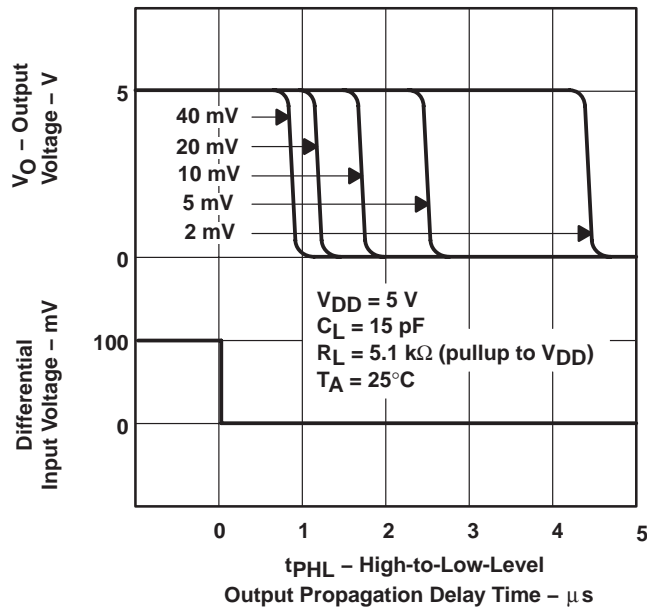## APPLICATION INFORMATION

The inputs should always remain within the supply rails in order to avoid forward biasing the diodes in the electrostatic discharge (ESD) protection structure. If either input exceeds this range, the device is not damaged as long as the input current is limited to less than 5 mA. To maintain the expected output state, the inputs must remain within the common-mode range. For example, at 25°C with $V_{DD}$ = 5 V, both inputs must remain between $-0.2$ V and 4 V to assure proper device operation. To assure reliable operation, the supply should be decoupled with a capacitor (0.1 µF) positioned as close to the device as possible.

The output and supply currents require close observation since the TLC139/TLC339 does not provide current protection. For example, each output can source or sink a maximum of 20 mA; however, the total current to ground has an absolute maximum of 60 mA. This prohibits sinking 20 mA from each of the four outputs simultaneously since the total current to ground would be 80 mA.

The TLC139 and TLC339 have internal ESD-protection circuits that prevent functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2; however, exercise care when handling these devices as exposure to ESD may result in the degradation of the device parametric performance.

**Table of Applications**

|  | FIGURE |
|---|---|
| Pulse-width-modulated motor speed controller | 19 |
| Enhanced supply supervisor | 20 |
| Two-phase nonoverlapping clock generator | 21 |
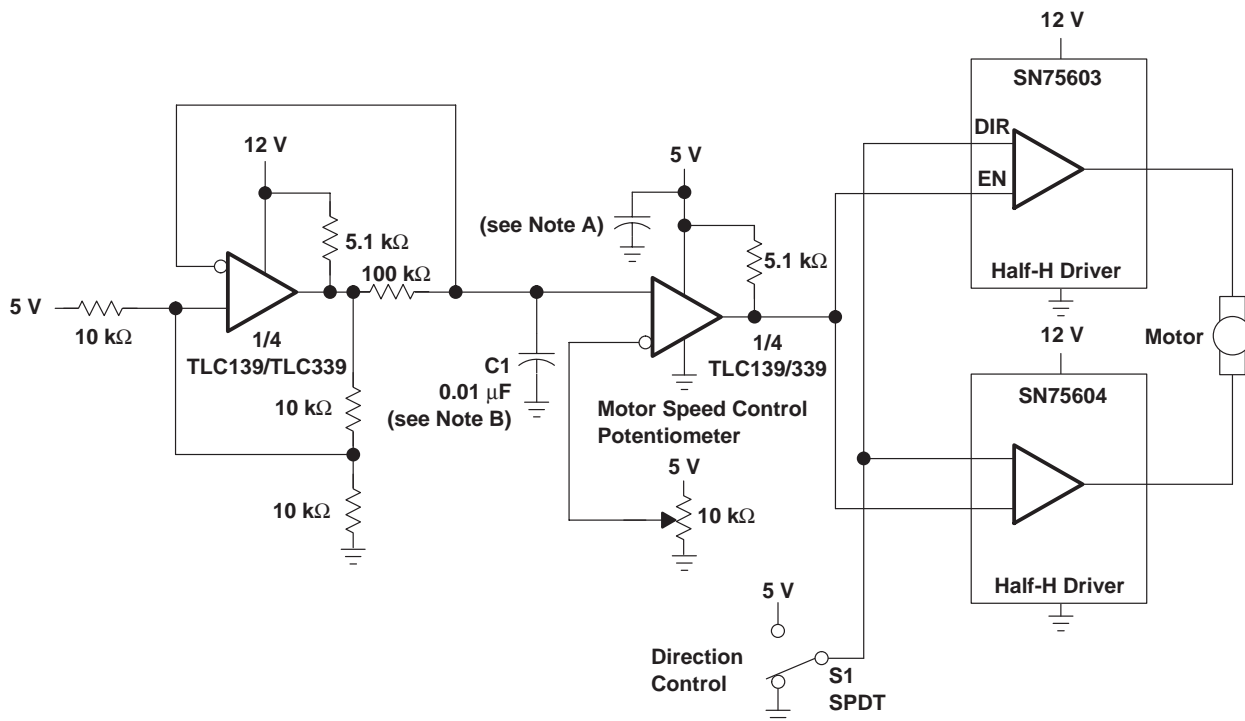


NOTES: A. The recommended minimum capacitance is 10 µF to eliminate common ground switching noise.
B. Select C1 for change in oscillator frequency.

**Figure 19. Pulse-Width-Modulated Motor Speed Controller**

## TYPICAL APPLICATION DATA
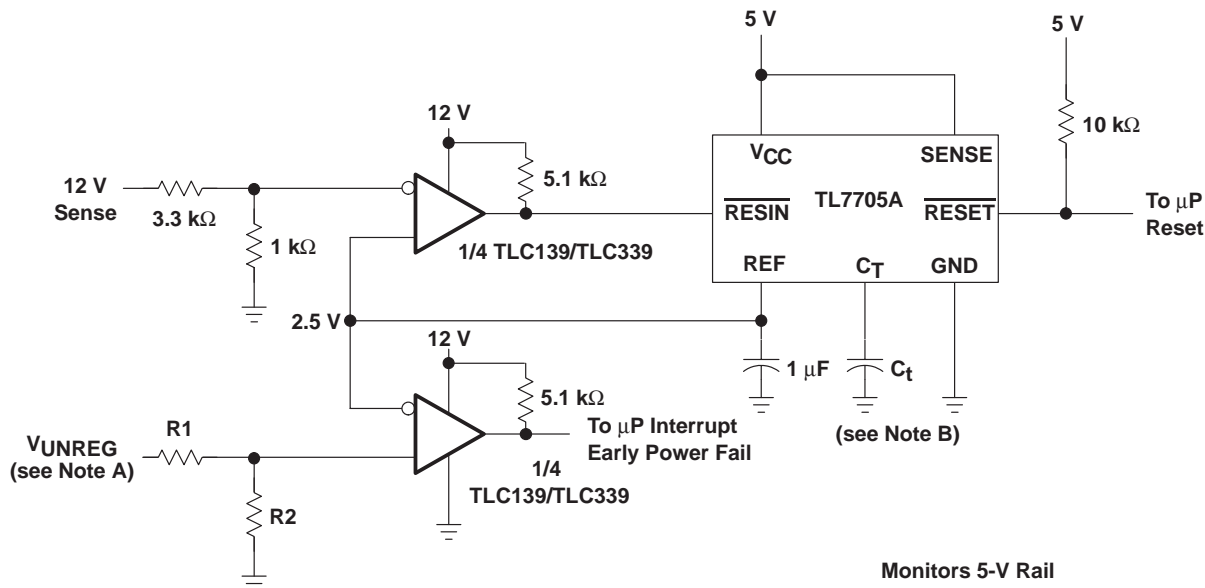


NOTES: A. $V_{UNREG} = 2.5 \left( \dfrac{R1 \ + \ R2}{R2} \right)$

      B. The value of $C_t$ determines the time delay of reset.

**Figure 20. Enhanced Supply Supervisor**
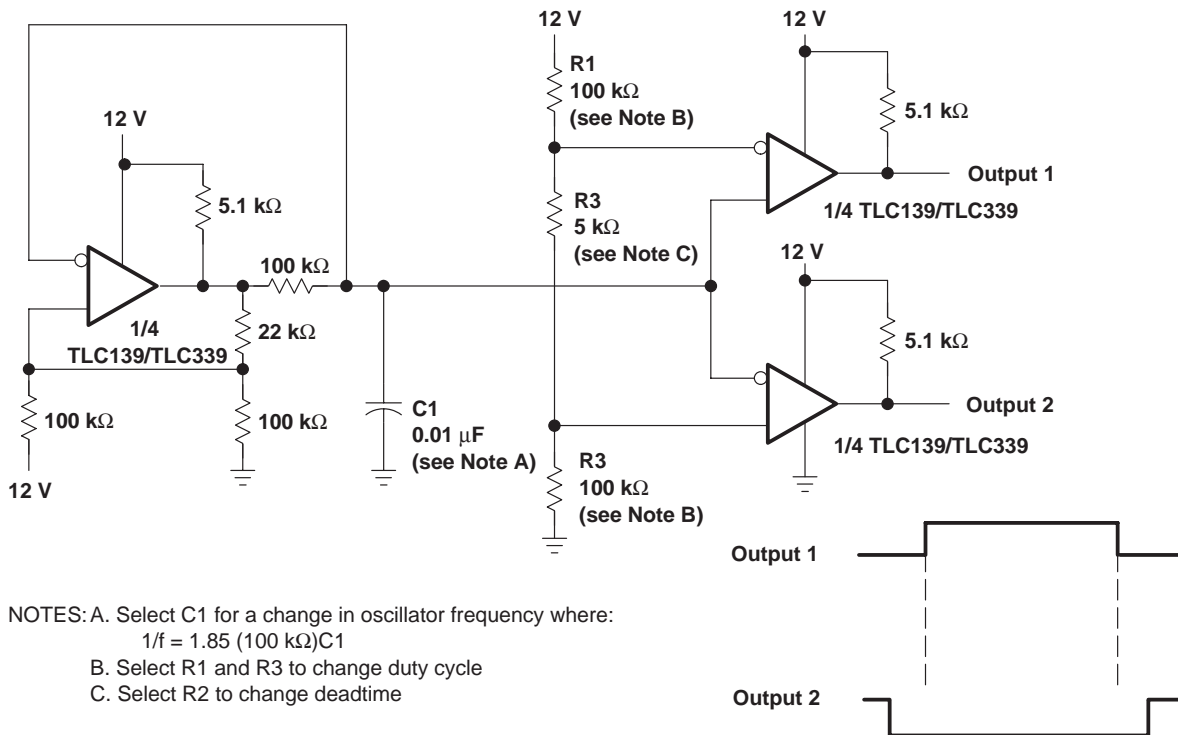


NOTES: A. Select C1 for a change in oscillator frequency where:
           $1/f = 1.85 \ (100 \ \text{k}\Omega)\text{C1}$
      B. Select R1 and R3 to change duty cycle
      C. Select R2 to change deadtime

**Figure 21. Two-Phase Nonoverlapping Clock Generator**

TEXAS
INSTRUMENTS
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## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 5962-87659022A | ACTIVE | LCCC | FK | 20 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-87659022A TLC139MFKB | Samples |
| 5962-8765902CA | ACTIVE | CDIP | J | 14 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-8765902CA TLC139MJB | Samples |
| 5962-9555001NXD | ACTIVE | SOIC | D | 14 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | | QTLC139M | Samples |
| 5962-9555001NXDR | ACTIVE | SOIC | D | 14 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | | QTLC139M | Samples |
| TLC139MFKB | ACTIVE | LCCC | FK | 20 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | | 5962-87659022A TLC139MFKB | Samples |
| TLC139MJB | ACTIVE | CDIP | J | 14 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | | 5962-8765902CA TLC139MJB | Samples |
| TLC339CD | ACTIVE | SOIC | D | 14 | 50 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | | TLC339C | Samples |
| TLC339CDR | ACTIVE | SOIC | D | 14 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | | TLC339C | Samples |
| TLC339CN | ACTIVE | PDIP | N | 14 | 25 | RoHS & Green | NIPDAU | N / A for Pkg Type | | TLC339CN | Samples |
| TLC339CNSR | ACTIVE | SO | NS | 14 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | | TLC339 | Samples |
| TLC339CPW | ACTIVE | TSSOP | PW | 14 | 90 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | | P339 | Samples |
| TLC339CPWG4 | ACTIVE | TSSOP | PW | 14 | 90 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | | P339 | Samples |
| TLC339CPWR | ACTIVE | TSSOP | PW | 14 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | | P339 | Samples |
| TLC339ID | ACTIVE | SOIC | D | 14 | 50 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | | TLC339I | Samples |
| TLC339IDR | ACTIVE | SOIC | D | 14 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | | TLC339I | Samples |
| TLC339IDRG4 | ACTIVE | SOIC | D | 14 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | | TLC339I | Samples |
| TLC339IN | ACTIVE | PDIP | N | 14 | 25 | RoHS & Green | NIPDAU | N / A for Pkg Type | | TLC339IN | Samples |
| TLC339IPW | ACTIVE | TSSOP | PW | 14 | 90 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | | TLC339I | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TLC339IPWR | ACTIVE | TSSOP | PW | 14 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | | TLC339I | Samples |
| TLC339MD | ACTIVE | SOIC | D | 14 | 50 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | TLC339M | Samples |
| TLC339MDG4 | ACTIVE | SOIC | D | 14 | 50 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | TLC339M | Samples |
| TLC339MDR | ACTIVE | SOIC | D | 14 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | TLC339M | Samples |
| TLC339MDRG4 | ACTIVE | SOIC | D | 14 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | TLC339M | Samples |
| TLC339MN | ACTIVE | PDIP | N | 14 | 25 | RoHS & Green | NIPDAU | N / A for Pkg Type | -55 to 125 | TLC339MN | Samples |

**(1)** The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

**(2)** **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

**(3)** MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

**(4)** There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

**(5)** Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

**(6)** Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

# PACKAGE MATERIALS INFORMATION

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

**TAPE DIMENSIONS**



| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 5962-9555001NXDR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| TLC339CDR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| TLC339CNSR | SO | NS | 14 | 2000 | 330.0 | 16.4 | 8.2 | 10.5 | 2.5 | 12.0 | 16.0 | Q1 |
| TLC339CPWR | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| TLC339IDR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| TLC339IPWR | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| TLC339MDR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| TLC339MDRG4 | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |

# PACKAGE MATERIALS INFORMATION

**TAPE AND REEL BOX DIMENSIONS**



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| 5962-9555001NXDR | SOIC | D | 14 | 2500 | 350.0 | 350.0 | 43.0 |
| TLC339CDR | SOIC | D | 14 | 2500 | 350.0 | 350.0 | 43.0 |
| TLC339CNSR | SO | NS | 14 | 2000 | 853.0 | 449.0 | 35.0 |
| TLC339CPWR | TSSOP | PW | 14 | 2000 | 853.0 | 449.0 | 35.0 |
| TLC339IDR | SOIC | D | 14 | 2500 | 340.5 | 336.1 | 32.0 |
| TLC339IPWR | TSSOP | PW | 14 | 2000 | 853.0 | 449.0 | 35.0 |
| TLC339MDR | SOIC | D | 14 | 2500 | 350.0 | 350.0 | 43.0 |
| TLC339MDRG4 | SOIC | D | 14 | 2500 | 350.0 | 350.0 | 43.0 |

FK (S−CQCC−N**)                    LEADLESS CERAMIC CHIP CARRIER
28 TERMINAL SHOWN

| NO. OF TERMINALS ** | A | | B | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| 20 | 0.342 (8,69) | 0.358 (9,09) | 0.307 (7,80) | 0.358 (9,09) |
| 28 | 0.442 (11,23) | 0.458 (11,63) | 0.406 (10,31) | 0.458 (11,63) |
| 44 | 0.640 (16,26) | 0.660 (16,76) | 0.495 (12,58) | 0.560 (14,22) |
| 52 | 0.740 (18,78) | 0.761 (19,32) | 0.495 (12,58) | 0.560 (14,22) |
| 68 | 0.938 (23,83) | 0.962 (24,43) | 0.850 (21,6) | 0.858 (21,8) |
| 84 | 1.141 (28,99) | 1.165 (29,59) | 1.047 (26,6) | 1.063 (27,0) |

$\dfrac{0.020\ (0,51)}{0.010\ (0,25)}$

$\dfrac{0.020\ (0,51)}{0.010\ (0,25)}$

$\dfrac{0.080\ (2,03)}{0.064\ (1,63)}$

$\dfrac{0.055\ (1,40)}{0.045\ (1,14)}$

$\dfrac{0.045\ (1,14)}{0.035\ (0,89)}$

$\dfrac{0.028\ (0,71)}{0.022\ (0,54)}$

0.050 (1,27)

$\dfrac{0.045\ (1,14)}{0.035\ (0,89)}$

4040140/D 01/11

NOTES:    A.   All linear dimensions are in inches (millimeters).
          B.   This drawing is subject to change without notice.
          C.   This package can be hermetically sealed with a metal lid.
          D.   Falls within JEDEC MS−004

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## MECHANICAL DATA

| | PINS ** | 14 | 16 | 20 | 24 |
|---|---|---|---|---|---|
| DIM | | | | | |
| A MAX | | 10,50 | 10,50 | 12,90 | 15,30 |
| A MIN | | 9,90 | 9,90 | 12,30 | 14,70 |

4040062/C 03/03

NOTES:   A.   All linear dimensions are in millimeters.
    B.   This drawing is subject to change without notice.
    C.   Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

TEXAS
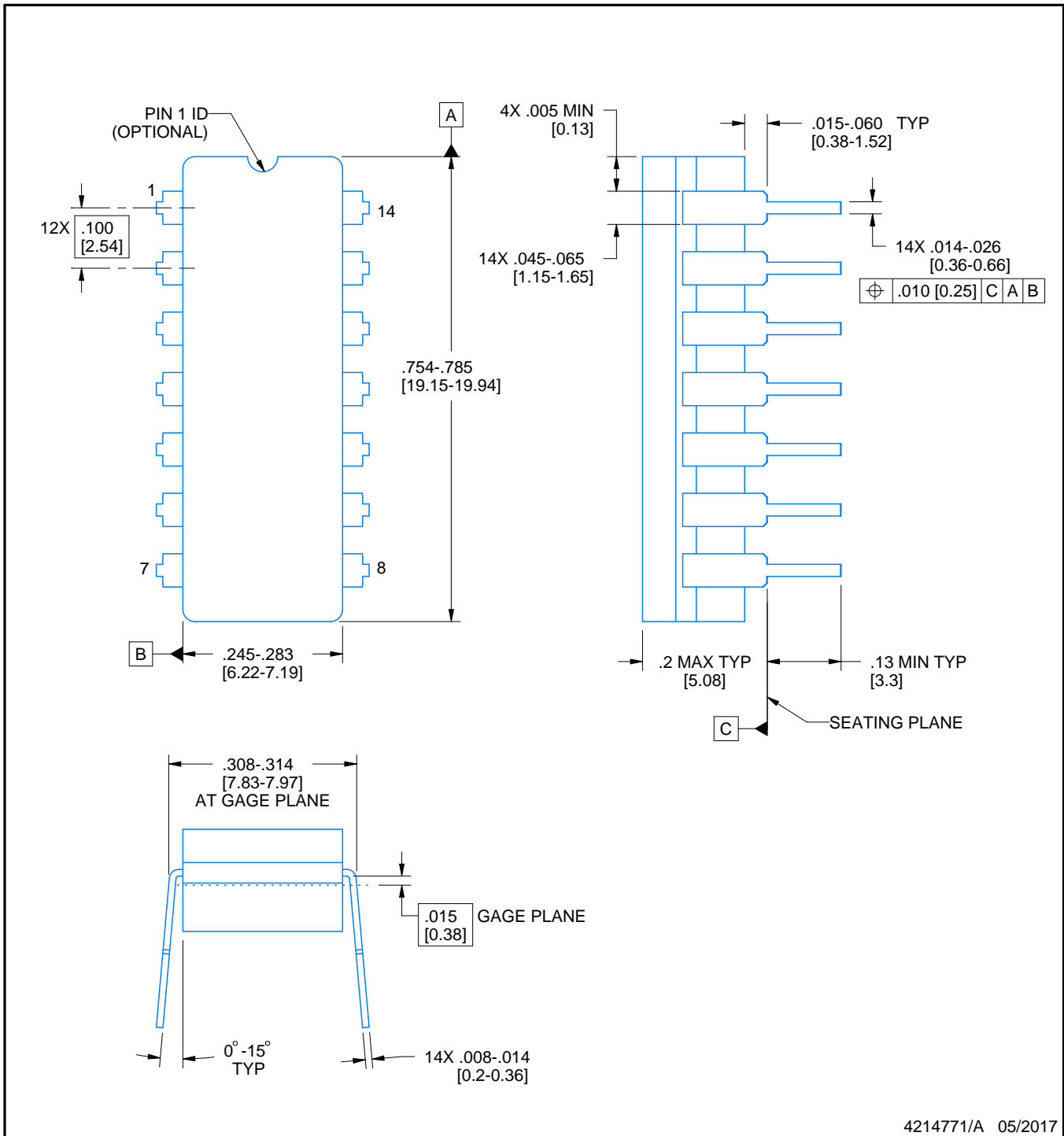INSTRUMENTS

PIN 1 ID
(OPTIONAL)

A

1

14

12X .100
[2.54]

.754-.785
[19.15-19.94]

7

8

B

.245-.283
[6.22-7.19]

4X .005 MIN
[0.13]

.015-.060 TYP
[0.38-1.52]

14X .045-.065
[1.15-1.65]

14X .014-.026
[0.36-0.66]

⊕ .010 [0.25] C A B

.2 MAX TYP
[5.08]

.13 MIN TYP
[3.3]

C

SEATING PLANE

.308-.314
[7.83-7.97]
AT GAGE PLANE

.015
[0.38]

GAGE PLANE

0°-15°
TYP

14X .008-.014
[0.2-0.36]

4214771/A   05/2017

NOTES:

1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermitically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

## J0014A

SEE DETAIL A

SEE DETAIL B

(.300 ) TYP
[7.62]

1

14

12X (.100 )
[2.54]

SYMM
₵

14X (⌀ .039)
[1]

7

8

SYMM
₵

LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X

.002  MAX
[0.05]
ALL AROUND

(.063)
[1.6]

SOLDER MASK
OPENING

METAL

(R.002 ) TYP
[0.05]

DETAIL A
SCALE: 15X

METAL

(⌀ .063)
[1.6]

SOLDER MASK
OPENING

.002  MAX
[0.05]
ALL AROUND

DETAIL B
13X, SCALE: 15X

4214771/A   05/2017

D (R−PDSO−G14)                                    PLASTIC SMALL OUTLINE



0.344 (8,75)
0.337 (8,55)
C

14                                                8

0.244 (6,20)
0.228 (5,80)

0.157 (4,00)
0.150 (3,80)  D

1                                                 7

Pin 1
Index Area

0.050 (1,27)

0.020 (0,51)
0.012 (0,31)

⊕ 0.010 (0,25) M

0.069 (1,75) Max

0.010 (0,25)
0.004 (0,10)

0.004 (0,10)

0.010 (0,25)
0.005 (0,13)

Gauge Plane

Seating Plane

0.010 (0,25)        0°−8°

0.050 (1,27)
0.016 (0,40)

4040047−5/M   06/11

NOTES:   A.   All linear dimensions are in inches (millimeters).
         B.   This drawing is subject to change without notice.
         C.   Body length does not include mold flash, protrusions, or gate burrs.  Mold flash, protrusions, or gate burrs shall
              not exceed 0.006 (0,15) each side.
         D.   Body width does not include interlead flash.  Interlead flash shall not exceed 0.017 (0,43) each side.
         E.   Reference JEDEC MS−012 variation AB.

**TEXAS**
**INSTRUMENTS**
www.ti.com

D (R−PDSO−G14)                    PLASTIC SMALL OUTLINE

Example Board Layout
(Note C)

|←12x1,27

5,40

Example
Non Soldermask Defined Pad

Example
Pad Geometry
(See Note C)

←0,60

1,55

←0.07
All Around

Example
Solder Mask Opening
(See Note E)

Stencil Openings
(Note D)

←14x0,55

14x1,50

|←12x1,27

5,40

4211283−3/E  08/12

NOTES:  A.  All linear dimensions are in millimeters.
        B.  This drawing is subject to change without notice.
        C.  Publication IPC−7351 is recommended for alternate designs.
        D.  Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release.  Customers should
            contact their board assembly site for stencil design recommendations. Refer to IPC−7525 for other stencil recommendations.
        E.  Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

**TEXAS INSTRUMENTS**
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PW (R−PDSO−G14)  PLASTIC SMALL OUTLINE

0,65

0,30
0,19

⊕ 0,10 Ⓜ

14

8

D  4,50
4,30

6,60
6,20

1

7

5,10
4,90

C

0,15 NOM

Gage Plane

0,25

0°−8°

0,75
0,50

1,20 MAX

0,15
0,05

Seating Plane

⌀ 0,10

4040064−3/G  02/11

NOTES:  A.  All linear dimensions are in millimeters.  Dimensioning and tolerancing per ASME Y14.5M−1994.
B.  This drawing is subject to change without notice.
C.  Body length does not include mold flash, protrusions, or gate burrs.  Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D.  Body width does not include interlead flash.  Interlead flash shall not exceed 0,25 each side.
E.  Falls within JEDEC MO−153

**TEXAS INSTRUMENTS**
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## N (R−PDIP−T**)

16 PINS SHOWN

## PLASTIC DUAL−IN−LINE PACKAGE

| DIM / PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A MAX | 0.775 (19,69) | 0.775 (19,69) | 0.920 (23,37) | 1.060 (26,92) |
| A MIN | 0.745 (18,92) | 0.745 (18,92) | 0.850 (21,59) | 0.940 (23,88) |
| MS−001 VARIATION | AA | BB | AC | AD |

A

16          9

0.260 (6,60)
0.240 (6,10)

1          8

0.070 (1,78)
0.045 (1,14)  △D

0.045 (1,14)
0.030 (0,76)  △D

0.020 (0,51) MIN

0.325 (8,26)
0.300 (7,62)

0.015 (0,38)

Gauge Plane

0.200 (5,08) MAX

Seating Plane

0.010 (0,25) NOM

0.125 (3,18) MIN

0.100 (2,54)

0.430 (10,92) MAX

0.021 (0,53)
0.015 (0,38)

⊕ 0.010 (0,25) Ⓜ

14/18 Pin Only
20 Pin vendor option  △D

4040049/E  12/2002

NOTES:   A.   All linear dimensions are in inches (millimeters).
         B.   This drawing is subject to change without notice.
      △C   Falls within JEDEC MS−001, except 18 and 20 pin minimum body length (Dim A).
      △D   The 20 pin end lead shoulder width is a vendor option, either half or full width.

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